Intel Agilex® 7 Device Family High-Speed Serial Interface Signal Integrity Design Guidelines

Online Version
Send Feedback

UG-20298

683864
2023.06.15

Contents

1. Signal Integrity (SI) in High-Speed PCB Designs

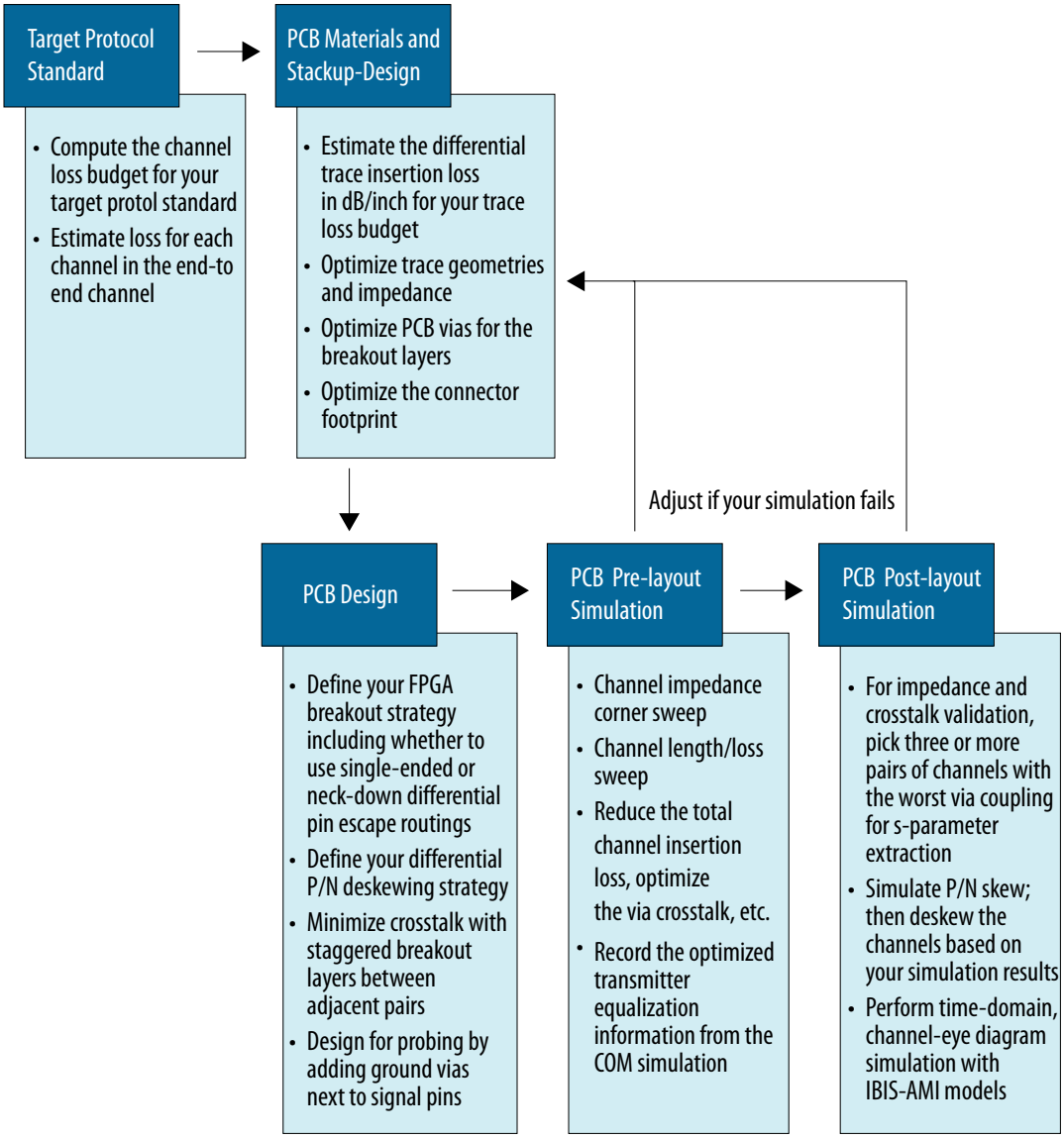
Many factors impact high-speed, serial interface signal integrity, for example, insertion loss (IL), insertion loss deviation (ILD), return loss (RL), crosstalk, and mode conversion. To mitigate these factors, first determine the loss budget for your targeted protocol. Second, select PCB materials and a stackup design that allow you to stay under your loss budget. Then design your PCB with these materials, and run channel compliance analysis.

The final steps are post-layout model extraction and end-to-end system simulation. Use IBIS-AMI models to conduct full-channel, end-to-end eye diagram simulations at the target BER level of your targeted protocol. For more details about IBIS-AMI models, contact Intel Premier Support and quote ID #14017451502 .

Intel Corporation. All rights reserved. Intel, the Intel logo, and other Intel marks are trademarks of Intel Corporation or its subsidiaries. Intel warrants performance of its FPGA and semiconductor products to current specifications in accordance with Intel's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.
*Other names and brands may be claimed as the property of others.

ISO 9001:2015 Registered

Figure 1. Signal Integrity Flow in High-Speed PCB Designs



Related Information

My Intel Support

1.1. Supported Protocols

For supported protocols, refer to the *Intel Agilex® 7 FPGAs and SoCs Device Overview*. For device characteristics, refer to the *Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series*. For transceiver details, refer to the relevant transceiver user guide. For protocol-specific layout requirements, refer to the relevant protocol specification.

Related Information

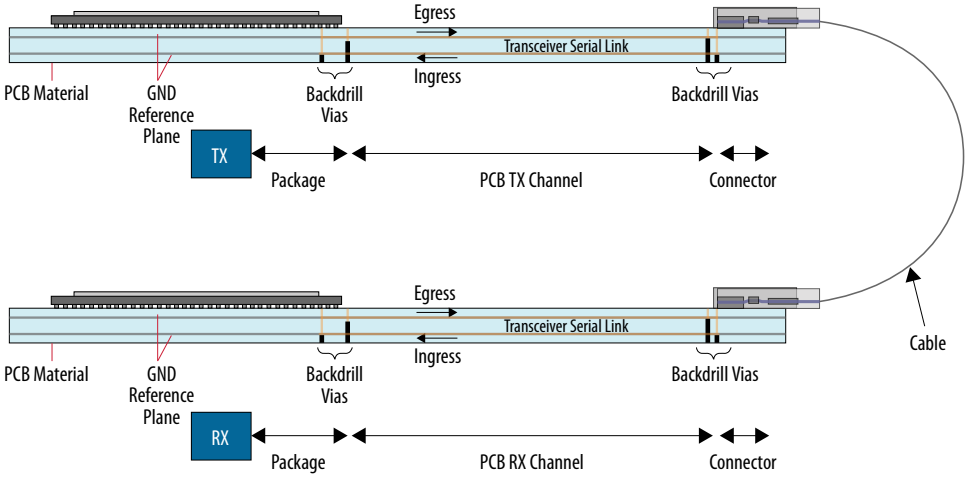
- Intel Agilex 7 FPGAs and SoCs Device Overview
- Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series
- E-Tile Transceiver PHY User Guide

1.2. Channel Insertion Loss (IL) Budget Calculation

The following figure is an example of a channel IL budget calculation for an end-to-end (TP0 to TP5) 200GBASE-CR4 channel, with the IL estimation at the Nyquist frequency for each channel component provided. Estimate the minimum and maximum insertion loss allocations for each component of the channel (from the transmitter to the receiver) to meet the link standard budget (for example, IEEE 802.3cd).

Figure 2. 200GBase-CR4 End-to-End Channel IL Estimation Example

Assign a few dB of margin to the end-to-end channel PCB design to account for PCB manufacturing and process, voltage, and temperature (PVT) variations.



Nyquist frequency 13.28 GHz
IL (TX PCB Via) = -1dB
IL (TX PCB Trace) = -6dB
IL (TX Connector + footprint) = -1.45dB
IL (Cable) = -12dB
IL (RX Connector + footprint) = -1.45dB
IL (RX PCB Trace) = -6dB
IL (RX PCB Via) = -1dB
Total IL = sum of IL = -28.9dB (the compliance budget is 30dB TP0 to TP5)

1.3. PCB Materials and Stackup Design Guidelines

The PCB stackup is the substrate upon which all design components are assembled. A well-designed PCB stackup can maximize the electrical performance of signal transmissions, power delivery, manufacturability, and long-term reliability of the finished product.

You need to know the following to decide the required number of signal and power layers:

- Board thickness requirements
- Connector requirement. For example, gold finger.
- Mechanical limitations
- PCB manufacturing capability limitations
- Your critical devices and their placement requirements
- High-speed signal data rate and connection requirements
- External memory interface configuration requirements
- The power tree and power budget for each power rail

1.3.1. Mitigating Insertion Loss with Dielectric Material

PCB routing from FPGA device to high-speed connectors has very strict IL requirements, for example, high speed Ethernet to the optical module interface and PCI Express* (PCIe) to the gold finger interface.

- Use the following dielectric constant (Dk) and dissipation factor (Df) values as a reference only for low-loss and ultra-low-loss dielectric materials. Test your design with a vector network analyzer (VNA).
  - Dk =3.5 and Df =0.007 (at 1 GHz) for low-loss material
  - Dk =3.4 and Df =0.002 (at 1 GHz) for ultra-low-loss material
- Use low-surface-roughness copper materials such as RTF2, VLP, HVLP, and HVLP2 copper to mitigate insertion loss caused by the skin effect. Copper resistance is a function of frequency, as when the frequency increases, the resistive loss increases because of the skin effect. This skin effect reduces the cross-sectional area of the transmission line, which increases the copper resistance.
- Use thick dielectric material (with the corresponding wider traces) for high-speed differential channel routing layers. Wider traces increase the effective surface area and reduce the sheet resistance.

1.3.2. Power Layers

For details about designing your power distribution network (PDN), see the *AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines*.

- Use 1 or 2 oz. thick copper foil where it is possible to provide a stronger current carrying capability in the same routing space.
- For high current power rails, like the core power rail which may carry a current of more than 100 A, use multi-layers in parallel.
- When designing in multiple planes for a single supply, add enough stitching vias for the power planes to provide a low resistance vertical path.
- Place power layers next to a ground layer to create planar capacitance, which aids high-frequency decoupling, reduces electromagnetic interference (EMI) radiation, and enhances electromagnetic compliance (EMC) robustness. Because planar capacitance is inversely proportional to the dielectric thickness between the power and ground planes, choose thin dielectrics between the power and ground planes to increase the planar capacitance while reducing planar spreading inductance.

Related Information

AN 910: Intel Agilex 7 Power Distribution Network Design Guidelines

1.3.3. Reference Planes

- Make sure all high-speed signals reference to solid planes over the length of their routing (ground reference is preferred) and do not cross split planes.
- Use a layer topology of ground-signal-ground for high-speed signal routing to provide good isolation and reference.

1.3.4. Layer Assignment

- For high-speed differential traces, avoid long via coupling between the closest transmit (TX) and receive (RX) channels.
- Make sure the via coupling length is as short as possible to reduce crosstalk.
- Use shallow layers for high-speed signals, especially for lanes that support PAM4 modulation.

1.3.5. Impedance

- Strictly control the impedance tolerance of high-speed traces. Generally, 10% can be used for stripline impedance, but 7% is better, especially for the 112G PAM4 signals.
- Breakout routing usually has limited routing space which may cause impedance discontinuity. Optimize breakout routing trace geometries to reduce the impedance discontinuity for better return loss performance.

1.3.6. Via Drill Size

- The aspect ratio (AR) is the ratio of a via length or depth to its drill hole diameter. An AR of 15 is a common manufacturing capability provided by most PCB vendors. PCB vendors define the exact AR based on the board thickness specified by their manufacturing capabilities.
- To meet the target differential via impedance, the optimized anti-pad size is usually larger than the default via anti-pad which may cause a reference issue for breakout routing in the BGA area. Check via impedance with time domain reflectometry (TDR), and use a teardrop or wider trace segment in the breakout area for a smooth impedance transition to the global area.

1.3.7. Fiber Weave

- A composite of fiber and resin make up the PCB material. The strand bundles of fiber run perpendicular to each other. Depending on the orientation of the weave relative to the trace, there can be a resin or a fiber bundle beneath the trace. The differing dielectric constants of these two materials may introduce a phase skew among signals that comprise a differential pair, manifesting itself as an AC common mode noise at the receiver, affecting both the voltage and timing margin at the receiver. This is the fiber weave effect. To mitigate the fiber weave effect, specify a dense spread of weave (1078, 1035, 3313, 1067, etc.) rather than a sparse weave (106, 1080) for prepreg(1) and core.
- Use a 2-ply (1078x2, 1078+1067, 1035x2, etc.) prepreg and core to mitigate the fiber weave effect. Especially for the 112G PAM4 application, it is better to use 2-ply (1035x2, 1078x2, 1035+1078) prepreg and core.
- For more details about the fiber weave effect, refer to *AN 528: PCB Dielectric Material Selection and Fiber Weave Effect on High-Speed Channel Routing*.

Related Information

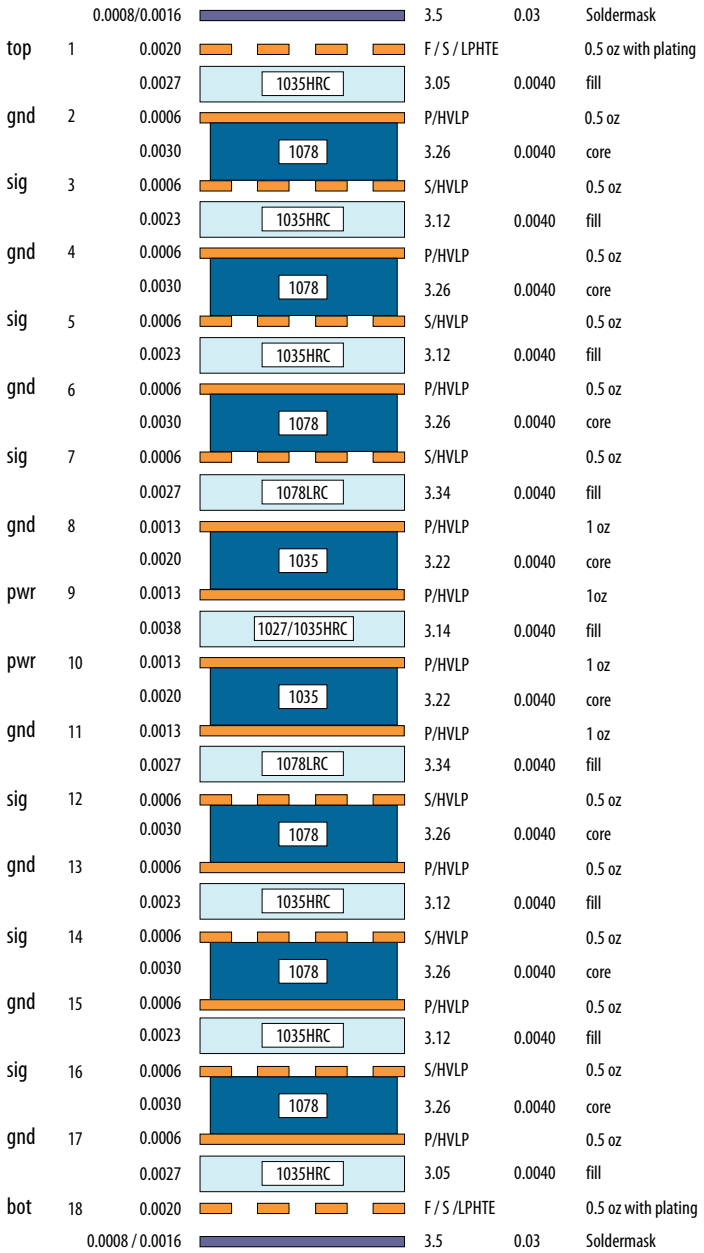
AN 528: PCB Dielectric Material Selection and Fiber Weave Effect on High-Speed Channel Routing

1.3.8. Reference Stackup

The following figure is a PCIe* add-in card reference stackup example. With 18 layers, the total board thickness is 62 mils. It has two 1 oz power layers at the center of the stackup referenced to the two ground layers on each side. The card uses the ground-signal-ground layer pattern for all signal configurations and a dense weave (1078, 1035) prepreg and core for dielectric prepreg and core.

(1) "Prepreg" is an abbreviation of "pre-impregnated material," in this case, referring to the PCB fiberglass impregnated with resin (an epoxy-based material) used in multilayer boards.

Figure 3. 18-layer Add-in Card Reference Stackup



1.4. PCB Design Guidelines

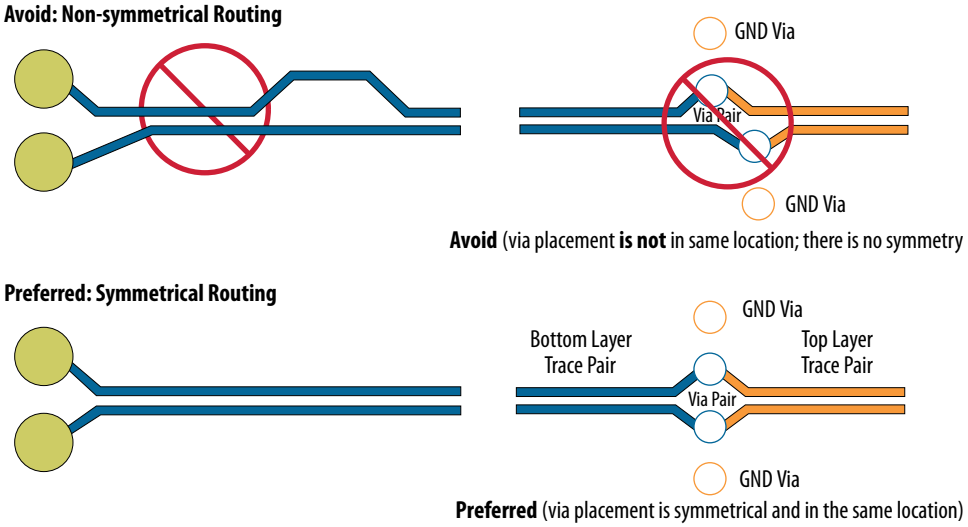
1.4.1. General PCB Design Guidelines

Each component in a high-speed channel can impact the overall system performance. From end-to-end, these components are the device packages, PCB traces, PCB vias, connectors, cables, and landing pads of integrated circuit pins, connector pins, and alternating current (AC) coupling capacitor pins.

1.4.1.1. PCB Traces

- Use stripline routing for better far end crosstalk performance and a tight impedance tolerance, and keep trace lengths shorter than the maximum allowed length limited by the full-channel IL and eye diagram simulation results.
- Follow the general stripline pair-to-pair spacing rule of 5H for TX-to-TX and RX-to-RX, 9H for TX-to-RX, TX-to-others, and RX-to-others, where 'H' is the distance from the signal layer to the closest reference layer.
- Use a solid ground reference for high-speed differential pairs.
- Keep at least 5H of spacing between the edge of a trace and the void and between the edge of a trace and the edge of the reference plane in the open field area.
- Maintain symmetrical routing between two signals that comprise a differential pair from end to end, including the trace length, the transition via location, and the placement of AC coupling capacitors. Failure to maintain routing symmetry introduces differential-to-common-mode or common-to-differential-mode conversion AC noise.

Figure 4. Symmetrical and Non-symmetrical Routing Examples



- Breakout routing usually has a smaller trace width and smaller pair-to-pair spacing, so keep the breakout routing as short as possible to minimize reflection and insertion loss and reduce crosstalk.
- To mitigate near end crosstalk, route the high-speed TX and RX signals on different layers, or separate the TX and RX signals with large spacing of at least 9H in the stripline layer.
- In the BGA pin field via array, avoid high-speed traces routed between two vias that comprise a differential pair via, and make the coupling area between the high-speed trace and via as small as possible. Follow the guidelines in the following figure to minimize crosstalk in the pin field area. Each differential pair has a short bar connecting the P and N in the figure to indicate the differential via.

Figure 5. Routing Rule in Hex Pattern Pin Field Via Array

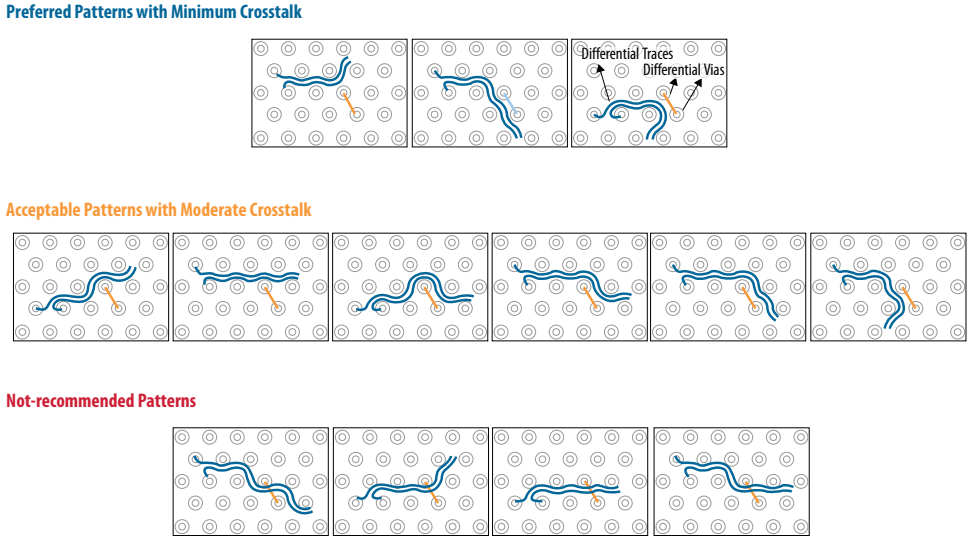
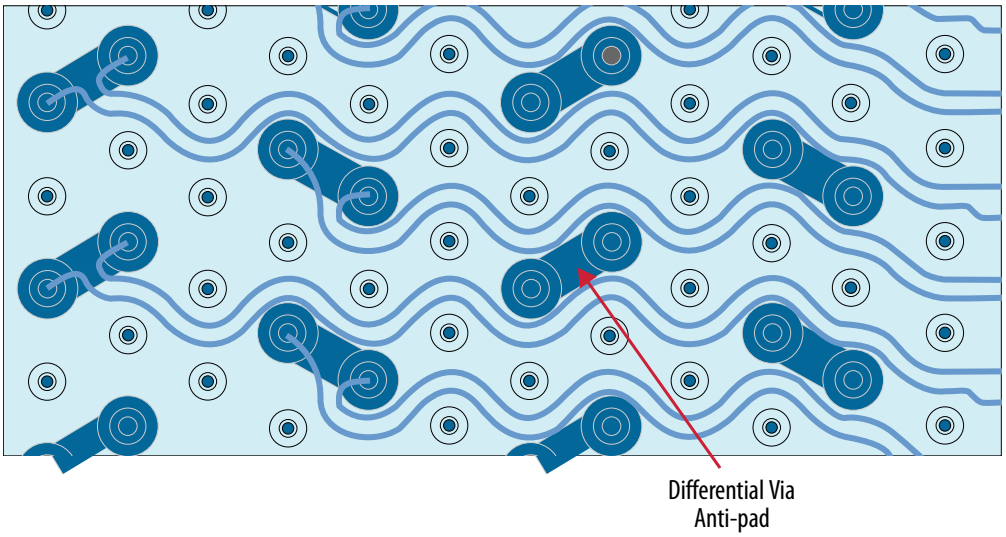
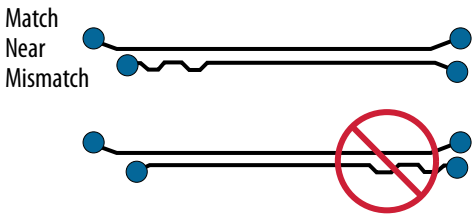


Figure 6. Breakout Routing Example of Hex Pattern BGA



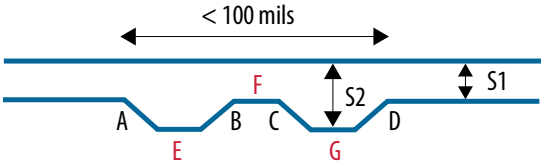
- To increase the common mode noise immunity, start differential pair P/N deskew at the transmitter, end deskew at the receiver, and compensate for the skew after the skew happens and close to the point where the variation occurs.

Figure 7. Intrapair Deskew Close to the Skew Happening Location



- Minimize serpentine layouts, making them transparent to the signal, because serpentine layouts introduce discontinuity to the differential channel. You can minimize them by making electrical lengths shorter than the signal rise time. In general, keep the serpentine routing length <100 mils with arcs and bends of 45 degrees. A loosely coupled differential pair is less affected by serpentine lines.

Figure 8. Deskew Trombone Routing Rule

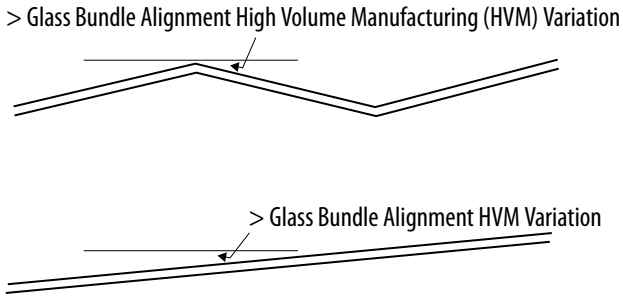


Intra-pair differential skew compensation
Recommended dimensions: A = B = C = D,
E = F = G = 3W (W = trace width) and S2<2S1

- Do not use tightly coupled high-speed differential pairs for a given routing density because they increases the impedance fluctuation caused by the deskew trombone and manufacturing tolerance. The general rule for intra-pair spacing is between one and two times the trace width.
- Use arc routing for high-speed differential traces.
- Use teardrop traces for high-speed differential traces in the pad and via area.
- Mitigate the fiber weave effect with techniques like zig-zag routing and image rotation (see below).

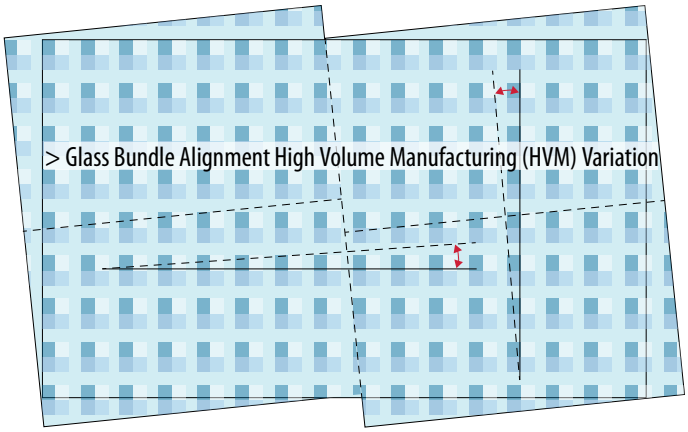
The following figure shows zig-zag routing. If the weave is aligned to the PCB edges, follow a zig-zag routing of differential traces. Generally, maintain a minimum angle of 10 degrees between the trace and fiber weave; thee angles are relative to the PCB edge. For more details about the fiber weave effect, refer to *AN 528: PCB Dielectric Material Selection and Fiber Weave Effect on High-Speed Channel Routing*.

Figure 9. Zig-Zag Routing



Another solution is image rotation that maintains an angle between the trace and the fiber weave pattern. Rotate until the traces are at a 10 degree angle relative to the fiber weave. Rotate by cutting the PCB at an angle, as shown in following figure, or by rotating the layout relative to the edge of the PCB.

Figure 10. Cutting the PCB Board to Rotate the Image Relative to the Fiber Weave Pattern



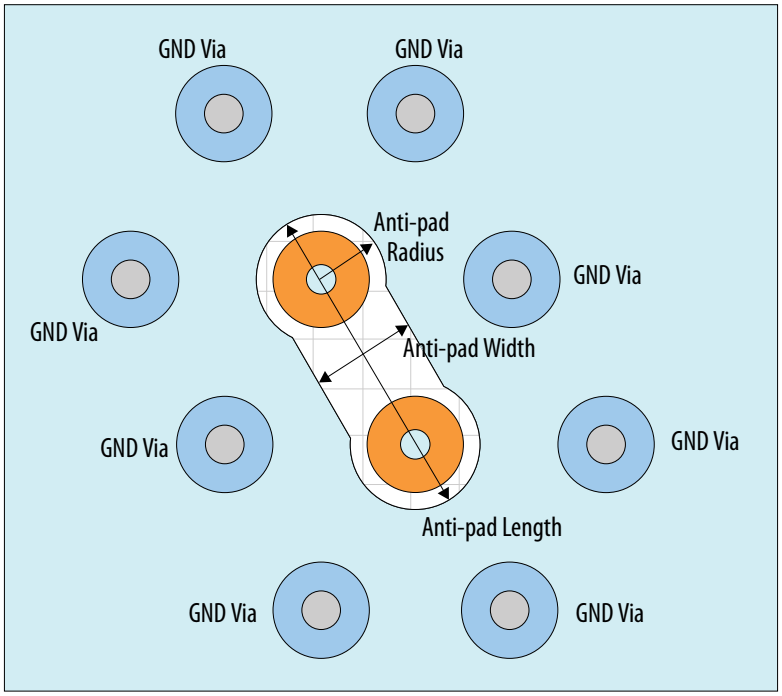
Related Information

AN 528: PCB Dielectric Material Selection and Fiber Weave Effect on High-Speed Channel Routing

1.4.1.2. PCB Vias

- Vias impact high-speed channel loss and the timing budget, so use as few vias as possible for the high-speed differential channel.
- Keep impedance continuity between the high-speed PCB via and trace. Vias usually have higher capacitance and lower impedance than traces.
- Optimize via impedance, using a 3D electromagnetic (EM) field solver, by sweeping the anti-pad width, length, and radius for your specific stackup, drill size, and via stub. Keep in mind that:
  - The smaller the drill size, the higher the via impedance
  - The larger the anti-pad size, the higher the via impedance
  - The shorter the via stub, the higher the via impedance
  - The smaller the via top, bottom, and functional pads, the higher the via impedance

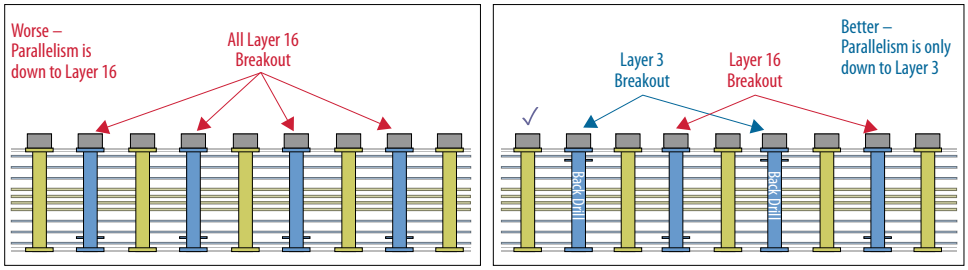
Figure 11. Hex Pattern BGA Via Optimization



Stackup: 22 layers, 2.7 mm thick
Pin pitch: 1 mm
Via drill diameter: 8 mils
Pad diameter: 16 mils
Target impedance: 95 Ω
Reference anti-pad for top to layer 7 via:
Anti-pad width = 24 mils
Anti-pad length = 67.37 mils
Anti-pad radius = 14 mils

- Make sure that each high-speed signal via has a ground via for reference, and make sure that the two signal vias of a differential pair have symmetrical ground vias as the above figure shows. If you do not do this, mode conversion is introduced.
- Remove non-functional pads for high-speed signal vias and ground vias to lower via capacitance.
- Make the closest TX and RX signal via coupling length as short as possible through an appropriate layer assignment.

Figure 12. Via Coupling Reduction by Routing Layer Assignment (18L Example)



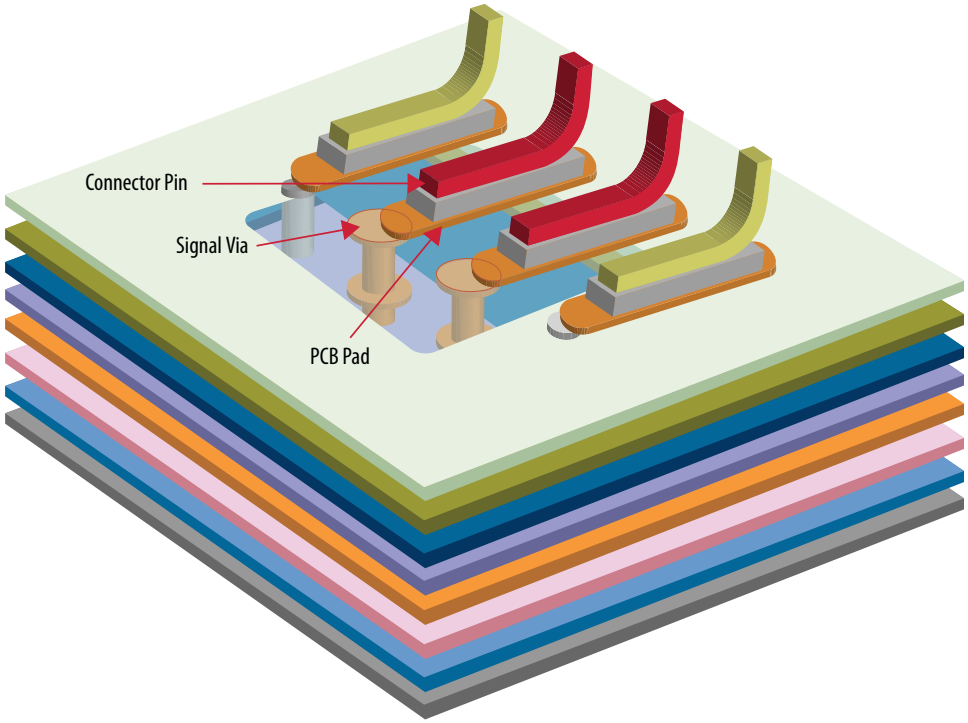
- During insertion loss evaluation, a resonance can occur in the frequency range of three times the Nyquist frequency. Control the via stub length to avoid this resonance.

1.4.1.3. Connector Breakout

For high-speed routing, use the correct breakout orientation to avoid long stubs caused by the connector pin and PCB pad.

Figure 13. Connector Pin and PCB Pad Connection

This is a surface-mount, ground-signal-signal-ground connector pin interconnection with the PCB. The different layers in the stackup are indicated with different colors.



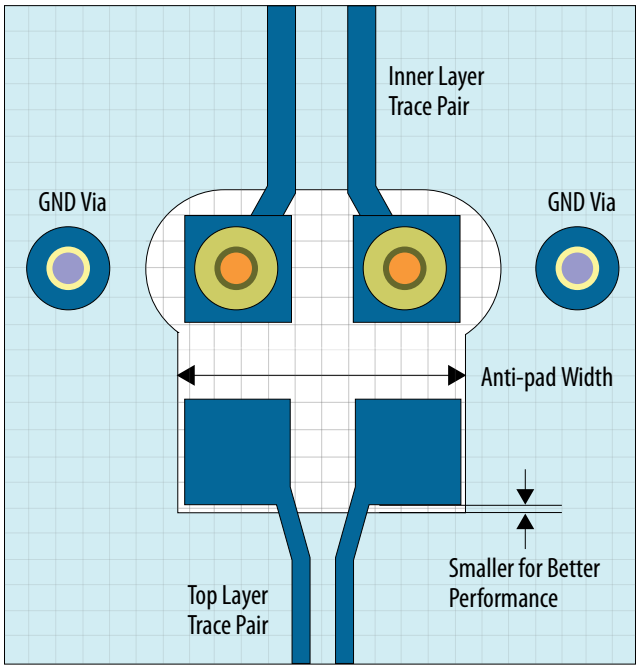
Optimize and tune the connector break-in and breakout to reach the target trace impedance and increase continuity. To accurately capture the interaction between the connector pin and PCB pad, co-simulate the connector-to-PCB interaction with connector structures integrated with the PCB by a 3D EM simulation tool.

1.4.1.4. AC Coupling Capacitor

The layout design of AC coupling capacitors can impact high-speed channel performance.

- Use a 0402 or 0201 size capacitor for a smaller parasitic and smaller footprint.
- Place the AC coupling capacitors at the device end or connector end. Do not place them in the middle of the trace routing.
- Keep the placement of the AC coupling capacitors on the two lines of a differential pair symmetrical, make sure that the fan-in and fan-out routing of the capacitors is symmetric, and make sure the line lengths on both sides of the capacitors are matched.
- Similar to the connector landing pad, optimize the cut-out size under the capacitor pad using a 3D EM simulation tool for your specific stackup and capacitor pad size. Cut the direct, next-layer ground plane of the capacitor pad.

Figure 14. AC Coupling Capacitor Layout



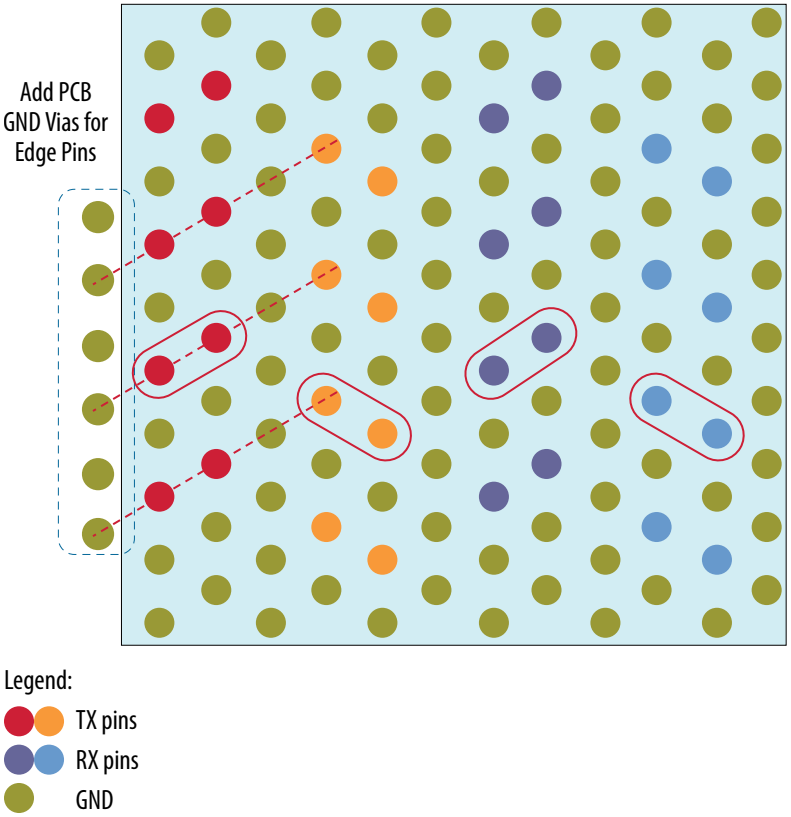
1.4.1.5. Others

- Do not route high-speed differential traces under power connectors, power delivery inductors, other interface connectors, crystals, oscillators, clock synthesizers, magnetic devices, or integrated circuits that use or duplicate clocks.
- Keep large spacing (greater than 100 mils) from high-speed traces, vias, and pads to high-noise power nets. High-noise power nets include nets like the switching node (phase node) of a voltage regulator module (VRM), 12 V power net, and high current transient power net.
- If you use a dog-bone fan-out in the BGA pin area, use a ground reference plane cutout under the high-speed signal pad to reduce the capacitance.

1.4.2. E-Tile PCB Design Guidelines

- Use a trace impedance of 90-100 Ω for differential signals. The nominal package impedance of the Intel Agilex 7 FPGA interface is 90 Ω.
- Route lanes that support 56G PAM4 on shallow layers to reduce via length, with connectors placed on the PCB close to the FPGA to reduce the trace length.
- Make via stubs as short as possible. Use top-drill, back-drill, buried via, blind via, and micro-via techniques as necessary to shorten the via stubs. Stub lengths of less than 10 mils are recommended.
- Use layer assignment to keep the coupling length of the closest TX and RX vias as short as possible. A coupling length including via stubs of less than 56 mils is recommended.
- Use additional ground reference vias for the package edge differential pairs in order to keep ground reference via symmetry for the two signal vias that comprise a differential pair.

Figure 15. Adding Reference Ground Vias for Package Edge Vias



- Make sure that QSFP-DD connector high-speed signal pin breakouts are on the side that faces toward the FPGA rather than the side that faces the board edge to avoid the long stub caused by the connector pin and PCB pad. For the QSFP-DD connector and PCB pad connection, refer to the following figures.

Figure 16. QSFP-DD Connector and PCB Connection

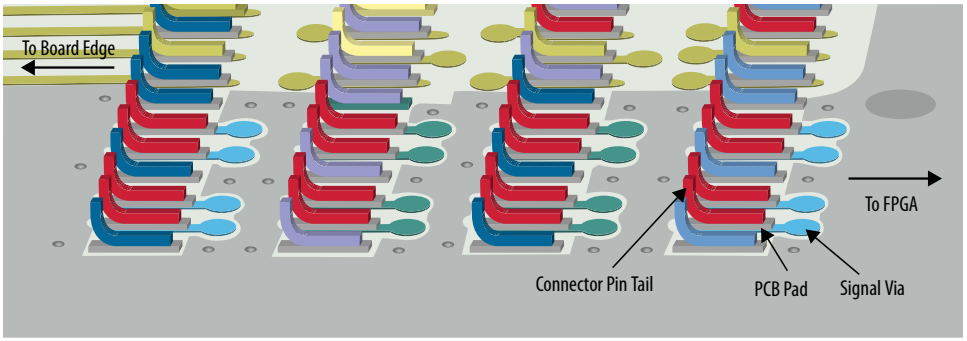
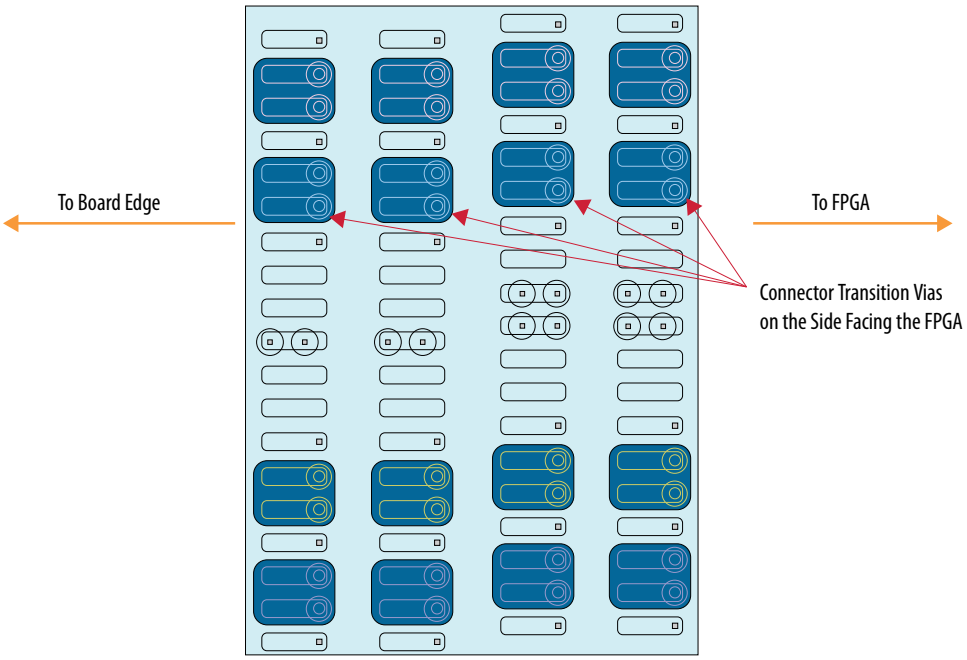


Figure 17. QSFP-DD Transition Via Layout



- The zQSFP+ connector has a different connection compared to a QSFP-DD connector as shown in the following figures. Keep the breakouts and the transition vias at the periphery of the zQSFP+ connectors.

Figure 18. zQSFP+ Connector and PCB Connection

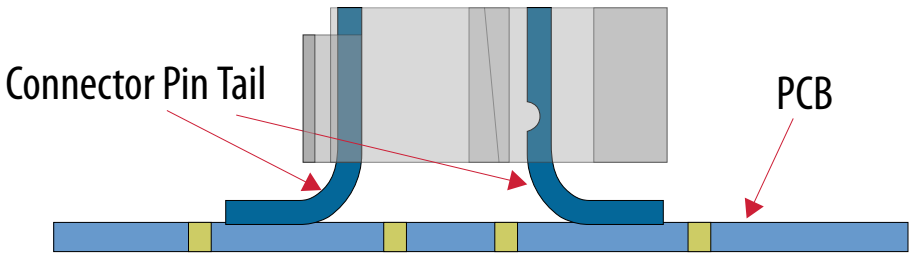
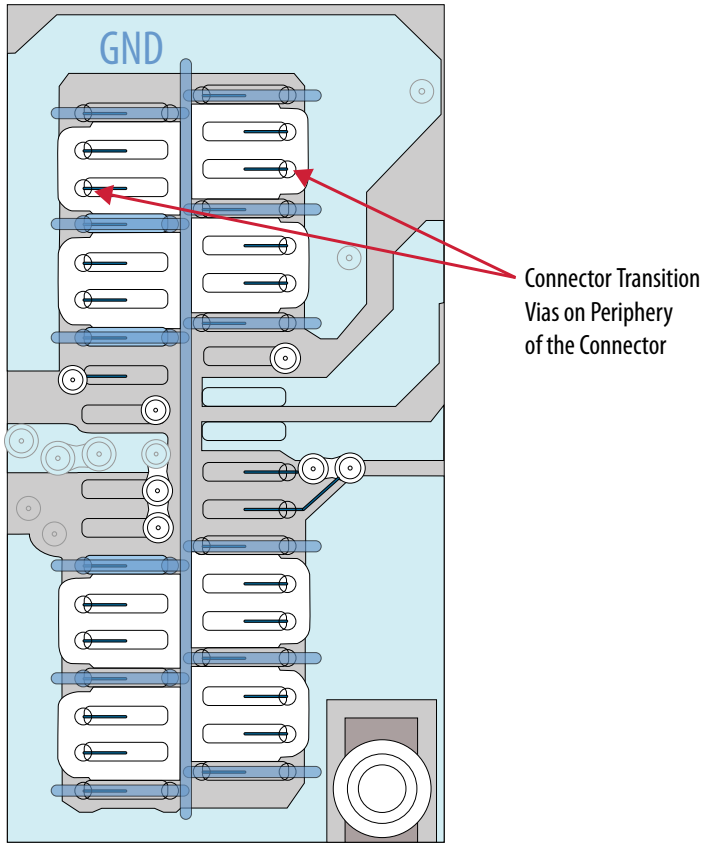
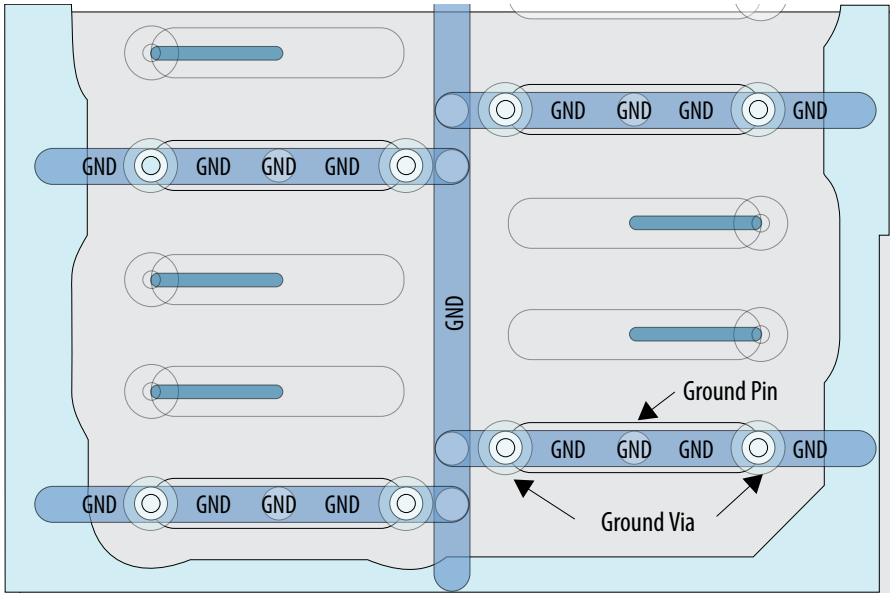


Figure 19. zQSFP+ Transition Via Layout



- Add ground vias on both sides of the connector ground pin and connect them with short, thick ground trace to minimize the inductance of the ground connection. Keep the connector ground pins locally shorted to maintain an equal potential.

Figure 20. zQSFP+ Connector Ground Pin Layout



1.4.3. F-Tile PCB Design Guidelines

For F-tile transceivers, the highest data rate and most challenging protocol is 400G Ethernet application (defined by CEI-112G-VSR/MR/LR or IEEE 802.3ck specification) with a data rate of up to 116G PAM4. This topic focuses on this application. For other applications with lower data rates, refer to the E-tile and P-tile design guidelines.

To design a 400G application interface on a CEI-112G compliant board, the typical design flow is:

- Optimize the passive channel
- COM simulation
- Simulate the active channel

1.4.3.1. F-Tile Features and Capabilities

The Intel Agilex 7 F-tile transceivers are general purpose transceivers..

The F-tile transceivers have the following two usage modes:

- 4 channels up to 112G PAM4 + 12 channels up to 58G PAM4
- 4 channels up to 112G PAM4 + 16 channels up to 32G NRZ

They have multiprotocol support for:

- CEI
- Ethernet
- CPRI
- FlexE
- 300G Interlaken

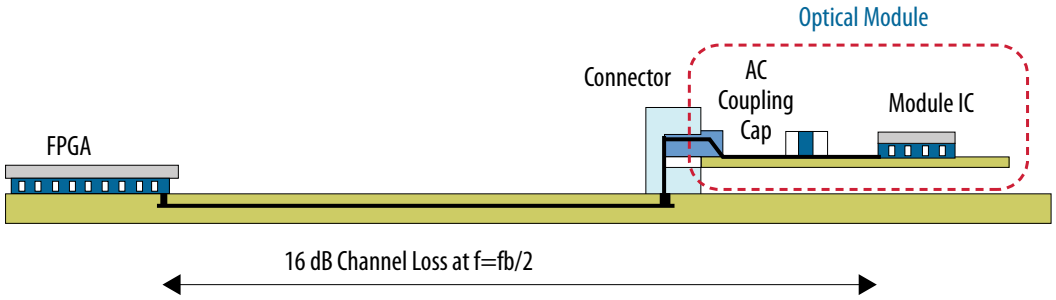
- Fibre Channel
- SRIO
- SerialLite IV
- OTN
- JESD204B/C
- FlexO
- IEEE1588
- GPON
- SDI
- Vby1
- HDMI
- Display Port.

In addition, F-tile transceivers support PCIe Gen4 x16 with the P-Tile features, precise time management, and PMA direct mode.

1.4.3.2. Optimizing the Passive Channel

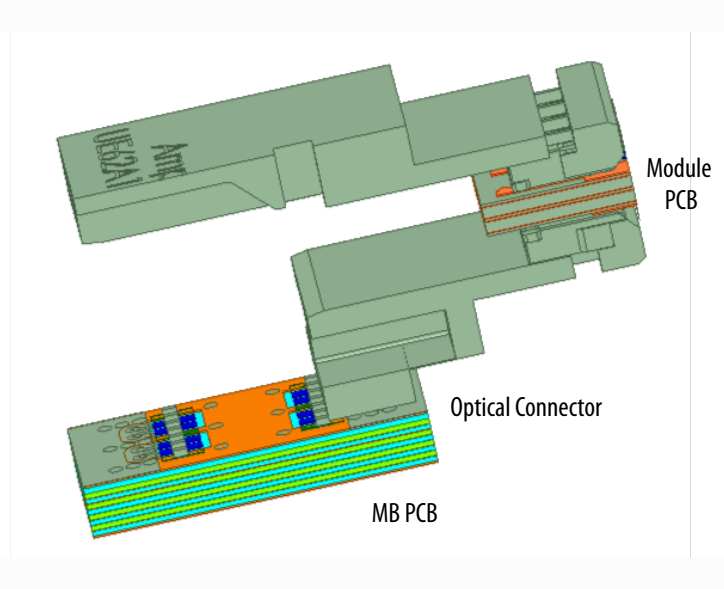
You should optimize the whole channel from FPGA BGA pad to module IC pad. You only need to focus optimizing the channel on the PCB, from FPGA BGA pad to optical connector footprint because the optical module is already optimized according to the vendor protocol specification. Refer to the *General PCB Design Guidelines* for general recommendations on how to optimize PCB channel. You can start board design with Intel FPGA development kits.Refer to *All Development Kits*.

Figure 21. Typical CEI-112G-VSR channel



1. Use 3D EM tools for via structure optimization, including FPGA BGA breakout via and optical connector fan out via.
2. Include connector 3D model for connector fan out via optimization, connector vendor typically can provide encrypted 3D model for connector and PCB joint simulation.

Figure 22. Connectors



3. Include crosstalk effects for all components in the simulation (FPGA BGA vias, traces, connector fan out vias)
4. After you finish the optimization for each element of the channel, cascade them to build a passive channel (from ball to ball) to get channel performance, typically in S parameter format.
5. Produce traditional channel performance plots like insertion loss, return loss, crosstalk and mode conversion from the channel S parameter to understand the channel performance.
6. Further optimize it if you find any defects.

Related Information

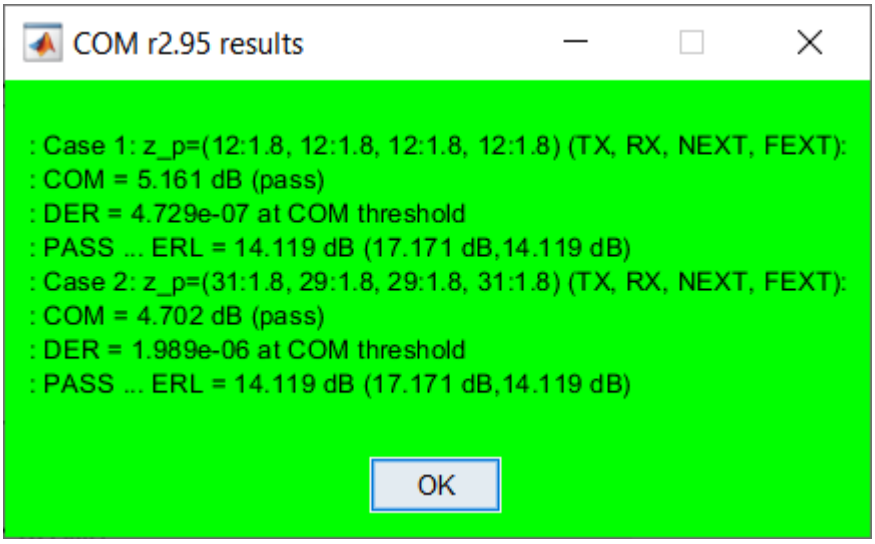
All Development Kits

1.4.3.3. COM Simulations

Channel operating margin (COM) is a standardized method of determining the overall figure of merit of a channel. Some of the traditional channel parameters like IL, RL, ICN/ICR(integrated crosstalk noise/ratio) are informative only. COM is a single value in dB derived using the MATLAB code.

The COM calculation code is a built-in feature for most of the commercial channel simulation tools. You can run and get the results directly from these tools. Refer to the *IEEE 802.3* website to get the latest COM code and configuration file. The configuration file is different for different applications (VSR, MR, LR). Read through protocol spec to get the most suitable one based on the target application.

Figure 23. Example COM Simulation Results



Typically, COM simulation needs to run two cases: a long package case and a short package case, which represent the worst-case package parameters defined in the protocol specification for TX and RX devices. You can also use the device package model to replace these predefined parameters for more accurate results. COM simulation can report channel COM and ERL (effective return loss, refer to 802.3 spec for details) data in dB. You need to compare it with the mask defined in the protocol specification. Different applications define different masks, typically 3dB for COM and 10dB for ERL. Passing these specifications means the designed channel is protocol compliant, and the larger the data values, the more margin the channel has. Intel strongly suggest you run COM simulation to make sure the designed board channel can meet the protocol specification. Optimize the channel and calculate the channel design margin based on COM and ERL results.

Related Information

IEEE 802.3

1.4.3.4. Simulating the Active Channel

Passive channel simulation checks most board designs. However, Intel suggests performing active channel simulation (eye diagram simulation with IBIS-AMI model) to further capture the channel behavior with TX and RX devices.

1. Contact Intel for the F-tile IBIS-AMI model and user guide.
2. Cascade the IBIS-AMI model with the optimized passive channel model in channel simulation tools.
3. Tune the TX PMA parameter (**auto adaption for RX**).
4. Run channel simulations to get the optimized eye diagram.

   Typically, any non-zero open eye means the channel can work, but you should optimize the TX PMA setting for the best eye opening at the target BER level, to get the best design margin.

1.4.4. P-Tile PCB Design Guidelines

- For PCIe add-in-card designs, the insertion loss from the top of the edge finger to the silicon pad (including the package insertion loss and the silicon loss) for both the receiver and transmitter paths must not exceed 8 dB at 8 GHz. Because the P-tile package plus silicon loss is under 3 dB at 8GHZ, you may have an add-in-card PCB loss under 5 dB at 8GHZ.
- Use an insertion loss of 28 dB at 8GHZ including the transmitter and receiver packages as the reference maximum loss for end-to-end channel design, but validate the final design through complete channel simulation and measurements.
- Use a trace impedance of 85 Ω for P-tile differential channels.
- Make via stubs as short as possible. Use top-drill, back-drill, buried via, blind via, and micro-via techniques as necessary to shorten the via stubs. Stub lengths of less than 30 mils are recommended.
- Use additional ground reference vias for the package edge differential pairs in order to keep ground reference via symmetry for the two signal vias that comprise a differential pair.
- Place the AC coupling capacitors on FPGA TX paths close to the FPGA or connector. Do not place them in the middle of the trace routing.
- Optimize the PCIe slot connector footprint by cutting the ground planes beneath the connector PCB pad, considering the interaction of the connector pin and PCB pad, for less return loss.
- Ensure that the PCIe slot connector high-speed signal pin breakout is at the periphery of the connector as shown below to avoid a long stub caused by the connector pin and PCB pad.

Figure 24. PCIe Slot Connector and PCB Pad Connection

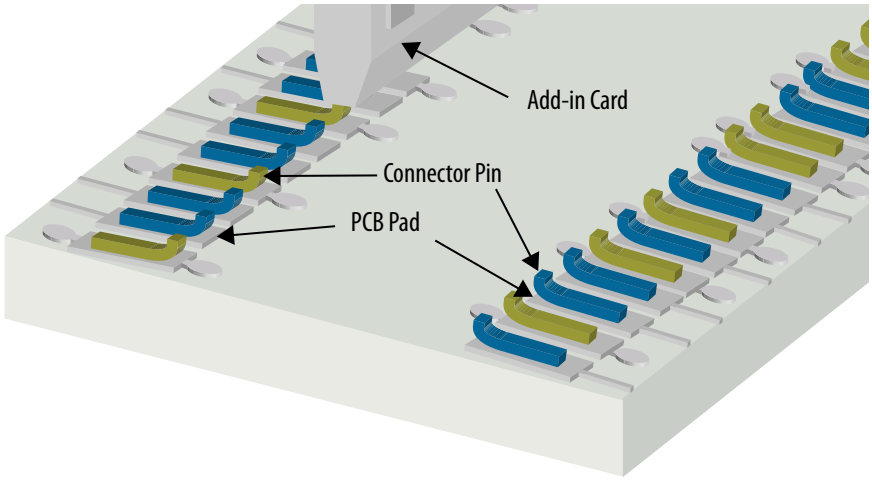
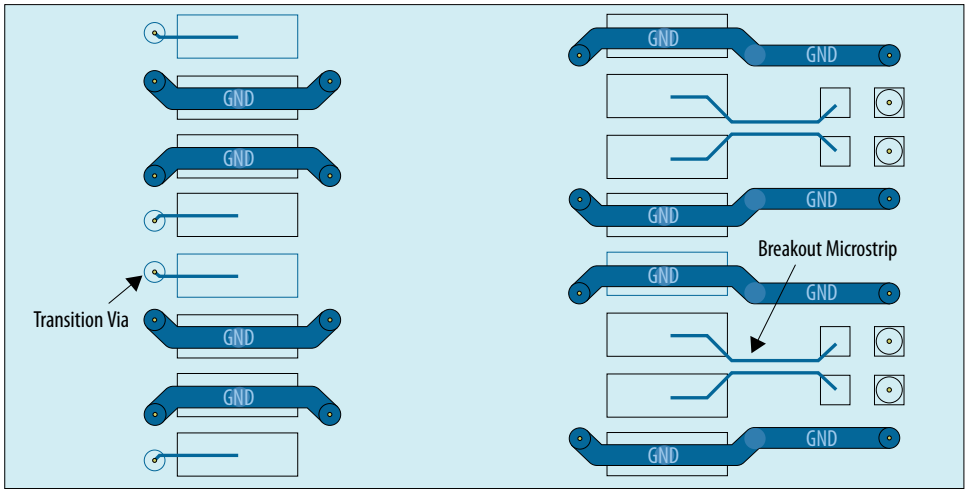
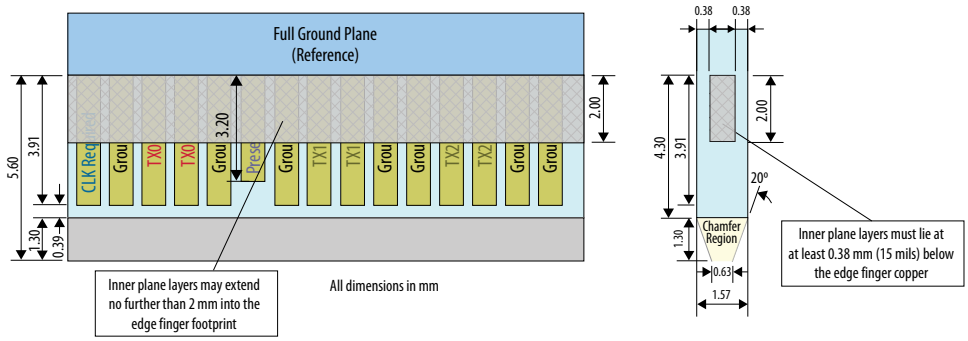


Figure 25. PCIe Slot Connector Breakout



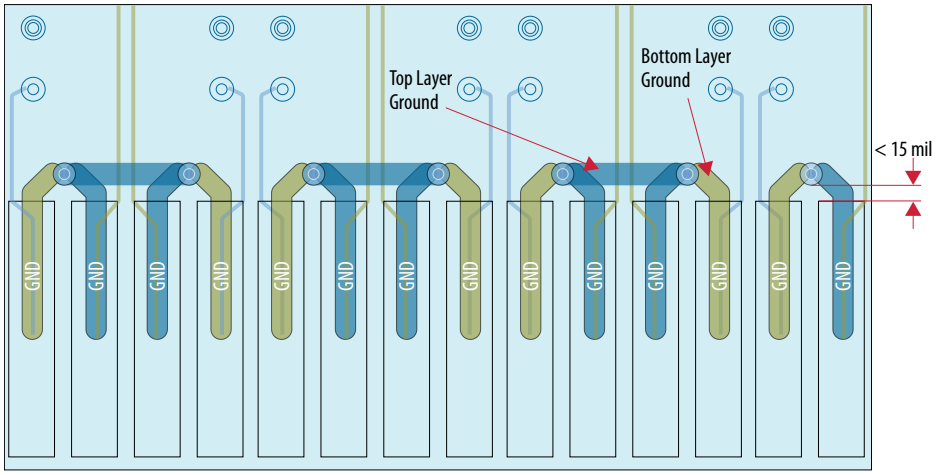
- For an add-in card that supports PCIe Gen4 16.0 GT/s, make sure that there are no inner-layer conductors of any kind, including ground or power planes, beneath the edge-fingers (for a distance of 15 mils). You may add inner plane layers beneath any of the edge fingers if they extend no more than 2 mm into the edge finger region from the main routing area of the board and are at a depth of at least 15 mils (0.38 mm) beneath the edge finger copper pads on the surface of the PCB.

Figure 26. Add-in Card Edge-finger Regions with Allowed Inner Layer Plane Volume Indicated



- For add-in-card ground fingers, make sure that the distance between a horizontal line across the top edge ground fingers and a horizontal line across the bottom edge of the ground via pads does not exceed 15 mils. Also join the adjacent ground edge-fingers at the lowered via location to provide additional improvement in the ground resonance.

Figure 27. Add-in-card Ground Finger Layout



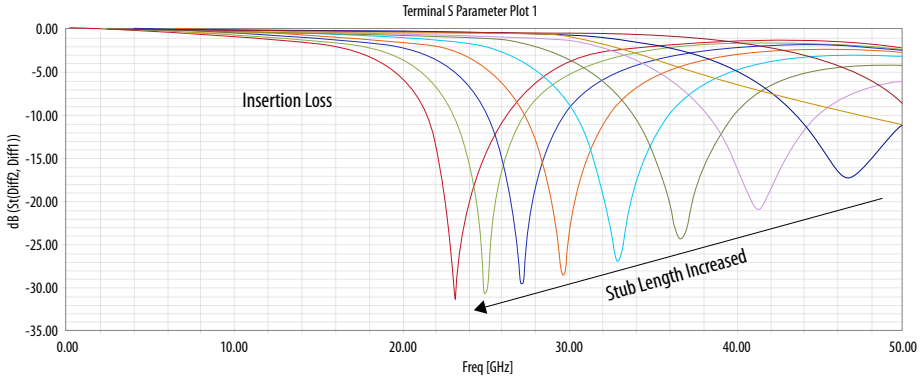
1.4.5. R-Tile PCB Guidelines

R-Tile is PCIe Gen5 transceiver tile.

All the P-tile guidelines apply to R-tile devices. Additionally, the following guidelines are for R-tile devices running at 32 Gbps data rate:

- Intel guarantees the insertion loss of the FPGA package plus the silicon does not exceed 4.0dB at 16 GHz.
- Ensure the R-tile high speed signal (HSSI) via stub is as short as possible through back-drill or micro via techniques. Intel recommends a stub length smaller than 10 mils. Long via stubs reduce the via impedance and produce resonances at low frequencies that worsen the channel insertion loss and return loss.

Figure 28. Insertion loss curve of a differential via pair with different via stub length

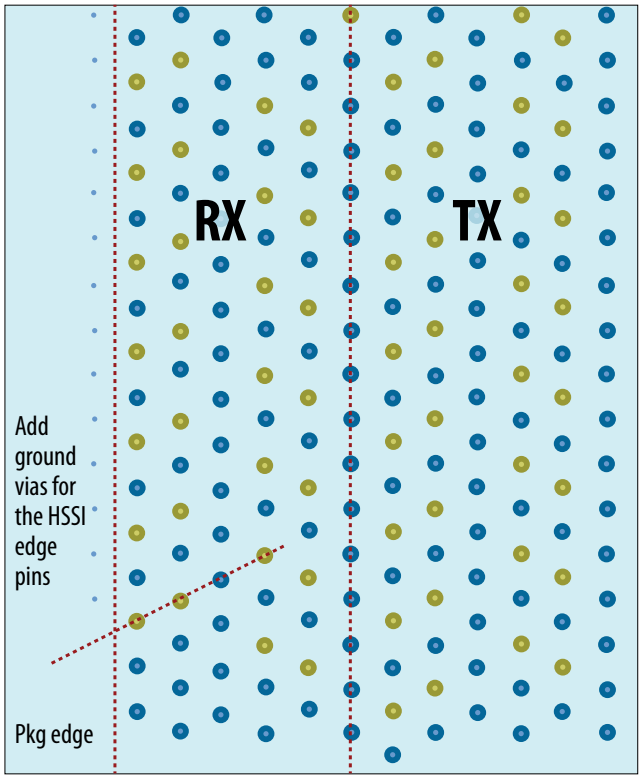


- Use a short coupling length between HSSI vias, where the via stub is part of via length.

- Assigning suitable routing layers to high speed Tx and Rx signals obtain better Rx performance and less crosstalk between Tx breakout traces and Rx vias after implementing back-drilling or micro via techniques.

Figure 29. R-tile Hex Pin Pattern

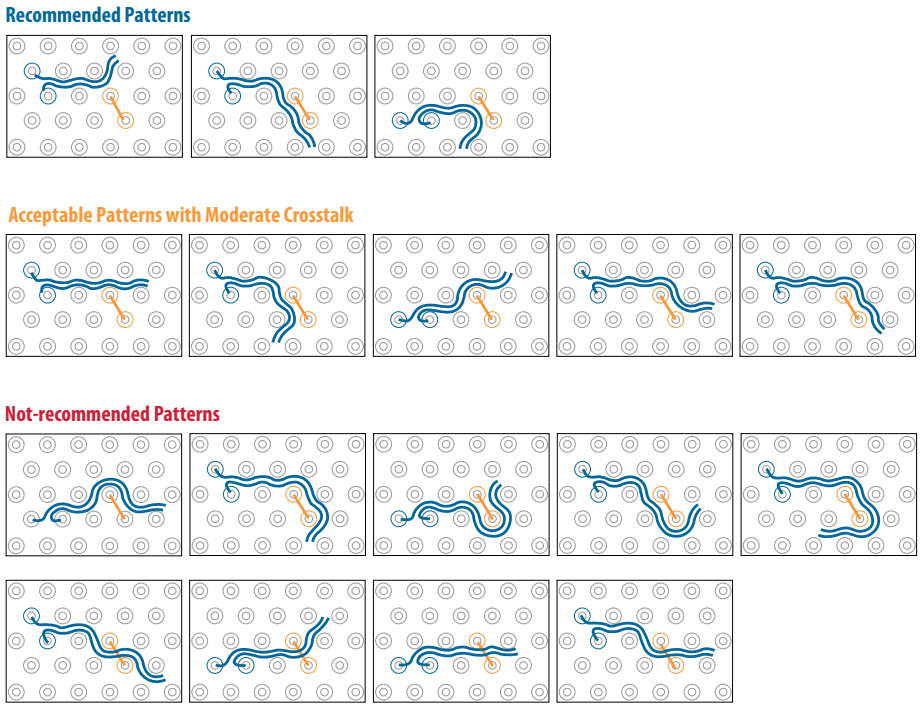
Blue represents the GND, green represents R-tile HSSI Differential Pairs



- Improve the HSSI TX and RX breakout routing in the pin field area. This routing strategy reduces breakout area signal trace to via coupling. The larger distance between breakout trace and adjacent signal vias, the smaller crosstalk; the smaller the coupling area between breakout trace and adjacent signal vias, the smaller the crosstalk.

Figure 30. Recommended Patterns

The figure shows the examples of recommended breakout pattern to minimize the trace to via coupling. Each differential via pair has a short bar connecting the P and N together just for indicating the differential via.



- Optimize the breakout trace width and space based on the PCB manufacturing capabilities in BGA via field to keep the impedance matching with the main routing is recommended.
- Use small package AC coupling capacitors to minimize the impedance discontinuity, e.g. 0201(inch). Ensure the capacitor landing pad is as small as possible as per the DFM requirements. Optimize the cut-out underneath the capacitor pads to improve the channel impedance continuity.
- Ensure a tight trace impedance control, e,g, 5% or 7% depending on the specific PCB.
- Keep the number of transition vias in the HSSI channel as few as possible. Layer transition vias in the HSSI channel typically reduce electrical performance. For example, only add vias at BGA pin, AC cap (only exist on the FPGA transmit channels), and connector pins.

1.4.5.1. R-Tiles Features and Capabilities

R-tile devices support 16 channels of SERDES hard IP, running up to 32Gbps NRZ. The PHY supports the channels according to the specification definition of each protocol. R-tile devices support a maximum end-to-end channel loss of 36dB at 16 GHz with BER of 1E-12 for NRZ signaling. This 36dB includes package and silicon losses. For add-in

card applications, the maximum insertion loss is 9.5dB at 16 GHz on add-in cards. This loss is from the top of the edge finger to the silicon die pad based on the PCIe CEM5.0 spec. This 9.5dB includes PCB traces, vias, AC caps, and package including the effective die capacitance. Intel recommends running the end-to-end channel passive characteristics simulation, e.g. insertion loss (IL), return loss (RL), and crosstalk simulation, especially if the channel IL is high.

The channel passive characteristics simulation allows for quick risk evaluation at the initial stage of the board and system design. Finally, perform the complete post layout channel timing closure simulation and measurements while considering all impairments, e.g. the crosstalk and manufacturing tolerance.

1.4.5.2. R-Tile Design Layout Examples

The design examples are from the Intel Agilex 7 PCIe development board, which has 22 layers and is 2.8mm thick with M7N PCB material.

1.4.5.3. Landing Pad Cut-out Optimization of AC Coupling Capacitor

The simulation uses pad size of 0201 capacitor and the PCIe development board stack-up.

The simulation parameters are:

- Capacitor landing pad size: 12x13 mil rectangle
- Capacitor interpair pin pitch: 26 mil
- Signal micro-via drill and pad diameter: 10 mil and 16 mil
- Signal via depth: top to layer3

Figure 31. Capacitor pad size and the Cut-out Optimization results

Avoid signals routed underneath the capacitor cut-out. Optimize the cut-out size based on the specific stack-up, the capacitor pad size, and the placement through 3D simulation.

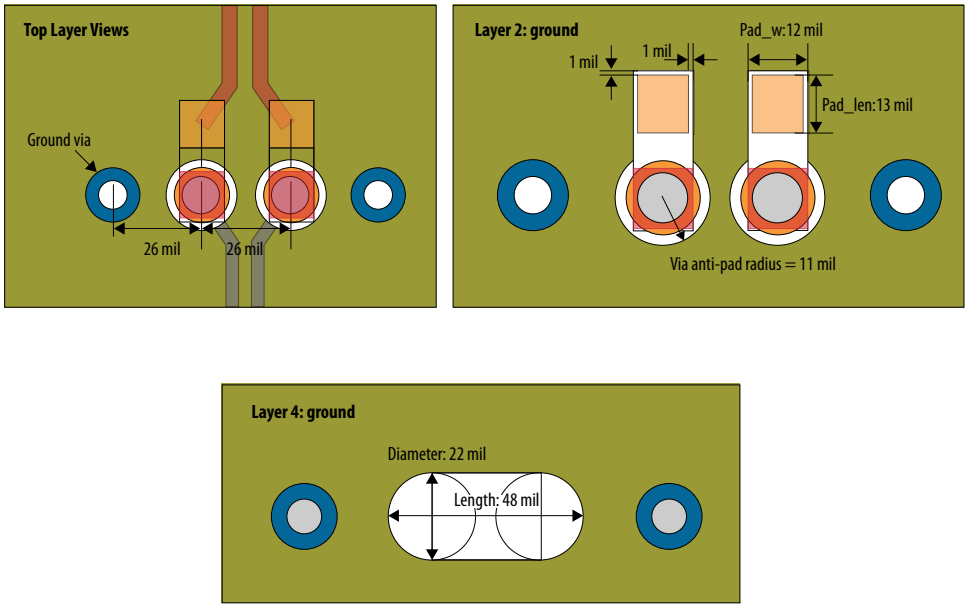
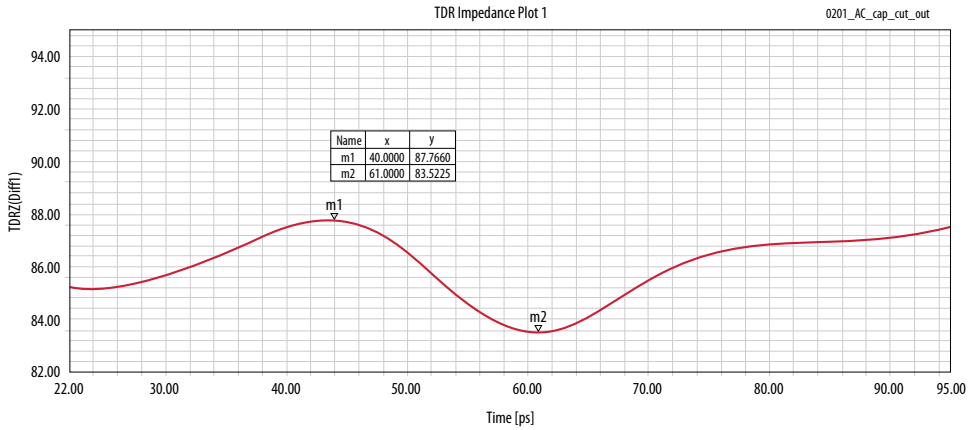


Figure 32. TDR simulation result of 0201 capacitor cut-out



1.4.5.4. R-tile HSSI Breakout Routing in BGA Field Area and MCIO connector Pin Area

This design example on the PCIe development board uses the breakout trace width and space of 3.35mil and 4.65mil. The TX routes on layer3 and RX routes on layer16 because of the pin definition of the Mini Cool Edge IO (MCIO) connector (the PCIe channels connect FPGA and MCIO connector). The connector TX pins are located at the side near FPGA. The RX pins are located at the opposite side to the FPGA. The RX traces route underneath the MCIO connector pin cut-out if RX traces route on layer3.

Figure 33. MCIO Connector Fan-out Design Example

Red represents TX on layer3, yellow represents RX on layer16, blue represents GND. Includes two vias per ground pin to reduce the ground parasitic effect. Route the micro-strip trace length on the top and bottom as short as possible.

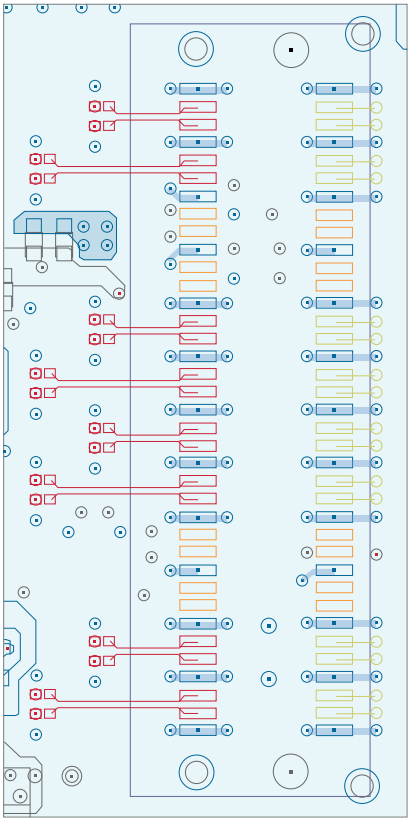


Figure 34. R-tile Breakout Routing Example in BGA Pin Field Area

Dark blue represents TX on layer3 (by micro via, top to layer3), red represents RX on layer16 (by through hole via, top to layer16), blue represents GND.

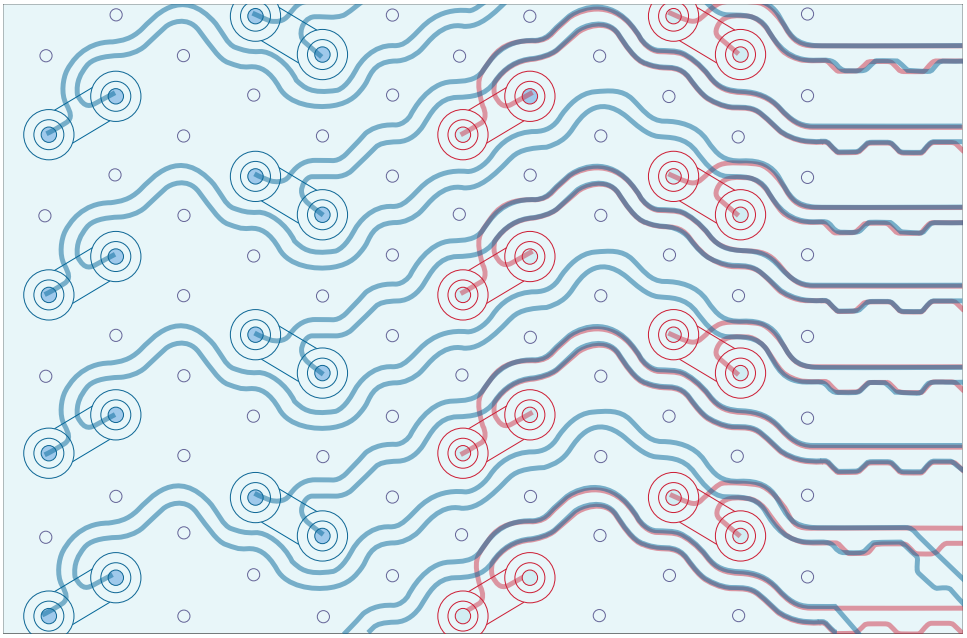
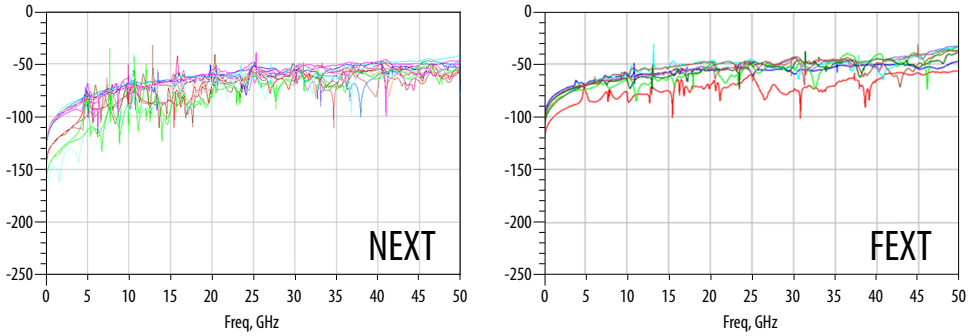


Figure 35. R-tile Breakout Routing Crosstalk Simulation Results

The figures show four TX pairs and four RX pairs. The simulation includes FPGA BGA ball, BGA via, breakout trace, and part of main routing. The simulation results show the near end crosstalk (NEXT) is less than -60.0dB up to 16.0 GHz, the far end crosstalk (FEXT) is less than -50.0dB up to 16.0 GHz.



1.4.5.5. AC Coupling Capacitor Placement Around MCIO Connector

Intel recommends staggered placement for AC coupling capacitors for ease of routing and crosstalk control. Ensure the top layer microstrip trace length from AC coupling capacitor to MCIO connector pin is as short as practical per DFM requirements. Optimize the open field PCB layout to improve the NEXT and FEXT.

Figure 36. AC Coupling Capacitor Staggered Placement Around the MCIO Connector

This example shows the crosstalk simulation results based on the Intel Agilex 7 F-Series FPGA Development Board. Red represents TX on layer7, yellow represents RX on layer5, blue represents GND.

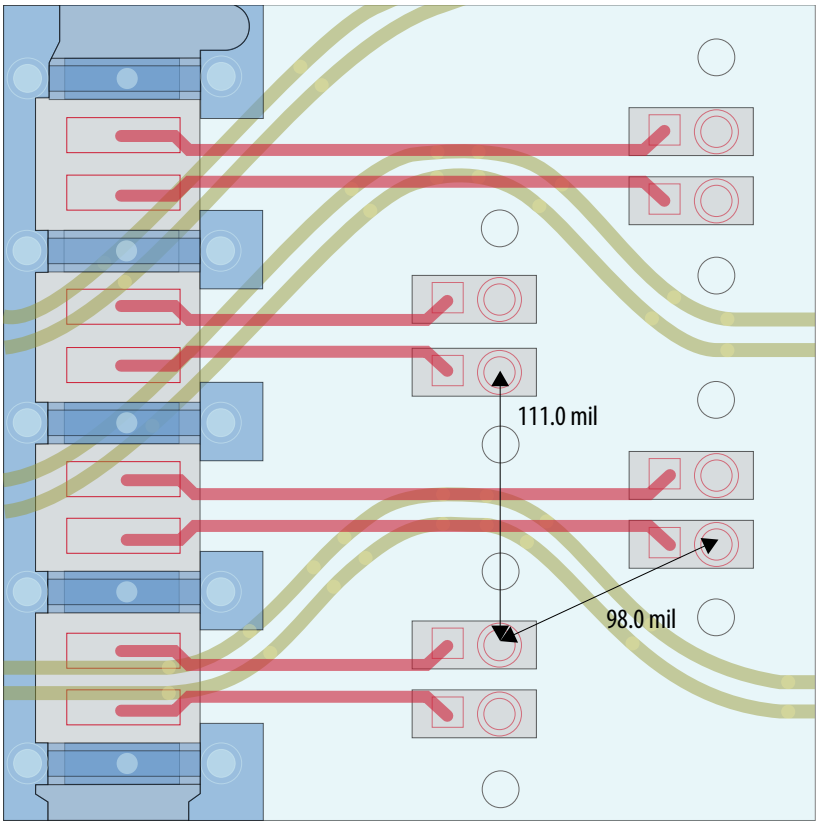
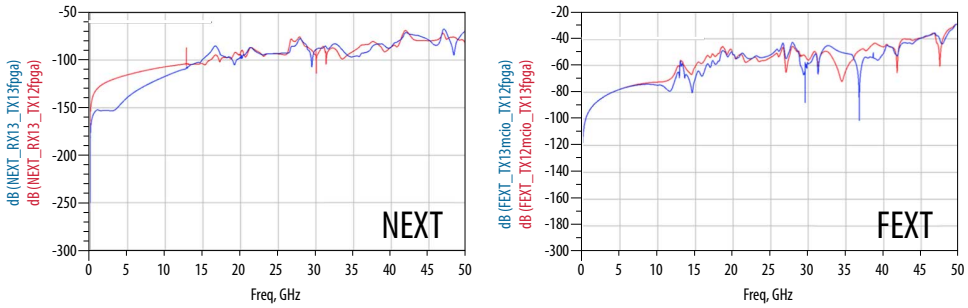


Figure 37. Simulation Results

The figures show two TX pairs and one RX pair. The simulation includes an AC coupling capacitor, via, part of the microstrip trace and part of the strip-line trace. The simulation results show the NEXT is less than -60.0dB up to 16.0 GHz; the FEXT is less than -50.0dB up to 16.0 GHz.



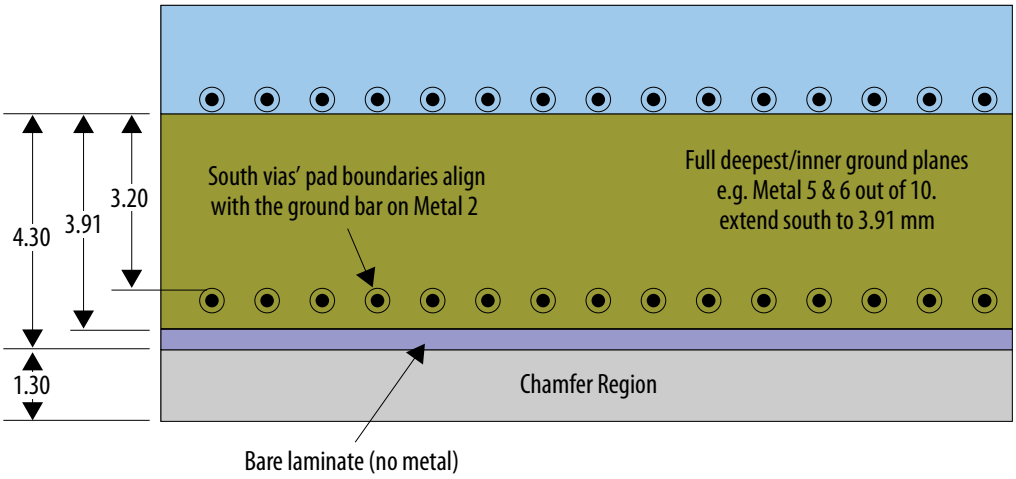
1.4.5.6. PCIe Gen5 Add-in Card Edge Finger Breakout Design Guidelines

Intel implements the following guidelines from the PCIe CEM 5.0 specification version 0.7 in the PCIe development board. For edge finger design, follow the PCIe CEM 5.0 specification.

Ensure inner layer ground under edge-fingers in the high-speed region comprising pins A12/B12 and beyond. The inner layer ground plane must extend to cover the full length of the edge finger region from the main routing area of the board. The inner layer ground plane must lie at least 0.52 mm (20.5 mil) below the edge finger copper. This requirement applies to both sides of the add-in card, so a symmetric pair of shielding planes is used.

Figure 38. Detail of the Core Shielding Ground Plane beneath the Add-in Card Edge Fingers

The figure shows a portion of the N-1 plane for reference

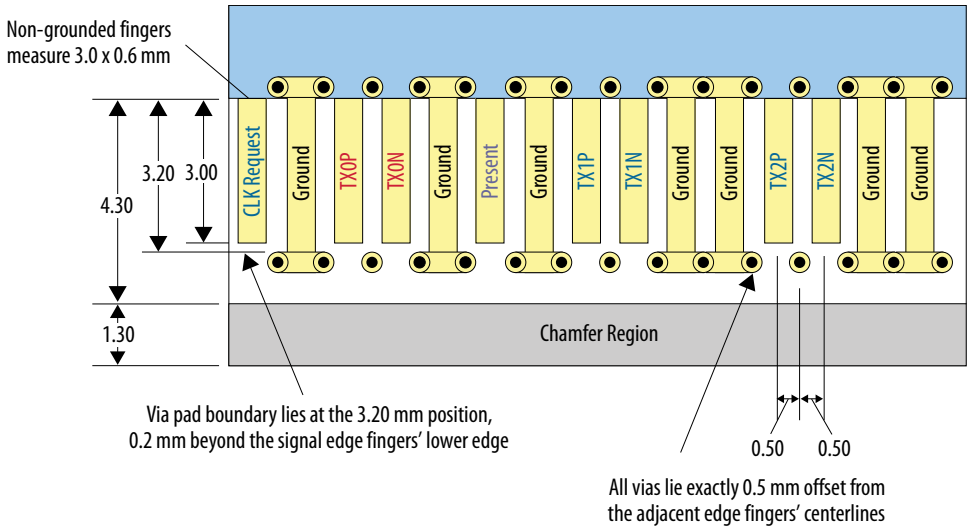


Connect a row of plated vias to the inner layer ground plane along the bottom of the edge fingers in the high-speed region comprising pins A12/B12 and beyond. These vias are known as fingertip south vias. The vias must be plated through holes (PTH). You can share them among ground pads on both surfaces of the add-in card. The upper boundary of the via pad must align with the 3.20 mm dimension. Join ground vias in the "I bar" with surface metal.

Align add-in card ground vias serving the north edge-finger ground conductors with the gap between adjacent edge-fingers, to reduce obstruction to signals routed from non-ground edge fingers. The axes of the north ground vias must be no more than 0.38 mm (15 mil) from the boundary of the edge finger pin field. Connect the edge fingers to the ground via with a length of trace whose width matches or exceeds the via pad diameter to minimize the inductance of the ground connection.

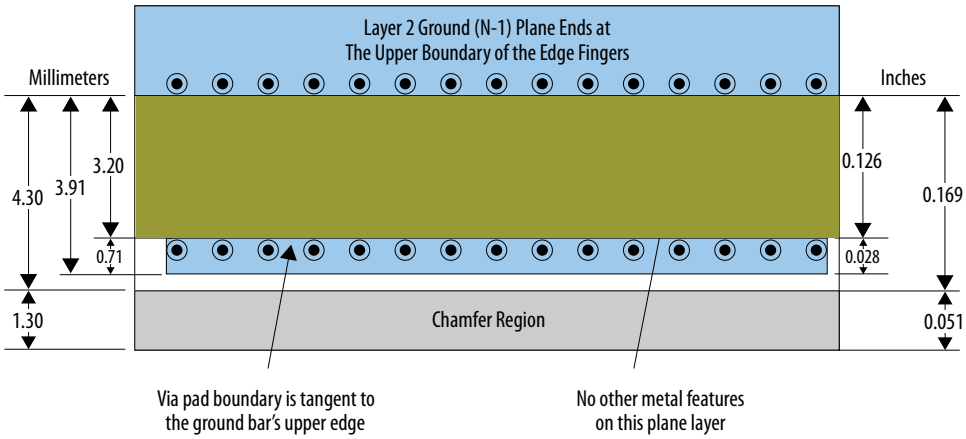
Figure 39. Add-in Card Edge Finger Region

The figure shows south and north edge ground vias. The figure shows a portion of the N-1 plane (e.g. metal 2) for reference



Implement a lateral ground bar to join all the fingertip south vias on the first inner layer (N-1) on each side of the board (Metal 2, for example). The ground bar must align with the north edge of the vias with a distance of 3.20 mm. The ground bar should be 0.71 mm wide, to ensure adequate clearance from the chamfer region.

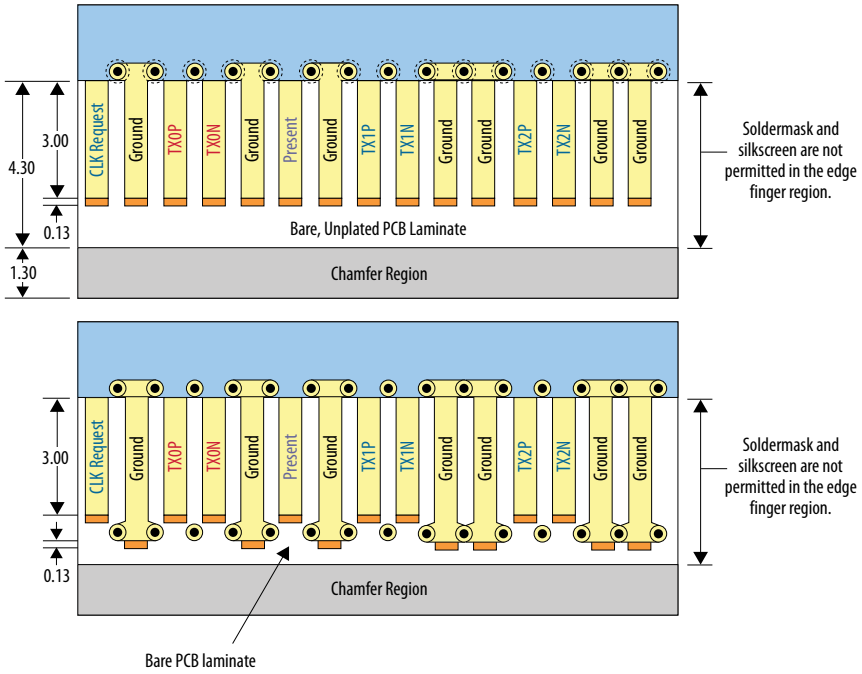
Figure 40. Detail of the N-1 Layer Geometry Highlighting the Lateral South Ground Bar



Ensure the edge-fingers that are not assigned to ground in the region A12/B12 and beyond are 3.00 mm long and 0.60 mm wide (±0.038mm) (refer to *Add-in-Card Edge Fingers Indicating Edge Finger Length*). Ensure the upper of the edge-finger is 5.60 mm above the south edge of the add-in card (refer to *Add-in-Card Edge Fingers Indicating Edge Finger Length*). Small amounts of residual surface metal are permitted in the region extending 0.13 mm beyond the lower end of the edge finger.

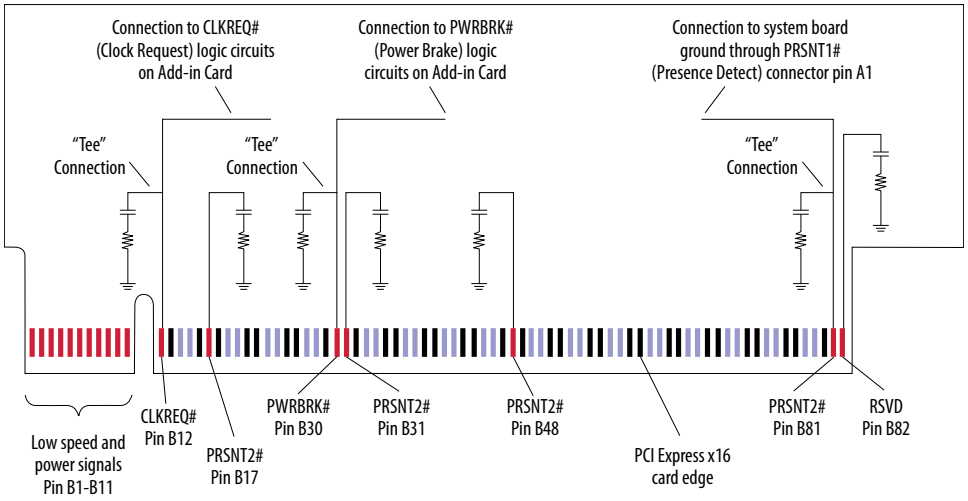
Figure 41. Add-in-Card Edge Fingers Indicating Edge Finger Length

The figure shows a portion of the N-1 plane for reference



Ensure the trace length from the top of an auxiliary signal, or unused edge-finger, to the DC blocking capacitor in the termination circuit is as short as practicable. PCI CEM 5.0 specifies no maximum trace length. Maintain a 42.5Ω trace impedance for traces between edge fingers and DC blocking capacitors. The ground via for the termination network must lie within 1.0 mm (39.4 mil) of the resistor component pad or through-hole.

Figure 42. Add-in Card with AC Termination on All Auxiliary and Reserved Signal Conductors



1.5. Document Revision History for the Intel Agilex 7 Device Family High-Speed Serial Interface Signal Integrity Design Guidelines

Document Version	Changes
2023.06.15	• Updated product family name to "Intel Agilex 7".
2022.09.26	Added miscellaneous changes
2021.03.18	Added F-tile and R-tile Design Guidelines.
2020.07.10	Initial release.