AN 745: Design Guidelines for DisplayPort Intel® FPGA IP Interface

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Contents

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1. Design Guidelines for DisplayPort Intel® FPGA IP Interface

The design guidelines help you implement the DisplayPort Intel® FPGA IP using Intel FPGA devices.

These guidelines facilitate board designs for the DisplayPort Intel FPGA IP video interfaces.

Related Information

- DisplayPort Intel FPGA IP User Guide
- AN 837: Design Guidelines for HDMI Intel FPGA IP

1.1. DisplayPort Intel FPGA IP Design Guidelines

The DisplayPort Intel FPGA IP interface consists of a Main link, an auxiliary channel (AUX CH), and a Hot-Plug Detect (HPD) signal.

- Main Link—Main Link is a unidirectional, high-bandwidth channel that transports video and audio over 1, 2, or 4 lanes at 8.1, 5.4, 2,7, and 1.62 Gigabits per second (Gbps) per lane. All lanes carry data. The clock is embedded in 8b/10b encoded serial data.
- AUX CH—The AUX CH is 1 Megabits per second (Mbps) half-duplex bidirectional channel used for link management and device control.
- HPD—The DisplayPort Intel FPGA IP sink device uses HPD to detect its presence, The HPD signal serves as an interrupt request by the DisplayPort sink device.

Figure 1. **DisplayPort Intel FPGA IP DisplayPort Transport Channels**

This figure shows the DisplayPort Intel FPGA IP link between a source and a sink device.
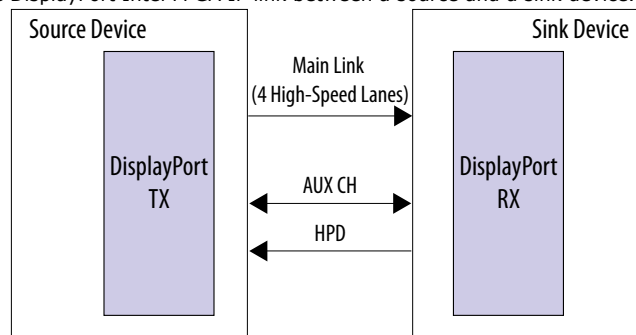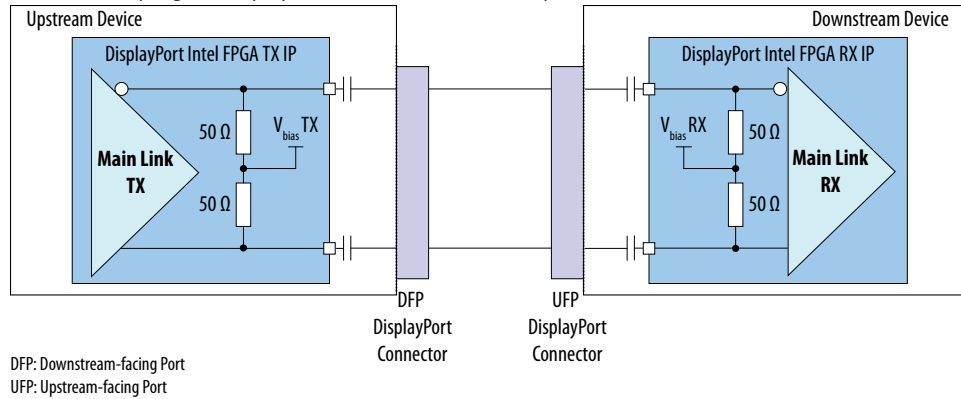

1.1.1. Main Link

The DisplayPort Intel FPGA IP Main Link is a unidirectional, high-bandwidth channel used to transport video and audio data.

Figure 2. **Main Link Differential Pair with FPGA Transceiver PHY**

This figure shows a Main Link differential pair. The DisplayPort Intel FPGA IP source must have AC-coupling capacitors. AC-coupling for DisplayPort Intel FPGA IP sink is optional.

DFP: Downstream-facing Port
UFP: Upstream-facing Port

1.1.1.1. Main Link TX

The Main Link TX drives doubly-terminated AC-coupled differential pairs.

The FPGA Transceiver PHY TX includes on-chip 100 ohm differential termination and bias voltage generation. You may add a repeater such as a retimer or a redriver in between the FPGA and the external DisplayPort connector to compensate for loss.

Table 1. **FPGA Transceiver PHY TX Operation Guidelines**

FPGA Transceiver PHY Operations	Description

Transceiver PHY TX Reference Clock Connection	A free-running 135 MHz differential clock (e.g. LVDS) is AC-coupled to a dedicated reference clock input of the transceiver bank. The reference clock input supports on-chip termination (OCT).
	Enable OCT using a QSF assignment:
	• Intel Stratix® 10 L-tile and H-tile devices
	
	`set_instance_assignment -name XCVR_S10_REFCLK_TERM_TRISTATE TRISTATE_OFF -to <dedicated refclk pin name>`
	• Intel Arria® 10 devices
	
	`set_instance_assignment -name XCVR_A10_REFCLK_TERM_TRISTATE TRISTATE_OFF -to <dedicated refclk pin name>`
	• Intel Cyclone® 10 GX devices
	
	`set_instance_assignment -name XCVR_C10_REFCLK_TERM_TRISTATE TRISTATE_OFF -to <dedicated refclk pin name>`
	• Arria V, Cyclone V, and Stratix V devices
	
	`set_instance_assignment -name XCVR_REFCLK_PIN_TERMINATION AC_COUPLING -to <dedicated refclk pin name>`
	Note: Your design does not require external termination if OCT is enabled.

Transceiver TX On-Chip Termination	By default, the Intel Quartus® Prime software enables differential 100 ohm OCT and bias voltage generation. Your design does not require external 50 ohm termination and bias voltage (`Vbias_TX`).
Transceiver TX Channel Bonding	Bonding TX channels reduces on-chip channel-to-channel skew, which allows more skew margin at the board or system level to meet the DisplayPort Intel FPGA IP Source inter-lane skew requirement.

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FPGA Transceiver PHY Operations	Description
	Refer to Table 2 on page 6 for more information.
Transceiver TX Voltage Swing and Pre-emphasis	DisplayPort TX specification for the Main Link allows four differential peak-to-peak voltage swing levels, and four pre-emphasis (Post Cursor1) levels. Certain combinations of voltage swing levels and pre-emphasis levels that result in differential peak-to-peak swing outside the allowable range (1.38 V) are not allowed.
	The reconfiguration management module available in the Intel Quartus Prime design example includes a sub-module that translates the DisplayPort voltage swing and pre-emphasis levels to the FPGA transceiver setting. Refer to Table 3 on page 6 for more information.
	Use the reconfiguration management file and a sub-module of the Intel Quartus Prime design examples that maps the DisplayPort levels to the transceiver analog parameter setting.

	• Intel Stratix 10 L-tile and H-tile devices
	    Reconfiguration management module : `bitec_reconfig_alt_s10.v`
	    Sub-module: tx_analog mappings, rx_analog mappings
	• Intel Arria 10 devices
	    Reconfiguration management module : `bitec_reconfig_alt_a10.v`
	    Sub-module: tx_analog mappings, rx_analog mappings
	• Intel Cyclone 10 GX devices
	    Reconfiguration management module : `bitec_reconfig_alt_c10.v`
	    Sub-module: tx_analog mappings, rx_analog mappings
	• Arria V devices
	    Reconfiguration management module : `bitec_reconfig_alt_av.v`
	    Sub-module: dp_analog_mappings
	• Cyclone V devices
	    Reconfiguration management module : `reconfig_mgmt_hw_ctrl.v`
	    Sub-module: dp_analog_mappings
	• Stratix V devices
	    Reconfiguration management module : `bitec_reconfig_alt_sv.v`
	    Sub-module: dp_analog_mappings

TX Repeater (Redriver or Retimer)	To mitigate system signal losses, you may place a redriver or retimer between the FPGA and the external DisplayPort connector for a box-to-box connection. In such designs, place the repeater close to the external DisplayPort connector and generate the DisplayPort signals at the voltage and pre-emphasis levels determined during link training, instead of the FPGA.
	In this case, you can turn off the **Support analog reconfiguration** option in the DisplayPort Intel FPGA IP parameter editor and set the FPGA voltage swing in the QSF assignments. The selection of the appropriate signaling level between the FPGA and the repeater depend on the PCB loss and the equalization of the redriver/retimer input. The typical setting for the transmitter is 400 mV voltage swing without pre-emphasis.
	Refer to Table 4 on page 6 for more information.

Bonded TX channels placed in a single transceiver bank results in lower channel-to-channel skew, allowing more skew budget at the board level. For information about the maximum channel-to-channel skew, refer to the *Device Datasheet*.

You have the option to select bonding mode through the Transceiver PHY parameter editor.

Table 2.   Bonding Mode Selection Guidelines

Device Family	Transceiver PHY Bonding Mode	Notes
Intel Stratix 10 L-tile and H-tile/Intel Arria 10/Intel Cyclone 10 GX	PMA and PCS bonding	• Requires bonded TX channels to be placed contiguously • Logical channel 0 is selected as a bonding master • Uses x6/xN clock network driven by Master Clock Generation Block (MCGB). MCGB is enabled in the TX PLL (e.g. fPLL) parameter editor. *Note:* The digital reset signal (`tx_digitalreset`) to all TX channels within a bonded group must meet a maximum skew tolerance of one-half the TX parallel clock cycle (`tx_clkout`). Refer to the *Timing Constraints for Bonded PCS and PMA Channels* section of the respective *Transceiver PHY User Guides* for more information.
Arria V	xN	–
Stratix V	x6/xN	–

Table 3.   Recommended Combinations of Voltage Swing and Pre-Emphasis Levels

This table lists the 4 levels of voltage swing level defined in the *Video Electronics Standards Association (VESA) DisplayPort Standard*. The combination of these levels is independent of the devices. Intel FPGA devices support all 4 levels. The mapping between the DisplayPort levels and the actual PMA values is provided in the DisplayPort Intel FPGA IP design examples.

Voltage Swing Level	Pre-Emphasis Level			
	0	1	2	3
0	Supported	Supported	Supported	Supported
1	Supported	Supported	Supported	Not allowed
2	Supported	Supported	Not allowed	Not allowed
3	Supported	Not allowed	Not allowed	Not allowed

Table 4.   Guidelines on the Usage of the TX Repeater Device

Device Family	DisplayPort version 1.2 Rates (RBR, HBR, HBR2)	DisplayPort version 1.4 Rate (HBR3)	Example Repeater
Intel Stratix 10 L-tile and H-tile	Not Required	Not Required	–
Intel Arria 10	Not Required	Not Required	–
Intel Cyclone 10 GX	Not Required	Not Required	–
			continued...

Device Family	DisplayPort version 1.2 Rates (RBR, HBR, HBR2)	DisplayPort version 1.4 Rate (HBR3)	Example Repeater
Arria V	Required [1]	Not Applicable [2]	TI SN75DP130 (Redriver)
Cyclone V	Required [1]	Not Applicable [2]	TI SN75DP130 (Redriver)
Stratix V	Not Required	Not Applicable [2]	–

1.1.1.2. Main Link TX Electrical Specifications

Use the listed Main Link transmitter electrical parameters for reference. Refer to the *VESA DisplayPort Standard* for other transmitter electrical parameters.

Table 5.   TP2 (TX External Connector)

Note: The Lane-to-Lane Output Skew specification at TP2 in *VESA DisplayPort Standard* version 1.2a differs from version 1.4.

Parameter	Minimum	Typical	Maximum	Notes
Maximum Output Voltage Level	–	–	1.38 V	Maximum differential peak-to-peak swing for all output level and pre-emphasis combinations
Lane-to-Lane Output Skew	–	–	1250 ps	*VESA DisplayPort Standard version 1.4* for all data rates
Lane-to-Lane Output Skew (HBR, RBR)	–	–	2 UI	*VESA DisplayPort Standard version 1.2a* for HBR and RBR
Lane-to-Lane Output Skew (HBR2)	–	–	4 UI + 500 ps	*VESA DisplayPort Standard version 1.2a* for HBR2

Table 6.   TP3_EQ (Compliance Cable Model with Reference Receiver Equalizer)

Parameter	Minimum	Typical	Maximum	Notes
Maximum TX Total Jitter	–	–	0.65 UI	For HBR3, TPS4 pattern, at 1E-9
	–	–	0.62 UI	For HBR2, CP2520 pattern, at 1E-9
	–	–	0.40 UI	For HBR2, D10.2 pattern, at 1E-9
TX Differential Peak-to-Peak EYE Voltage at HBR3	75 mV	–	–	For HBR3, TPS4 pattern, at 1E-9
TX Differential Peak-to-Peak EYE Voltage at HBR2	90 mV	–	–	For HBR2, CP2520 pattern, at 1E-9

Note: For more information about TP2 and TP3_EQ compliance measurement points and reference receiver equalizer, refer to the *VESA DisplayPort Standard*.

1.1.1.3. Main Link RX

The FPGA Transceiver PHY RX includes on-chip 100 ohm differential termination and bias voltage generation.

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[1] Configure the PMA settings of the repeater, so that the link quality between the repeater and FPGA is optimum.

[2] This device does not support HBR3 data rate.

You may add an RX repeater such as a retimer or a redriver in between the FPGA and the external DisplayPort connector to clean up jitter and compensate for losses. AC-coupling is optional for Main Link RX.

Table 7.   FPGA Transceiver PHY RX Operation Guidelines

FPGA Transceiver PHY Operations	Description
Transceiver RX On-Chip Termination	By default, the Intel Quartus Prime software enables differential 100 ohm OCT and bias voltage generation. Your design does not require external 50 ohm termination and bias voltage (`Vbias_RX`).
RX Repeater (Redriver or Retimer)	To clean up jitter and compensate for signal losses, a sink device uses a redriver or retimer between the external DisplayPort connector and the FPGA RX. In such systems, the device places the repeater close to the external DisplayPort connector and regenerates the received DisplayPort signals. • The retimer includes the clock and data recovery (CDR) circuit that cleans up the jitter. • The redriver does not have a CDR circuit. Refer to Table 8 on page 8 for more information.

Table 8.   Guidelines on the Usage of the RX Repeater Device

Device Family	VESA DisplayPort Standard version 1.2a Rates (RBR, HBR, HBR2)	VESA DisplayPort Standard version 1.4 Rate (HBR3)	Example Repeater
Intel Stratix 10 L-tile and H-tile	Not Required [3]	Not Required [3]	–
Intel Arria 10 and Intel Cyclone 10 GX	Not Required [3]	Required [4]	• Parade Technologies PS8460 (Retimer) • Megachip MCD6000C1
Arria V	Required [4]	Not Applicable [5]	TI SN75DP130 (Redriver)
Cyclone V	Required [4]	Not Applicable [5]	TI SN75DP130 (Redriver)
Stratix V	Not Required	Not Applicable [5]	–

1.1.1.4. Main Link RX Electrical Specifications

Use the listed Main Link receiver electrical parameters for reference. Refer to the *VESA DisplayPort Standard* for other receiver electrical parameters.

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[3] Intel recommends that you perform signal integrity analysis to determine whether a retimer or redriver should be added between the DisplayPort RX connector and the FPGA for data rates up to HBR3; to compensate the insertion loss due to long cables or multiple cables with different signal qualities and weakness in the transmitter.

[4] Configure the PMA settings of the repeater or retimer, so that the link quality between the repeater or retimer and FPGA is optimum.

[5] This device does not support HBR3 data rate.

Table 9.   TP3_EQ

Parameter	Minimum	Typical	Maximum	Notes
Minimum Receiver EYE Width at HBR3	0.35 UI	–	–	For HBR3, TPS4 pattern
RX Differential Peak-to-Peak EYE Voltage at HBR3	75 mV	–	–	
Minimum Receiver EYE Width at HBR2	0.38 UI	–	–	For HBR2, CP2520 pattern
RX Differential Peak-to-Peak EYE Voltage at HBR2	70 mV	–	–	

*Note:*   For more information about TP3_EQ compliance measurement point and reference receiver equalizer, refer to the *VESA DisplayPort Standard*.

1.1.2. AUX Channel

The DisplayPort AUX channel is a half-duplex, bidirectional channel running at 1 Mbps rate.

Figure 3.   AUX Channel Differential Pair

The AUX channel is a differential pair doubly-terminated with 50 ohm resistors and AC-coupled at both source and sink devices.
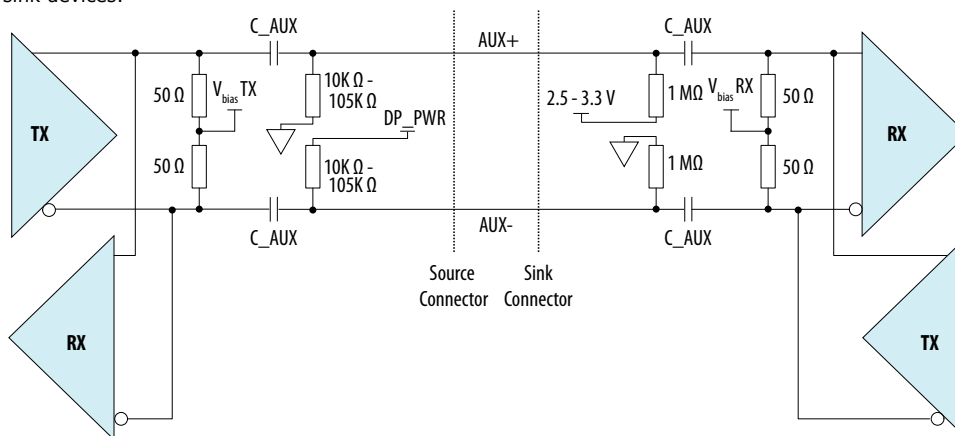
The 100-KΩ and 1-MΩ pull-up and pull-down resistors are placed between the connectors and AC-coupling capacitors. These resistors help detect any DisplayPort upstream devices, including a powered DisplayPort upstream device by a sink device.

Table 10.   AUX Channel Electrical Specification

The table shows the parameters of the DisplayPort AUX channel electrical specification.

Parameter	Minimum	Maximum	Notes
AUX Direct Current (DC) Common Mode Voltage	0.0 V	2.0 V	Common mode voltage is equal to Vbias_TX (or Vbias_RX)
AUX Peak-to-Peak Voltage	0.29 V	1.38 V	Differential peak-to-peak voltage swing
AUX AC-Coupling Capacitor	75 nF	200 nF	The AUX channel AC-coupling capacitors are placed on both the DisplayPort upstream and downstream devices.

1.1.2.1. Implementing Bus LVDS I/O Interface

Intel devices offer on-chip Bus LVDS (BLVDS) I/O interface that you can use to implement the DisplayPort AUX channel.

The BLVDS I/O is a bidirectional differential I/O interface and requires special pin assignment consideration. Depending on the FPGA bank VCCIO voltage and I/O standard used, the BLVDS I/O may require a series resistor, R_s. The series resistor ensures the AUX channel differential voltage swing is below the maximum peak-to-peak voltage swing specification.

Figure 4. AUX Channel Using BLVDS I/O Interface

The figure shows the FPGA BLVDS I/O with series resistors for the DisplayPort Source (or Sink) AUX channel implementation.
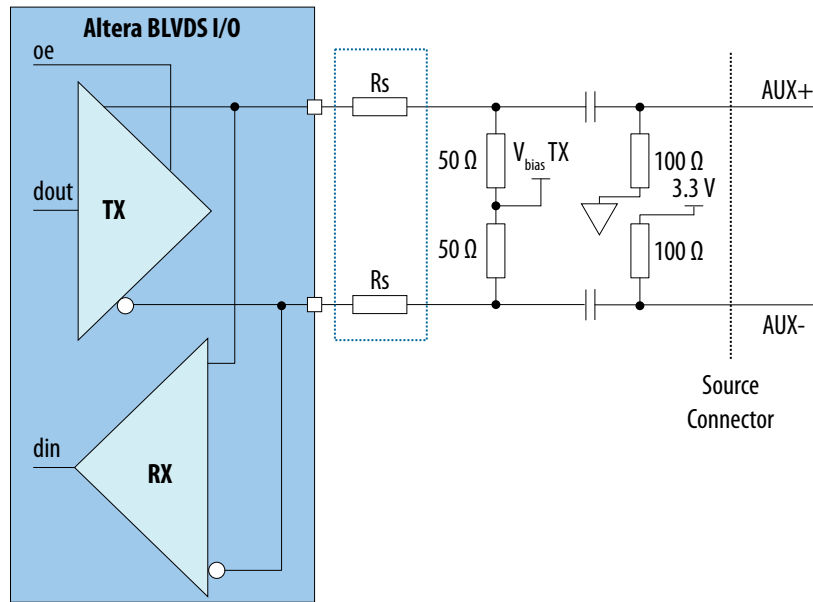

Table 11. BLVDS I/O Support

The table lists the FPGA BLVDS I/O supported features and I/O standards.

Note: Vbias_TX (or Vbias_RX) = VCCIO/2, VCCIO is the FPGA I/O supply voltage.

| FPGA Device	Pin	I/O Standard	VCCIO	Series Resistor (Rs) Value
Intel Arria 10, Intel Cyclone 10 GX, and Intel Stratix 10	LVDS	Differential SSTL-18 Class I	1.8 V	22 Ω
		Differential SSTL-18 Class II		
Arria V, Cyclone V, and Stratix V	DIFFIO_RX[6]	Differential SSTL-2 Class II	2.5 V	100 Ω

1.1.2.2. Implementing Bidirectional LVDS

Alternatively, you can implement half-duplex, bidirectional LVDS using an external LVDS line driver/receiver.

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[6] DFFIO_TX pins do not support true LVDS differential inputs.

Figure 5.   External LVDS Line Driver/Receiver

The figure shows an example of an external LVDS driver/receiver, TI SN65MLVD200A used in Bitec HSMC DisplayPort daughter card.
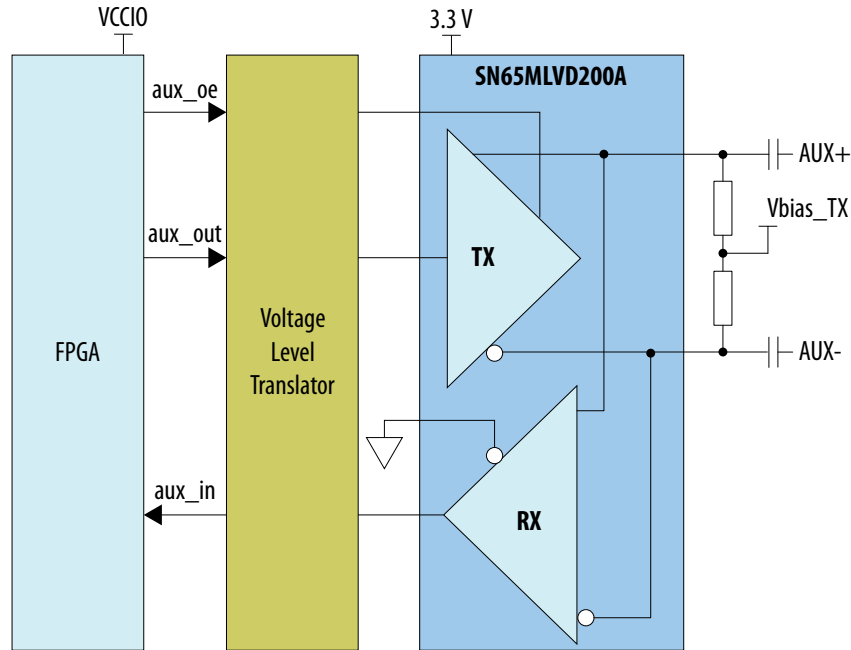
The interface to the device is straightforward. For example, TI SN65MLVD200A requires three LVTTL general purpose I/O pins (`aux_oe`, `aux_out`, `aux_in`). If the FPGA bank I/Os are not tolerant with LVTTL, a level shifter is required, as shown in the figure above.

There may be crosstalk from the single-ended LVTTL signals to the Main-Link high speed signals if the traces are routed close to each other. During board signal integrity (SI) design, pay special attention to routing.

Note: The DisplayPort Intel FPGA IP design examples are developed based on the Bitec DisplayPort daughter card using TI SN65MLVD200A.

For more information about the BLVDS driver, TI SN65MLVD200A, refer to the SN65MLVD20xx Multipoint-LVDS Line Driver and Receiver datasheet.

1.1.2.3. Detection of DisplayPort Upstream Source Device

The DisplayPort sink device senses the AUX+ and AUX- signal logic level to detect the upstream source.

The weak pull-up and pull-down resistors form a voltage divider that allows the sink device to detect the presence of the upstream source device.

Between the AC-coupling capacitor and the DisplayPort connector:

- The source device weakly pulls down the AUX+ line to GND and weakly pulls up the AUX- line to DP_PWR (typically 3.3 V) with nominal 100K ohm resistors.
- The sink device weakly pulls up the AUX+ line to 3.3 V and weakly pulls down the AUX- line to GND with nominal 1M ohm resistors.

The AUX+ and AUX- lines connect to the FPGA through 10K ohm resistors (e.g. `RX_SENSE_P` and `RX_SENSE_N` signals in the Bitec DisplayPort daughter card). The DisplayPort Intel FPGA IP sink senses the logic level of the AUX+ and AUX- lines using the `rx_cable_detect` and `rx_pwr_detect` inputs and triggers the HPD signal when the powered upstream source device is detected.

The sense signals require level translation if they are connected to an FPGA I/O that is not 3.3V tolerant, for example, Intel Arria 10 device bank with VCCIO = 1.8 V.

1.1.3. DisplayPort Hot Plug Detect (HPD)

The DisplayPort sink device drives the HPD signal using 3.3V TTL signal level. The upstream DisplayPort source device monitors the HPD signal.

To prevent the HPD signal from floating when not connected, tie to GND with a >100K ohm resistor in both the DisplayPort Intel FPGA IP source and sink devices.

Note: The voltage level of the HPD pin uses 3.3 V TTL. FPGA I/Os that are not tolerant with 3.3V TTL require a level shifter.

1.1.4. DisplayPort Power

For Box-to-Box DisplayPort connection, the DisplayPort source and sink devices provide a power pin and a return current pin on the connector.

This power is provided by the DisplayPort source and sink to power up attached devices such as a Branch device or an Active Cable Assembly.

As per the *VESA DisplayPort Standard*, the maximum current drawn by an attached device is 0.5 A at 3.3V setting.

1.1.5. Bitec DisplayPort Daughter Card Revisions

The schematic diagrams of the Bitec HSMC and FMC DisplayPort daughter cards show the connectivity for Intel FPGA development boards.

Table 12.   Bitec DisplayPort FMC Daughter Card Revisions

Revision	Release Date	Change	Note
Rev. 11	August 2018	Added MCD6000C1 Retimer at RX.	• RX lane polarity inverted • RX lane order reversed • TX lane polarity not inverted • TX lane order not reversed
Rev. 10	May 2017	Added Parade Technologies Retimer (PS8460) on RX.	• RX lane polarity inverted • RX lane order not reversed • TX lane polarity not inverted • TX lane order not reversed *VESA DisplayPort PHY CTS version 1.4* passed in Intel Arria 10 device.
			continued...

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Revision	Release Date	Change	Note
			Note: The production of Bitec FMC daughter card Rev. 10 has been discontinued. However, Intel still supports the daughter card to be used with DisplayPort Intel FPGA IP designs.
Rev. 8	November 2017	–	• RX lane polarity not inverted • RX lane order not reversed • TX lane polarity inverted • TX lane order reversed • No redriver/retimer used

Related Information

- Schematic Diagram for HSMC DisplayPort Daughter Card Revision 11
- Schematic Diagram for FMC DisplayPort Daughter Card Revision 8

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2. Document Revision History for AN 745: Design Guidelines for DisplayPort Intel FPGA IP Interface

Document Version	Changes
2020.04.13	• Updated the *Main Link TX* and *Main Link RX* sections to update the existing information and include information about Intel Stratix 10 L-tile and H-tile devices. • Updated the *Implementing Bus LVDS I/O Interface* section to include the latest I/O standard information. • Updated the *Bitec DisplayPort FMC Daughter Card Revisions* with the latest Bitec daughter card revision information.
2020.01.10	• Added description for the AUX channel differential pair diagram and information about the AUX channel specification in the *AUX Channel* section. • Added information about Bus LVDS I/O interface.
2018.01.22	• Removed all information about the Intel FPGA HDMI interface to *AN 837: Design Guidelines for Intel FPGA HDMI* . • Changed the title of this document to *AN 745: Design Guidelines for DisplayPort Intel FPGA IP Interface*. • Added specific guidelines for Main Link RX and TX. • Added information about receiver electrical parameters. • Added guidelines for DisplayPort Power. • Removed the schematic diagrams and provided links to the diagrams on the Bitec product page.
2015.11.02	Initial release.

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