



AN 114: Board Design Guidelines for Intel Programmable Device Packages



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AN-114

ID: **683481**

Version: **2022.05.27**

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1. AN 114: Board Design Guidelines for Intel® Programmable Device Packages

As programmable logic devices (PLDs) increase in density and I/O pins, the demand for small packages and diverse packaging options continues to grow. Ball-grid array (BGA) packages are an ideal solution because the I/O connections are on the interior of the device, improving the ratio between pin count and board area. Typical BGA packages contain between two to eight more connections as quad flat pack (QFP) packages. Furthermore, BGA solder balls are considerably stronger than QFP leads, resulting in robust packages that can tolerate rough handling.

This application note provides the recommended PCB design guidelines for some of the more complex package options offered for Intel® Programmable Devices except for Intel Stratix® 10 devices and beyond.

Note: For more information about Intel Stratix 10 device packages and beyond, refer to the respective individual Manufacturing Advantage Services (MAS) Guidelines document.

Related Information

- [Package Information \(dimensions, materials, etc.\) and Thermal Resistance](#)
- [Manufacturing with Intel Stratix 10 Field Programmable Gate Arrays](#)
- [AN 766: Intel Stratix 10 Devices, High Speed Signal Interface Layout Design Guideline](#)
- [AN 875: Intel Stratix 10 E-Tile PCB Design Guidelines](#)

1.1. Overview of BGA Packages

In BGA packages, the I/O connections are located on the interior of the device. Leads normally placed along the periphery of the package are replaced with solder balls arranged in a matrix across the bottom of the substrate. The final device is soldered directly to the PCB using assembly processes that are virtually identical to the standard surface mount technology preferred by system designers.

Additionally, BGA packages provide the following advantages:

- Fewer damaged leads—BGA leads consist of solid solder balls, which are less likely to suffer damage during handling.
- More leads per unit area—Lead counts are increased by moving the solder balls closer to the edges of the package and by decreasing pitch to the following:
 - 1.0 mm for flip-chip and wirebond BGAs
 - 0.8 mm, 0.5 mm, and 0.4 mm for wirebond and wafer level chip scale package (WLCSP) (also known as VBGA) fine pitch BGAs.
- Less expensive surface mount equipment—BGA packages can tolerate slightly imperfect placement during mounting, requiring less expensive surface mount equipment. The placement can be imperfect because the BGA packages self-align during solder reflow.
- Smaller footprints—BGA packages are usually 20% to 50% smaller than QFP packages, making BGA packages more attractive for applications that require high performance and a smaller footprint.
- Integrated circuit speed advantages—BGA packages operate well into the microwave frequency spectrum and achieve high electrical performance by using ground planes, ground rings, and power rings in the package construction.
- Improved heat dissipation—Because the die is located at the center of the BGA package and most GND and VCC pins are located at the center of the package, the GND and VCC pins are located under the die. As a result, the heat generated in the device can be transferred out through the GND and VCC pins (i.e., the GND and VCC pins act as a heat sink).

1.2. PCB Layout Terminology

This section defines common terms used in PCB layout that you need to know to design with Intel Programmable Devices.

1.2.1. Escape Routing

Escape routing is the method used to route each signal from a package to another element on the PCB.

1.2.2. Multi-Layer PCBs

The increased I/O count associated with BGA packages has made multi-layer PCBs the industry-standard method for performing escape routing. Signals can be routed to other elements on the PCB through various numbers of PCB layers.

1.2.3. Vias

Vias, or plated through holes, are used in multi-layer PCBs to transfer signals from one layer to another. Vias are actual holes drilled through a multi-layer PCB and provide electrical connections between various PCB layers. All vias provide layer-to-layer connections only. Device leads or other reinforcing materials are not inserted into vias.

The following table lists the terms used to define via dimensions.

Table 1. Via Dimension Terms

Term	Description
Aspect ratio	The ratio of a via's length or depth to its pre-plated diameter.
Drilled hole diameter	The diameter of the actual via hole drilled in the board.
Finished via diameter	The final diameter of a via hole after it has been plated.

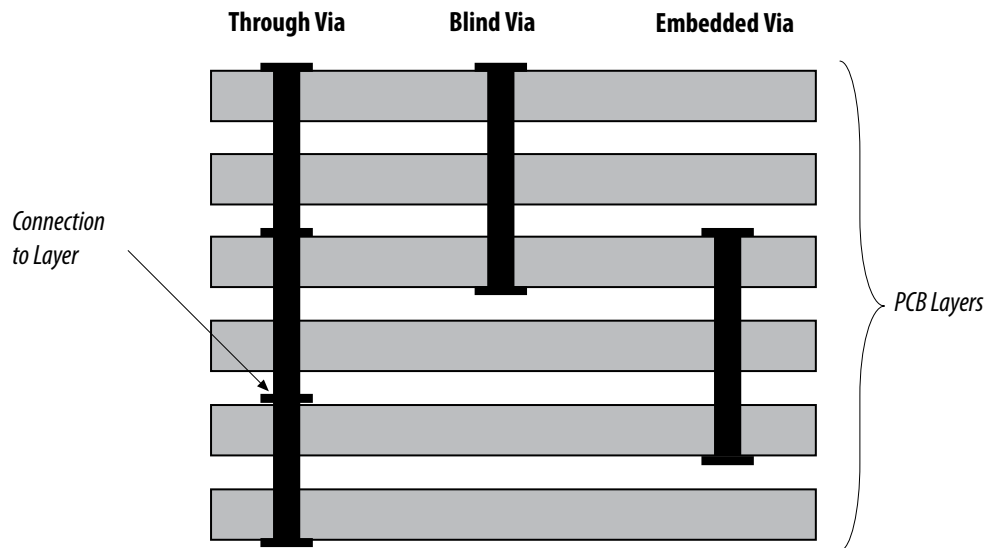
The following table lists the three via types typically used on PCBs.

Table 2. Via Types

Type	Description
Through via	An interconnection between the top and the bottom layer of a PCB. Vias also provide interconnections to inner PCB layers.
Blind via	An interconnection from the top or bottom layer to an inner PCB layer.
Embedded via	An interconnection between any number of inner PCB layers.

The following figure shows all three via types.

Figure 1. Types of Vias



Blind vias and through vias are used more frequently than embedded vias. Blind vias can be more expensive than through vias, but overall costs are reduced when signal traces are routed under a blind via, requiring fewer PCB layers. Through vias, on the other hand, do not permit signals to be routed through lower layers, which can increase the required number of PCB layers and overall costs.

1.2.4. Via Capture Pad

Vias are connected electrically to PCB layers through via capture pads that surround each via.

1.2.5. Surface Land Pad

Surface land pads are the areas on the PCB to which the BGA solder balls adhere. The size of these pads affects the space available for vias and for escape routing. In general, surface land pads are available in the following two basic designs:

- Non solder mask defined (NSMD), also known as copper defined
- Solder mask defined (SMD)

The main differences between the two surface land pad types are the size of the trace and spacing between the trace lines, the type of vias you can use, and the shape of the solder balls after solder reflow.

Figure 2. Side View of NSMD and SMD Land Pads

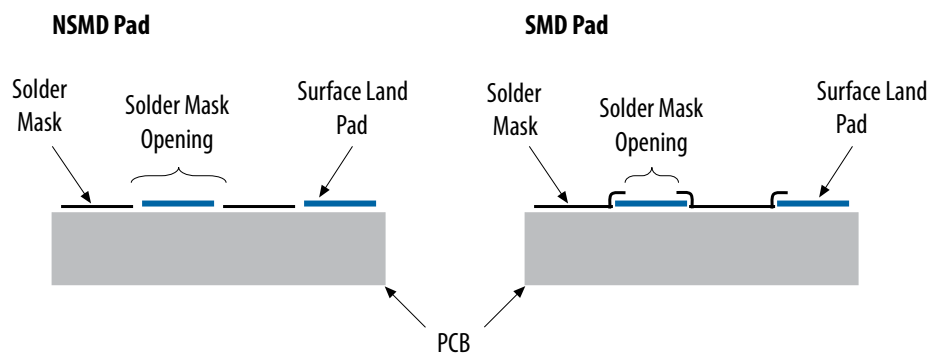
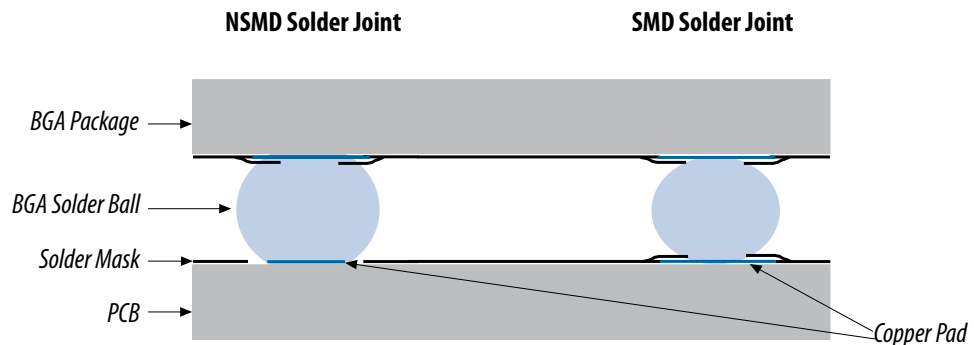


Figure 3. Side View of NSMD and SMD Solder Joints



1.2.5.1. Non Solder Mask Defined Pad

In the NSMD pad, the solder mask opening is larger than the copper pad. Thus, the surface land pad’s copper surface is completely exposed, providing greater area to which the BGA solder ball can adhere. Refer to [Figure 2](#) on page 6 for the Side View of NSMD and SMD Land Pads.

Note: Intel recommends that you use a NSMD pad for most applications because it provides more flexibility, fewer stress points, and more line-routing space between pads.

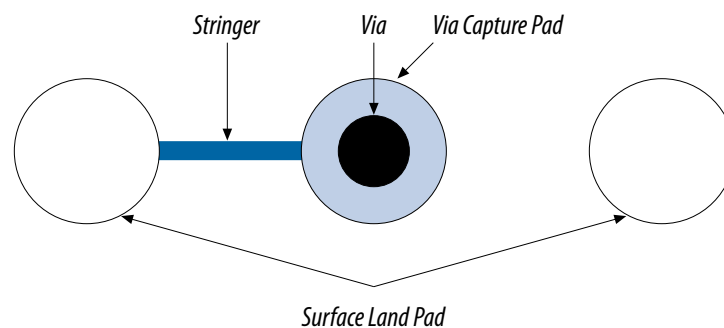
1.2.5.2. Solder Mask Defined Pad

In an SMD pad, the solder mask overlaps the surface land pad's copper surface. Refer to [Figure 3](#) on page 6 for the Side View of NSMD and SMD Land Pads. This overlap provides greater adhesion strength between the copper pad and the PCB's epoxy/glass laminate, which can be important under extreme bending and during accelerated thermal cycling tests. However, the solder mask overlap reduces the amount of copper surface available for the BGA solder ball.

1.2.6. Stringer

Stringers are rectangular or square interconnect segments that electrically connect via capture pads and surface land pads.

Figure 4. Via, Land Pad, Stringer, and Via Capture Pad



1.3. PCB Layout for High-Density BGA Packages

When designing a PCB for high-density BGA packages, consider the following factors:

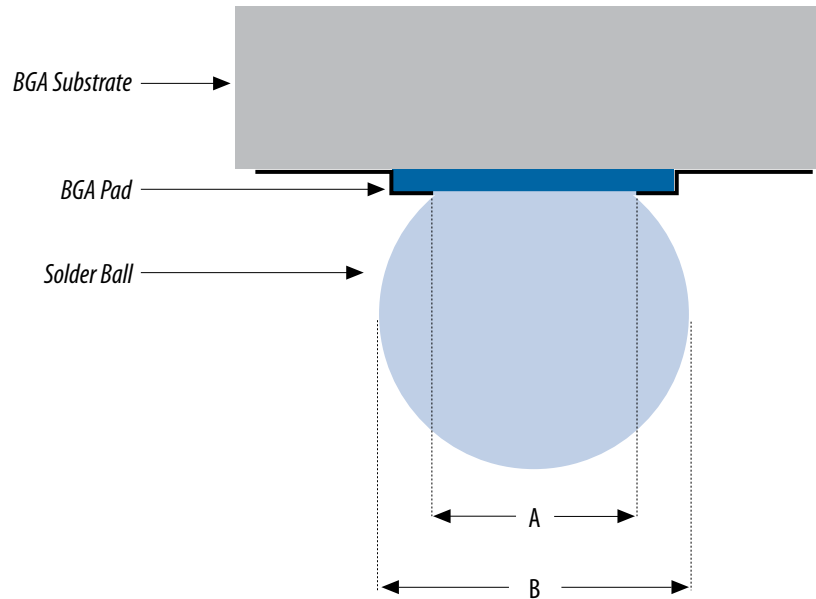
- Surface land pad dimension
- Via capture pad layout and dimension
- Signal-line space and trace width
- Number of PCB layers

Note: Controlling dimension is calculated in millimeters for all high-density BGA figures.

1.3.1. Surface Land Pad Dimension

Intel has done extensive modeling simulation and experimental studies to determine the optimum land pad design on the PCB to provide the longest solder joint fatigue life. The results of these studies show that a pad design that provides a balanced stress on the solder joint provides the best solder joint reliability. If SMD pads are used on the PCB, the surface land pads should be the same size as the BGA pad to provide a balanced stress on solder joints. If non-solder mask defined pads are used on the PCB, the land pads should be approximately 15% smaller than the BGA pad size to achieve a balanced stress on solder joints.

Figure 5. BGA Pad Dimensions



The following table lists the recommended pad sizes for SMD and NSMD land patterns. You should use NSMD pads for high-density board layouts because the smaller pad sizes allow for more space between vias and trace routing.

Table 3. Recommended Pad Sizes for SMD and NSMD Pads

BGA Pad Pitch	BGA Pad Opening (A) (mm) (Typical)	Recommended SMD Pad Size (mm)	Recommended NSMD Pad Size (mm) ⁽¹⁾
1.27 mm (Plastic Ball Grid Array (PBGA))	0.60	0.60	0.51
1.27 mm (Super Ball Grid Array (SBGA))	0.60	0.60	0.51
1.27 mm (Tape Ball Grid Array (TBGA))	0.60	0.60	0.51
1.27 mm (flip-chip) ⁽²⁾	0.65	0.65	0.55
1.00 mm (wirebond) ⁽²⁾	0.45	0.45	0.38
1.00 mm (flip-chip) ^{(2), (3)}	0.55	0.55	0.47
1.00 mm (flip-chip) ⁽²⁾ APEX 20KE	0.60	0.60	0.51
0.80 mm UBGA (wirebond)	0.40	0.40	0.34

continued...

- ⁽¹⁾ Stencil opening recommendation—Intel recommends you to use the NSMD Pad Size as the minimum stencil opening and should not go more than the SMD Pad Size for each of the BGA Package based on this table.
- ⁽²⁾ Fineline BGA packages that use flip-chip technology are marked "Thermally Enhanced FineLine BGA" and wirebond packages are marked "Non-Thermally Enhanced FineLine BGA" in the Intel Device Package Information Datasheet.
- ⁽³⁾ This is not applicable for Intel Stratix 10 devices.

BGA Pad Pitch	BGA Pad Opening (A) (mm) (Typical)	Recommended SMD Pad Size (mm)	Recommended NSMD Pad Size (mm) ⁽¹⁾
0.80 mm UBGA (EPC16U88)	0.40	0.40	0.34
0.80 mm UBGA (flip-chip)	0.425	0.425	0.36
0.80 mm UBGA (flip-chip)	0.45	0.45	0.38
0.50 mm MBGA	0.30	0.27	0.26

Note: For more information about Intel Stratix 10 packages and beyond, refer to the respective individual Manufacturing Advantage Services (MAS) Guidelines document.

The following table lists the PCB design guidelines for VBGA (also known as WLCSP) 0.4-mm ball pitch.

Table 4. Recommended Pad Sizes for VBGA (also known as WLCSP)

BGA Pad Pitch	PCB Cu Pad Size NSMD (mm)	Solder Mask Opening NSMD (mm)	PCB Cu Pad Size SMD (mm)	Solder Mask Opening SMD (mm)
0.4 mm VBGA (also known as WLCSP)	0.22	0.32	0.32	0.22

The following figures show the via and routing space available for 1.00-mm, 0.80-mm, and 0.50-mm pitch packages when using NSMD land pads.

⁽¹⁾ Stencil opening recommendation—Intel recommends you to use the NSMD Pad Size as the minimum stencil opening and should not go more than the SMD Pad Size for each of the BGA Package based on this table.

Figure 6. Via and Routing Space Available for 1.00-mm Flip-Chip BGA NSMD Land Pads

This is not applicable for Intel Stratix 10 devices.

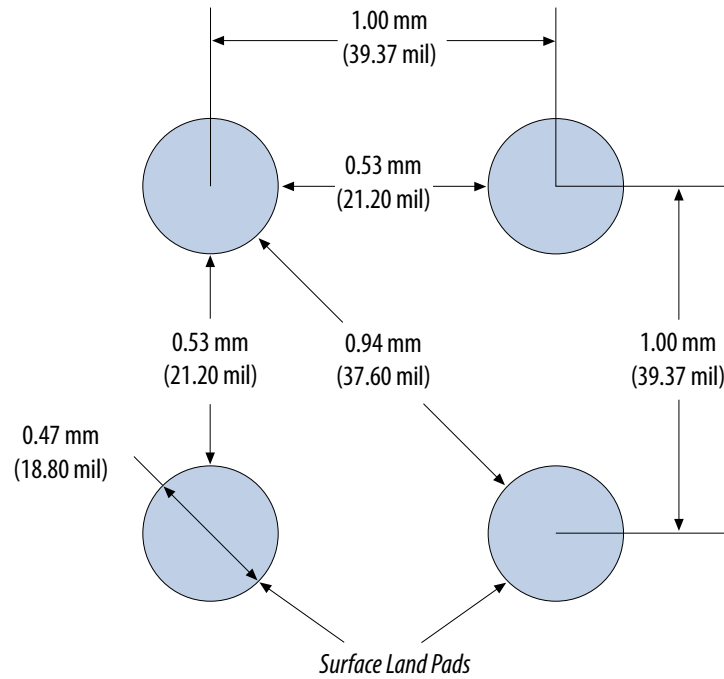


Figure 7. Via and Routing Space Available for 0.80-mm UBGA (BT Substrate) NSMD Land Pads

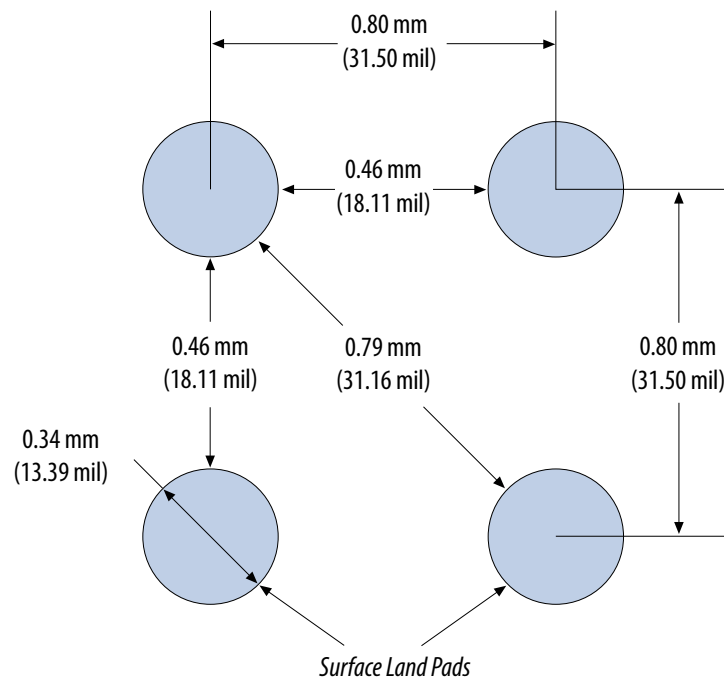
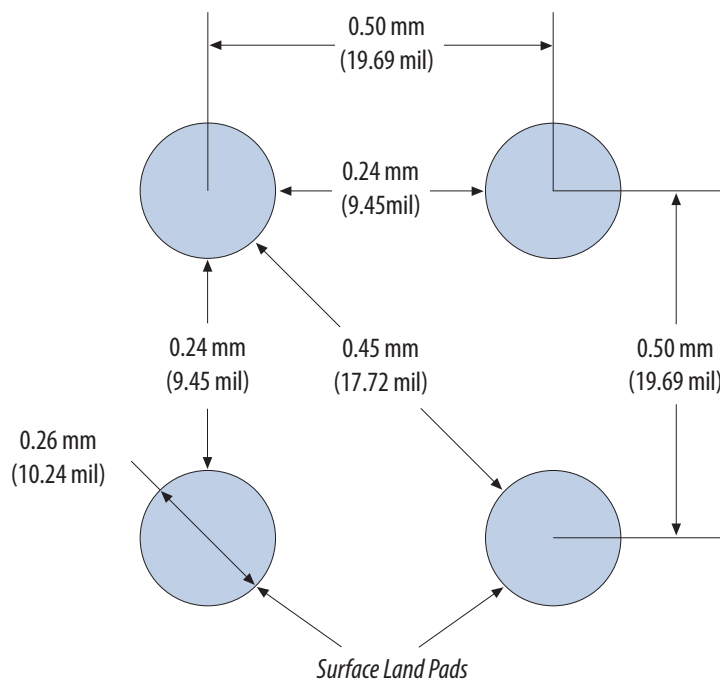


Figure 8. Via and Routing Space Available for 0.50-mm MBGA NSMD Land Pads



Related Information

[Manufacturing with Intel Stratix 10 Field Programmable Gate Arrays](#)

1.3.2. Via Capture Pad Layout and Dimension

The size and layout of via capture pads affect the amount of space available for escape routing. In general, you can lay out via capture pads in the following two ways:

- In-line with the surface land pads
- Diagonal to the surface land pads

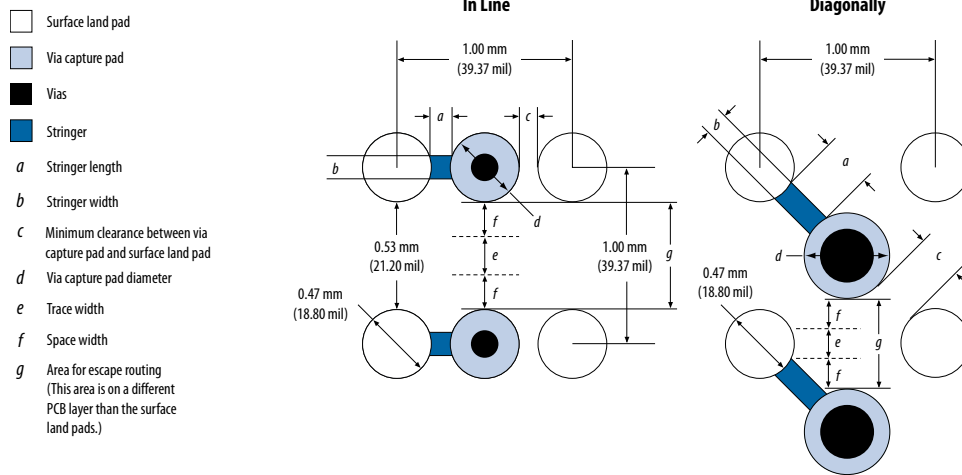
The decision to place the via capture pads diagonally or in-line with the surface land pads is based on the following factors:

- Diameter of the via capture pad
- Stringer length
- Clearance between via capture pad and surface land pad

Use [Figure 9](#) on page 12 and [Table 5](#) on page 12 to guide the layout of 1.00-mm pitch BGA packages using NSMD land pads.

Figure 9. Placement of Via Capture Pad for 1.00-mm Flip-Chip BGA NSMD Land Pads

This is not applicable for Intel Stratix 10 devices.



If your PCB design guidelines do not conform to either equation in the following table, contact Intel Premier Support for further assistance.

Table 5. Formula for Via Layouts for 1.00-mm Flip-Chip BGA NSMD Land Pads

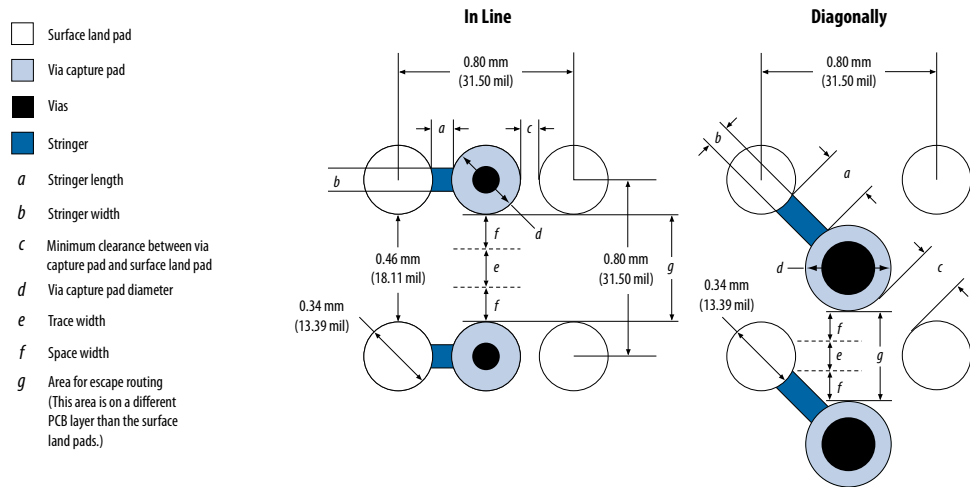
This is not applicable for Intel Stratix 10 devices.

Layout	Formula
In-line	$a + c + d \leq 0.53 \text{ mm}$
Diagonally	$a + c + d \leq 0.94 \text{ mm}$

Note that [Table 5](#) on page 12 shows that you can place a larger via capture pad diagonally than in-line with the surface land pads.

Use [Figure 10](#) on page 13 and [Table 6](#) on page 13 to guide the layout of 0.80-mm pitch U BGA packages using NSMD land pads.

Figure 10. Placement of Via Capture Pad for 0.80-mm UBGA (BT Substrate) NSMD Land Pads



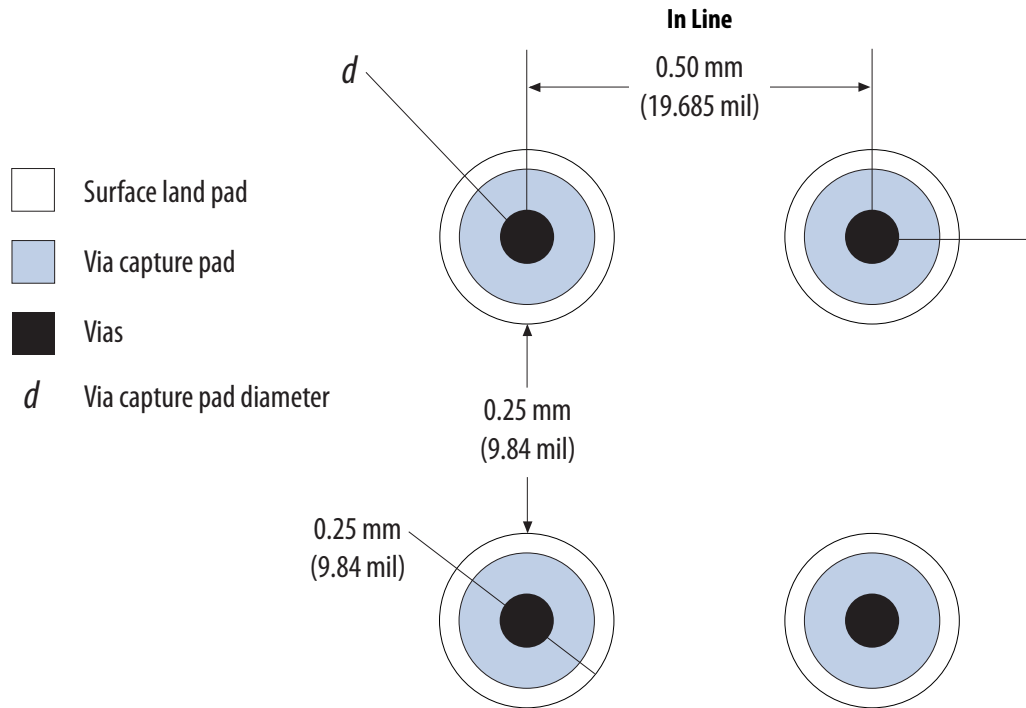
If your PCB design guidelines do not conform to either equation in the following table, contact mySupport for further assistance.

Table 6. Formula for Via Layouts for 0.80-mm UBGA (BT Substrate) NSMD Land Pads

Layout	Formula
In-line	$a + c + d \leq 0.46 \text{ mm}$
Diagonally	$a + c + d \leq 0.68 \text{ mm}$

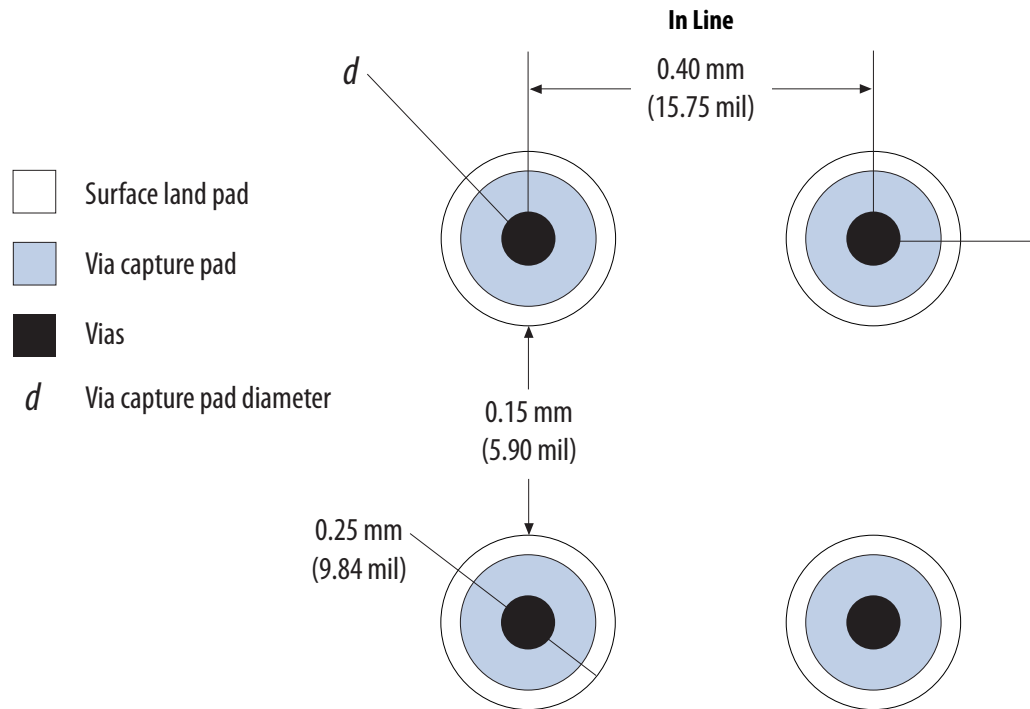
Note that [Table 6](#) on page 13 shows that you can place a larger via capture pad diagonally than in-line with the surface land pads.

Figure 11. Placement of Via Capture Pad for 0.5-mm MBGA Land Pads



For 0.5-mm pitch, Intel recommends you to use microvia technology of 0.10-mm via drill in the pad, and route trace in the inner layers.

Figure 12. Placement of Via Capture Pad for 0.4-mm VBGA (also known as WLCSP) Land Pads



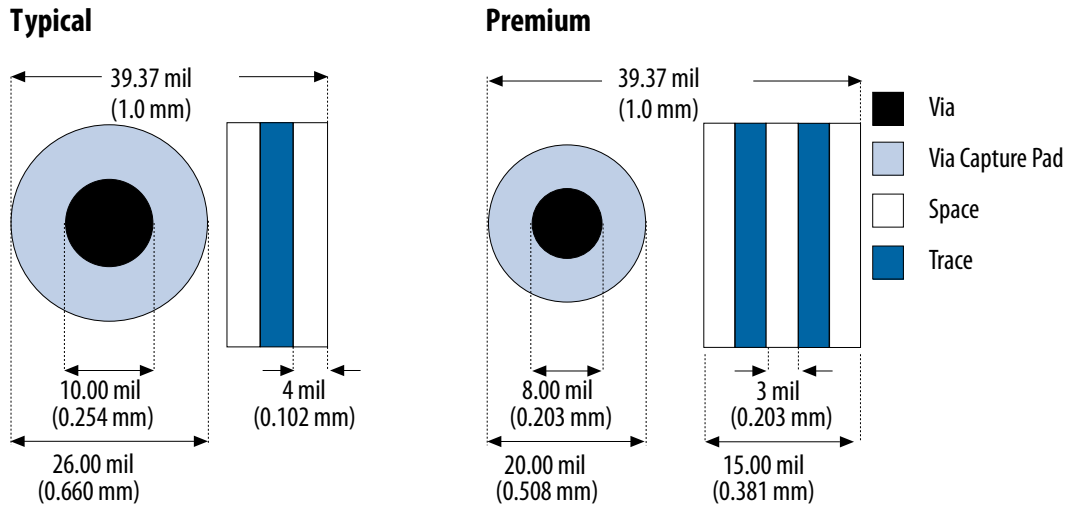
For 0.4-mm pitch, Intel recommends you to use microvia technology of 0.10-mm via drill in the pad, and route trace in the inner layers.

Via capture pad size also affects how many traces can be routed on a PCB. [Figure 13](#) on page 16 shows sample layouts of typical and premium via capture pads. The typical layout shows a via capture pad size of 0.660 mm, a via size of 0.254 mm, and an inner space and trace of 0.102 mm. With this layout, only one trace can be routed between the vias. If more traces are required, you must reduce the via capture pad size or the space and trace size.

The premium layout shows a via capture pad size of 0.508 mm, a via size of 0.203 mm, and an inner space and trace of 0.076 mm. This layout provides enough space to route two traces between the vias.

Figure 13. Typical and Premium Via Capture Pad Sizes for a 1.00-mm Flip-Chip BGA

This is not applicable for Intel Stratix 10 devices.



The following table lists the typical and premium layout specifications for a 1.00 mm Flip-Chip BGA used by most PCB vendors.

Table 7. PCB Vendor Specifications for a 1.00-mm Flip-Chip BGA

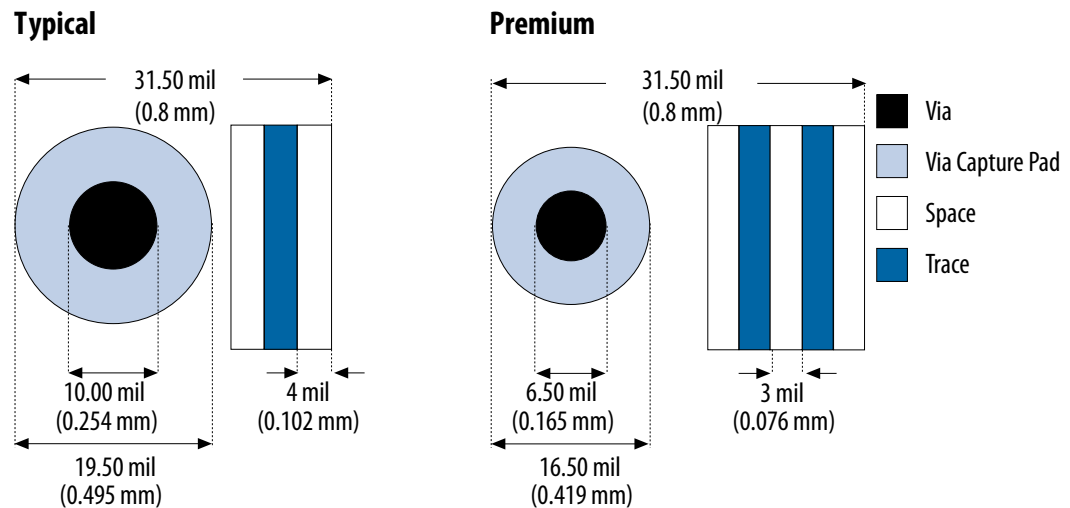
This is not applicable for Intel Stratix 10 devices.

Specification	Typical (mm)	Premium (mm) PCB Thickness >1.5 mm	Premium (mm) PCB Thickness ≤ 1.5 mm
Trace and space width	0.1/0.1	0.076/0.076	0.076/0.076
Drilled hole diameter	0.305	0.254	0.150
Finished via diameter	0.254	0.203	0.100
Via capture pad	0.660	0.508	0.275
Aspect ratio	7:1	10:1	10:1

Figure 14 on page 17 shows sample layouts of typical and premium via capture pads. The typical layout shows a via capture pad size of 0.495 mm, a via size of 0.254 mm, and an inner space and trace of 0.102 mm. With this layout, only one trace can be routed between the vias. If more traces are required, you must reduce the via capture pad size or the space and trace size.

The premium layout shows a via capture pad size of 0.419 mm, a via size of 0.165 mm, and an inner space and trace of 0.076 mm. This layout provides enough space to route two traces between the vias.

Figure 14. Typical and Premium Via Capture Pad Sizes for a 0.80-mm UBGA (BT Substrate)



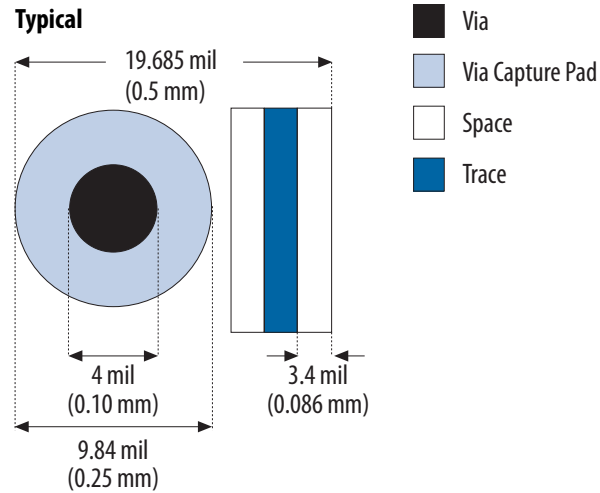
The following table lists the typical and premium layout specifications for a 0.80 mm UBGA (BT Substrate) used by most PCB vendors.

Table 8. PCB Vendor Specifications for a 0.80-mm UBGA (BT Substrate)

Specification	Typical (mm)	Premium (mm) PCB Thickness >1.5 mm	Premium (mm) PCB Thickness ≤ 1.5 mm
Trace and space width	0.1/0.1	0.076/0.076	0.076/0.076
Drilled hole diameter	0.381	0.330	0.254
Finished via diameter	0.254	0.165	0.127
Via capture pad	0.495	0.419	0.381
Aspect ratio	8:1	25:1	12:1

Figure 15 on page 18 shows sample layout of typical via capture pad. The typical layout shows a via capture pad size of 0.25 mm, a via size of 0.10 mm, and an inner space and trace of 0.068 mm.

Figure 15. Typical Via Capture Pad Size for a 0.50-mm MBGA



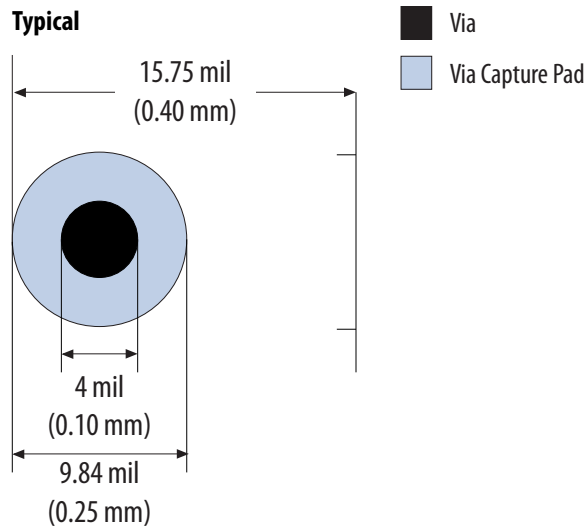
The following table lists the typical layout specifications for a 0.50-mm MBGA used by most PCB vendors.

Table 9. PCB Vendor Specification for a 0.50-mm MBGA

Specification	Typical (mm)
Trace and space width	0.086
Finished via diameter	0.10
Via capture pad	0.25

Figure 16 on page 19 shows sample layout of typical via capture pad. The typical layout shows a via capture pad size of 0.25 mm and a via size of 0.10 mm. For the 0.40-mm pitch, there is not enough space to route trace in the component layer, because the minimum trace width is 0.075 mm and the minimum gap between the trace and pad is 0.086 mm.

Figure 16. Typical Via Capture Pad Size for a 0.40-mm VBGA (also known as WLCSP)



For detailed information on drill sizes, via sizes, space and trace sizes, or via capture pad sizes, contact your PCB vendor directly.

1.3.3. Signal Line Space and Trace Width

The ability to perform escape routing is defined by the width of the trace and the minimum space required between traces. The minimum area for signal routing is the smallest area that the signal must be routed through (i.e., the distance between two vias, or g in the Escape Routing for Double and Single Traces for 1.00-mm Flip-Chip BGA figure). This area is calculated using the following formula:

$$g = (\text{BGA pitch}) - d$$

The number of traces that can be routed through this area is based on the permitted line trace and space widths. The following table shows the total number of traces that can be routed through g .

Table 10. Number of Traces

Number of Traces	Formula
1	$g \geq [2 \times (\text{space width})] + \text{trace width}$
2	$g \geq [3 \times (\text{space width})] + [2 \times (\text{trace width})]$
3	$g \geq [5 \times (\text{space width})] + [3 \times (\text{trace width})]$

The following figures show that by reducing the trace and space size, you can route more traces through g . Increasing the number of traces reduces the required number of PCB layers and decreases the overall cost.

Figure 17. Escape Routing for Double and Single Traces for 1.00-mm Flip-Chip BGA

This is not applicable for Intel Stratix 10 devices.

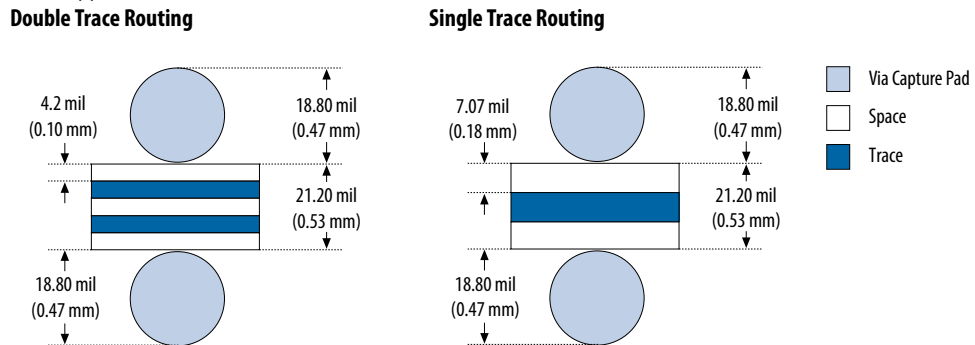


Figure 18. Escape Routing for Double and Single Traces for 0.80-mm UBGA (BT Substrate)

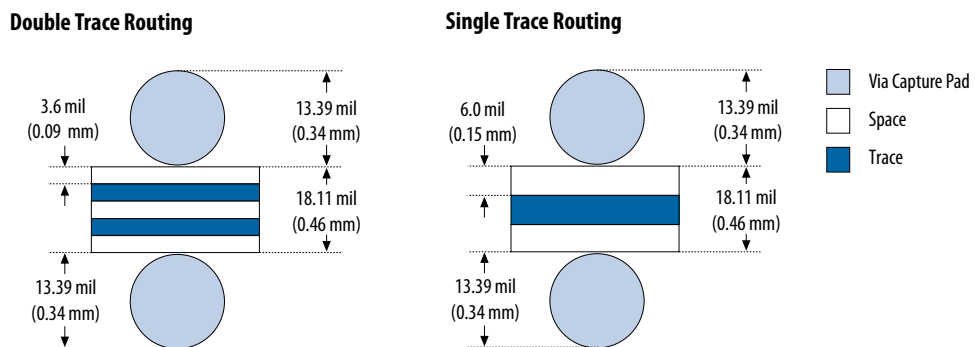
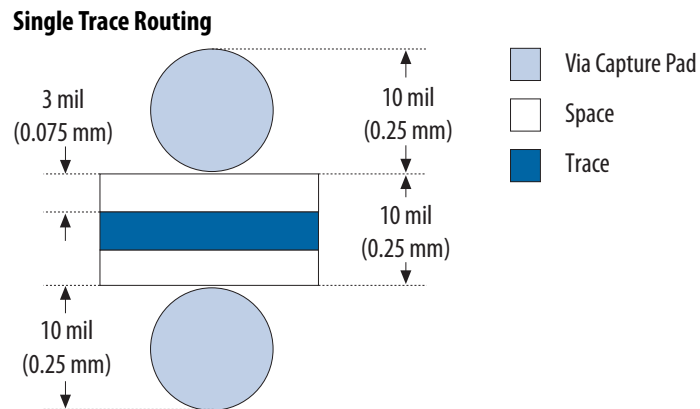


Figure 19. Escape Routing for Single Trace for 0.5-mm MBGA



1.3.4. Number of PCB Layers

In general, the number of PCB layers required to route signals is inversely proportional to the number of traces between vias (i.e., the more traces used, the fewer PCB layers required). You can estimate the number of layers your PCB requires by first determining:

- Trace and space size
- Number of traces routed between the via capture pads
- Type of vias used

Using fewer I/O pins than the maximum can reduce the required number of layers. The via type selected can also reduce the number of layers required. To see how the via type can affect the required number of PCB layers, consider the sample layouts shown in the following sections.

1.3.4.1. Sample PCB Layout for 1.00-mm Flip-Chip BGA and 0.80-mm UBGA (BT Substrate)

The blind via layout in the following figures require only two PCB layers. The signals from the first two balls can be routed directly through the first layer. The signals from the third and fourth balls can be routed through a via and out the second layer, and the signal from the fifth ball can be routed under the vias for the third and fourth balls and out the second layer. Together, only two PCB layers are required.

In contrast, the through via layout in the following figures require three PCB layers, because signals cannot be routed under through vias. The signals from the third and fourth balls can still be routed through a via and out the second layer, but the signal from the fifth ball must be routed through a via and out the third layer. Using blind vias rather than through vias in this example, saves one PCB layer.

Figure 20. Sample PCB Layout for 1.00-mm Flip-Chip BGA

This is not applicable for Intel Stratix 10 devices.

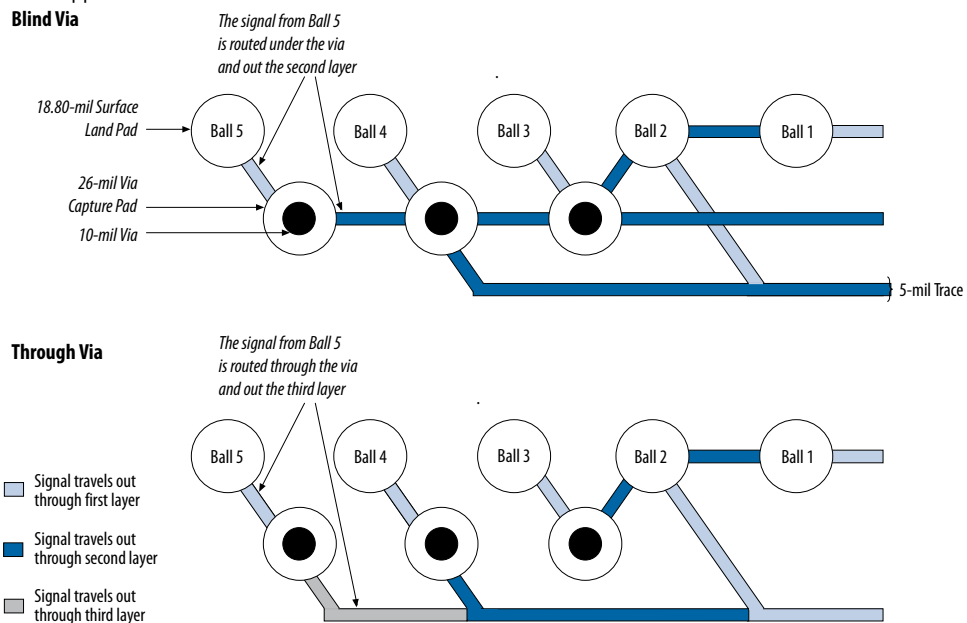
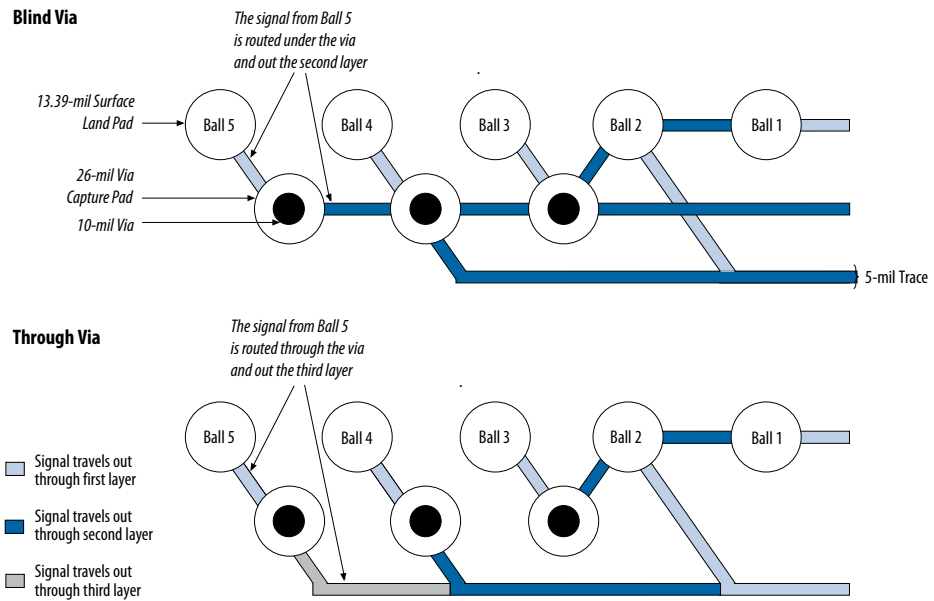


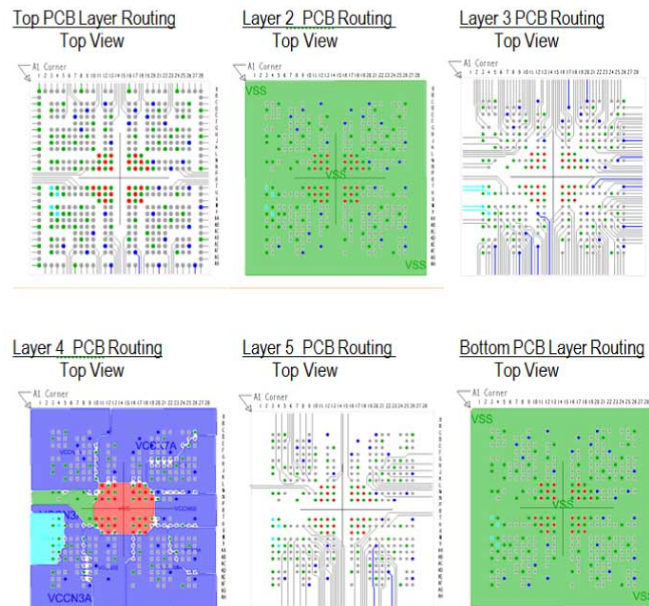
Figure 21. Sample PCB Layout for 0.80-mm UBGA (BT Substrate)



1.3.4.2. Sample PCB Routing Scheme on 6 Layers for 0.5-mm 484-pin MBGA

The following figure is the example of PCB routing scheme on 6 layers for the Cyclone V 0.5-mm 484-pin MBGA package.

Figure 22. A Sample PCB Routing Scheme on 6 Layers for 0.5-mm 484-pin MBGA



Routing Color Coding
 GREY – IO
 RED – VCCX
 GREEN – VSS
 BLUE – Common VCCN
 CYAN – VCCEN

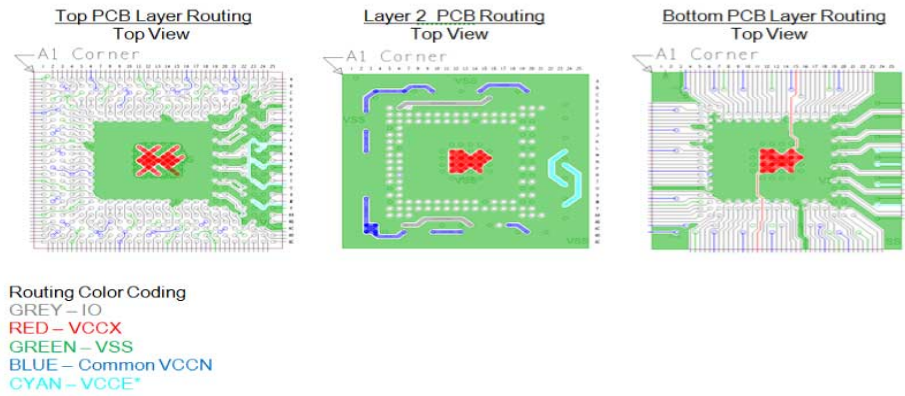
Routing Assumptions

1. Line width/space – 75 μm /75 μm (3 mils/3 mils)
2. Hole drill size – 150 μm (6 mils)
3. Via land size – 275 μm (11 mils)
4. Via land to line space – 75 μm (3 mils)

1.3.4.3. Sample PCB Routing Scheme on 3 Layers for 0.5-mm 383-pin MBGA

The following figures are the example of PCB routing schemes on 3 layers for the Cyclone V GX and Cyclone V E 0.5-mm 383-pin MBGA package.

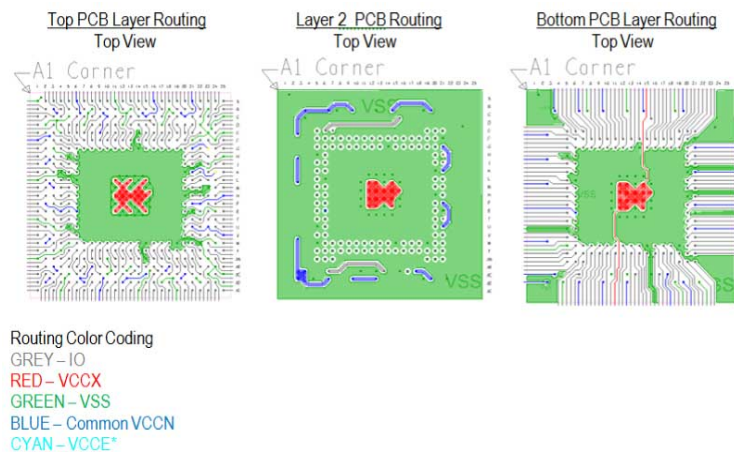
Figure 23. A Sample PCB Routing Scheme on 3 Layers for 0.5-mm 383-pin MBGA (Cyclone V GX)



Routing Assumptions

1. Line width/space – 75 μm /75 μm (3 mils/3 mils)
2. Hole drill size – 150 μm (6 mils)
3. Via land size – 275 μm (11 mils)
4. Via land to line space – 75 μm (3 mils)

Figure 24. A Sample PCB Routing Scheme on 3 Layers for 0.5-mm 383-pin MBGA (Cyclone V E)



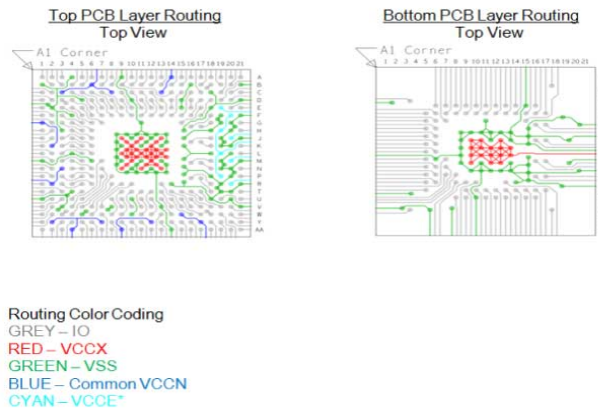
Routing Assumptions

1. Line width/space – 75 μm /75 μm (3 mils/3 mils)
2. Hole drill size – 150 μm (6 mils)
3. Via land size – 275 μm (11 mils)
4. Via land to line space – 75 μm (3 mils)

1.3.4.4. Sample PCB Routing Scheme on 2 Layers for 0.5-mm 301-pin MBGA

The following figure is the example of PCB routing scheme on 2 layers for the Cyclone V 0.5-mm 301-pin MBGA package.

Figure 25. A Sample PCB Routing Scheme on 2 Layers for 0.5-mm 301-pin MBGA



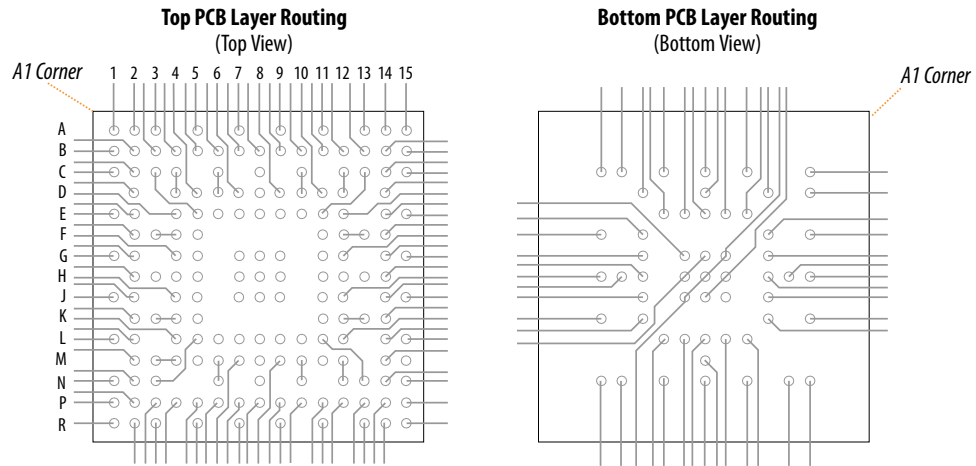
Routing Assumptions

1. Line width/space – 75 μm /75 μm (3 mils/3 mils)
2. Hole drill size – 150 μm (6 mils)
3. Via land size – 275 μm (11 mils)
4. Via land to line space – 75 μm (3 mils)

1.3.4.5. Sample PCB Routing Scheme on 2 Layers for 0.5-mm 153-pin MBGA

In 2014, M153 package is introduced in the MAX 10 device family. It has de-populated ball array with 0.5-mm ball pitch. Example of PCB routing scheme on 2 layers for 0.5-mm 153-pin MBGA is shown in the following figure.

Figure 26. A Sample PCB Routing Scheme on 2 Layers for 0.5-mm 153-pin MBGA

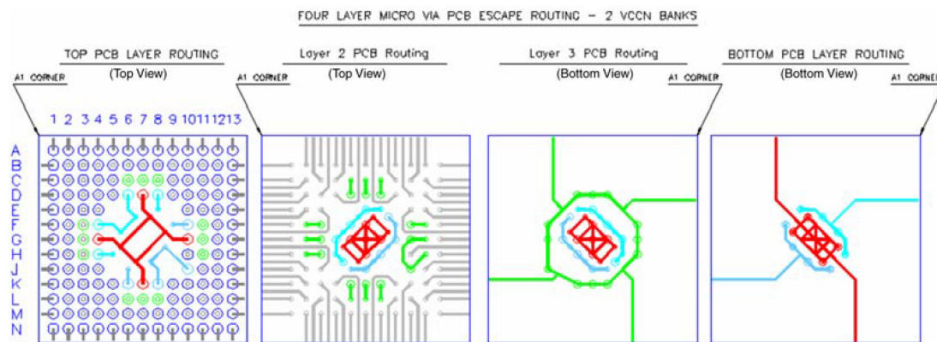


- Routing Assumptions**
1. Line width/space - 3 mils/3 mils
 2. Hole drill size - 6 mils
 3. Via land size - 11 mils
 4. Via land to line space - 3 mils

1.3.4.6. Sample PCB Routing Scheme on 4 Layers for 0.5-mm 144-pin MBGA

Example of layout scheme for routing is demonstrated for the 144-pin MBGA package in the following figure. The 144-pin package is routed in 4-layers.

Figure 27. A Sample PCB Routing Scheme on 4 Layers for 0.5-mm 144-pin MBGA



- ROUTING COLOR CODE**
 GRAY - LAYER 1 IO
 LT GRAY - Layer 2 IO
 GREEN - VSS
 RED - VCCX
 LT BLUE - VCCN1
 BLUE - VCCN2
- ROUTING ASSUMPTIONS**
- 1) Top Layer Line Width/Space - 4mils/4mils
 - 2) Layer 2 Line Width/Space - 3mils/3mils
 - 3) Micro Via Drill Size - 4mils
 - 4) PTH Drill Size - 6mils
 - 5) Micro Via/PTH/Ball Land Size - 11mils
 - 6) Via Land to Line Space - 3 mils

1.3.4.7. Sample PCB Routing Scheme on 2 Layers for 0.5-mm 256-pin and 100-pin MBGAs

In 2006, 0.5-mm pitch Micro FineLine BGA® (MBGA) packages is introduced in the MAX® II device family. The size and weight of these packages make them suitable for portable applications or any application that has board space and/or power constraints. The pin layout and the pin assignments have been designed so that the signals from solder pads can be routed in 2 layers using through-hole vias. Examples of layout schemes for routing on 2 layers is demonstrated in the following figures for the 100-pin and 256-pin MBGAs, respectively. This layout type is suitable for PCB thickness smaller than or equal to 1.5 mm. For PCB thickness greater than 1.5 mm, application of blind vias may be more suitable for escape routing. Additional MBGA packages have been added to the portfolio since 2006 and sample escape routing for these are shown in this section.

In this section, sample PCB routing schemes use VCCN and VSS. In the pin table, VCCN and VSS correspond to VCCIO and GND, respectively.

Figure 28. A Sample PCB Routing Scheme on 2 Layers for 0.5-mm 256-pin MBGA

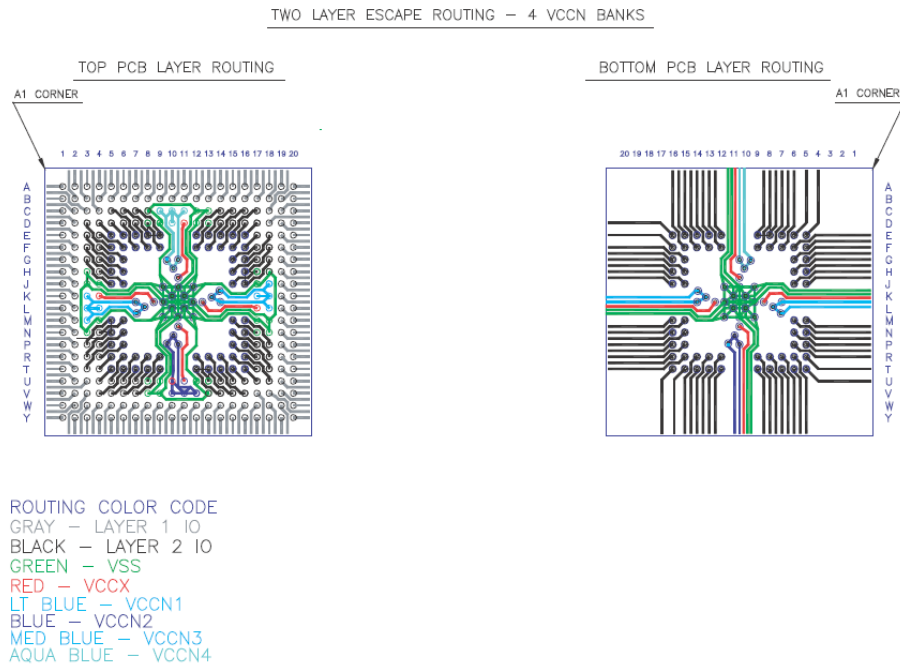
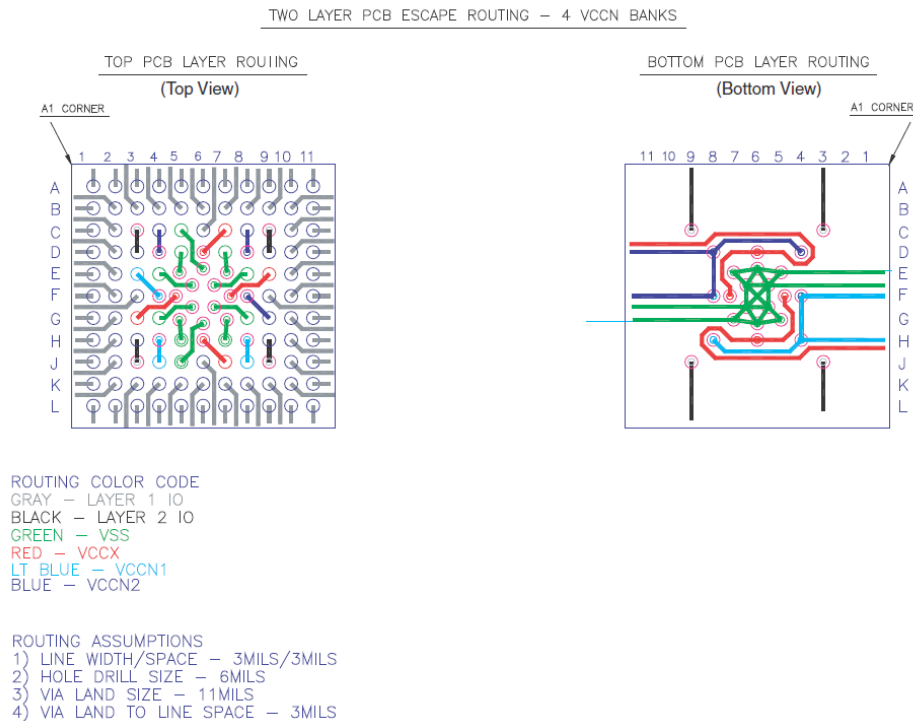


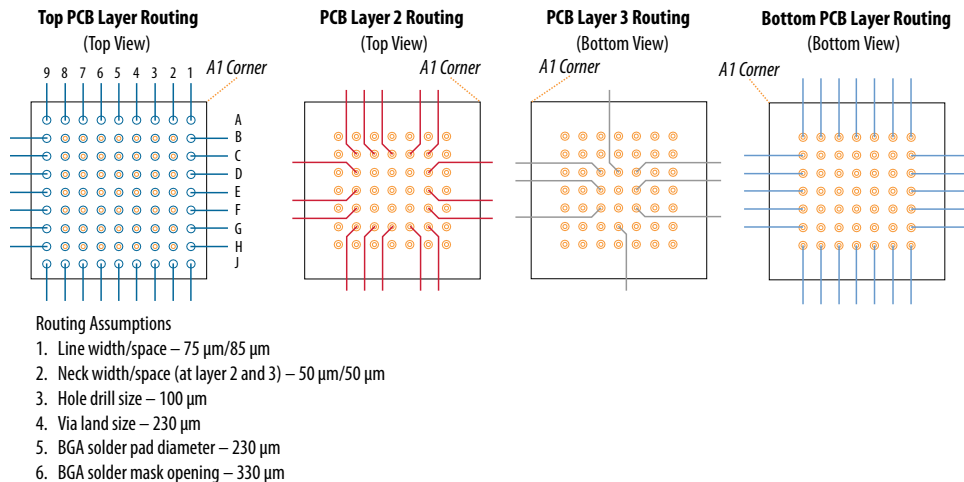
Figure 29. A Sample PCB Routing Scheme on 2 Layers for 0.5-mm 100-pin MBGA



1.3.4.8. Sample PCB Routing Scheme on 4 Layers for 0.4-mm 81-pin VBGA (also known as WLCSP)

The MAX 10 device family also introduced the first VBGA (also known as WLCSP) for 81-pin and 36-pin VBGA packages. The following figure is the example of PCB routing scheme on 4 layers for 0.4-mm 81-pin VBGA (also known as WLCSP) package.

Figure 30. A Sample PCB Routing Scheme on 4 Layers for 0.4-mm 81-pin VBGA (also known as WLCSP)



1.3.4.9. Sample PCB Routing Scheme on 2 Layers for 0.5-mm 68-pin MBGA

In 2007, 68-pin and 144-pin MBGA packages are introduced in the MAX IIZ device family. Examples of layout schemes for routing are demonstrated for 68-pin MBGA packages in the following figures. The 68-pin package is routed in 2-layers.

Figure 31. A Sample PCB Routing Scheme on 2 Layers for 0.5-mm 68-pin MBGA (Separate VCCN Banks)

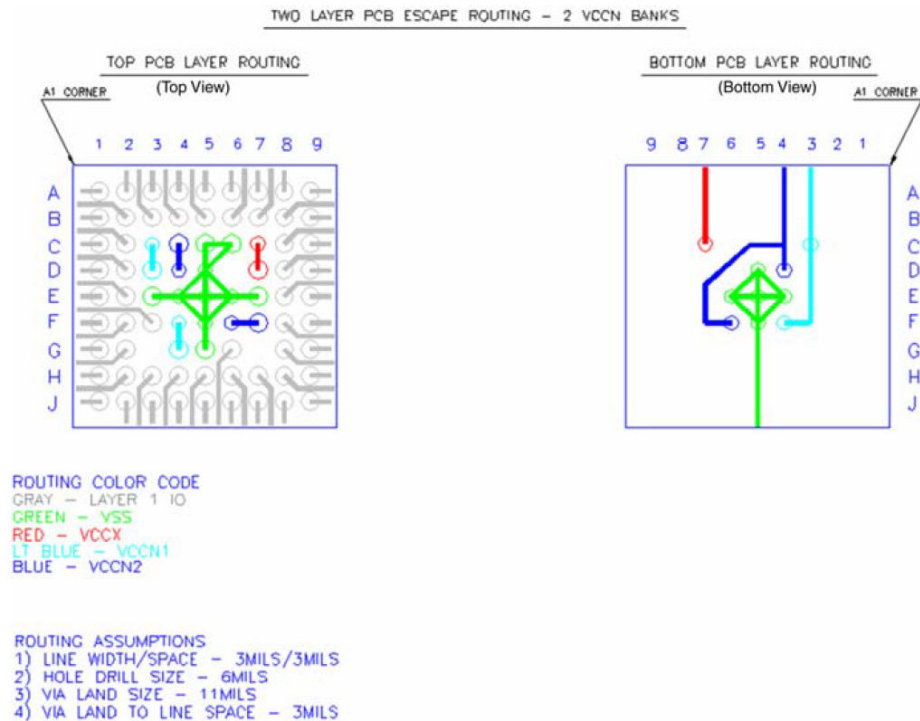
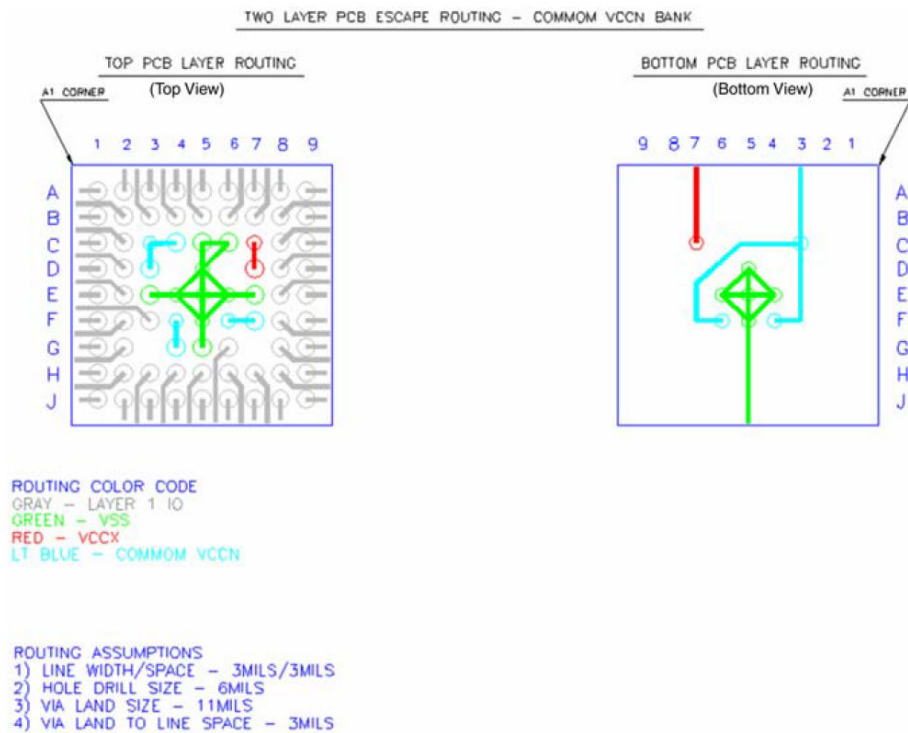


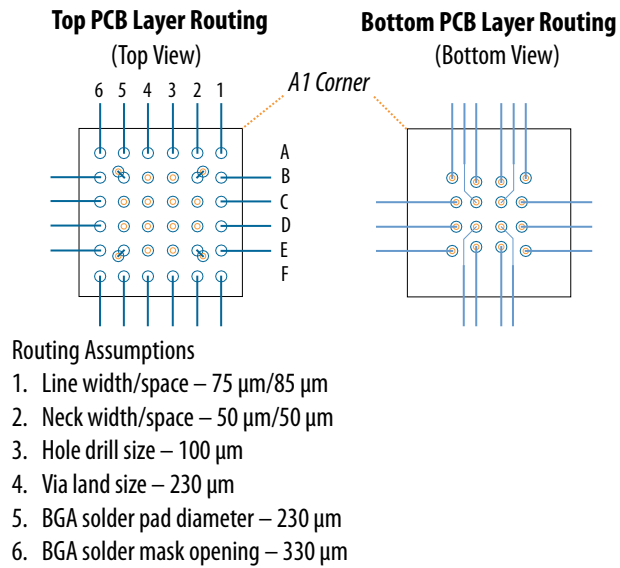
Figure 32. A Sample PCB Routing Scheme on 2 Layers for 0.5-mm 68-pin MBGA (Common VCCN Bank)



1.3.4.10. Sample PCB Routing Scheme on 2 Layers for 0.4-mm 36-pin VBGA (also known as WLCSP)

The following figure is the example of PCB routing scheme on 2 layers for 0.4-mm 36-pin VBGA (also known as WLCSP) package.

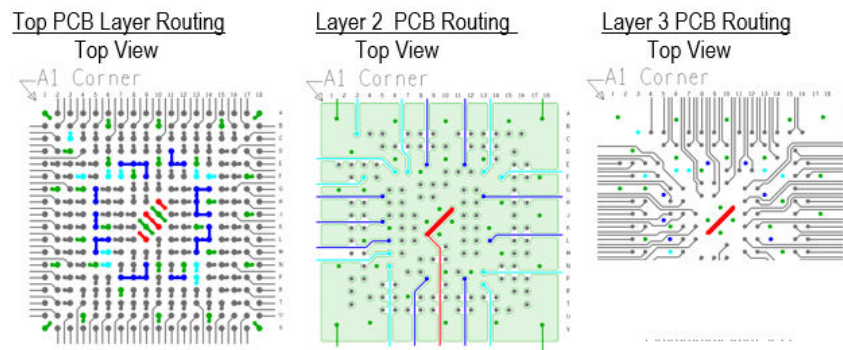
Figure 33. A Sample PCB Routing Scheme on 2 Layers for 0.4-mm 36-pin VBGA (also known as WLCSP)



1.3.4.11. Sample PCB Routing Scheme on 3 Layers for 0.8-mm 324-pin UBGA

Example of layout scheme for routing is demonstrated for the MAX 10 324-pin UBGA package in the following figure. The 324-pin package is routed in 3-layers.

Figure 34. A Sample PCB Routing Scheme on 3 Layers for 0.8-mm 324-pin UBGA



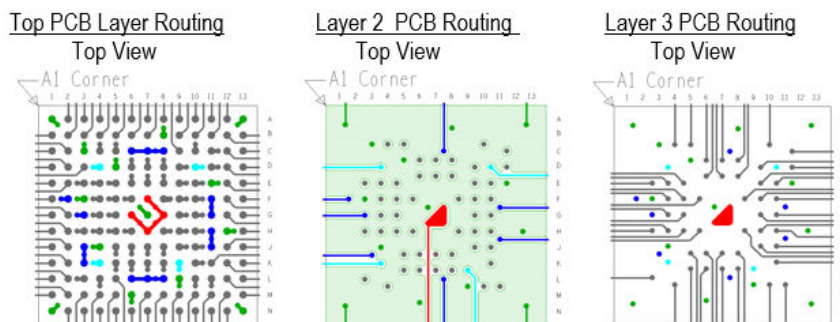
Routing Color Coding
 GREY – IO
 RED – VCC
 GREEN – VSS
 BLUE – Common VCCIO
 CYAN – Other Power

- Routing Assumptions
1. Line width/space – 100 μm /100 μm (4 mils/4 mils)
 2. Hole drill size – 150 μm (6 mils)
 3. Via land size – 300 μm (12 mils)
 4. Via land to line space – 100 μm (4 mils)

1.3.4.12. Sample PCB Routing Scheme on 3 Layers for 0.8-mm 169-pin UBGA

Example of layout scheme for routing is demonstrated for MAX 10 169-pin UBGA package in the following figure. The 169-pin package is routed in 3-layers.

Figure 35. A Sample PCB Routing Scheme on 3 layers for 0.8-mm 169-pin UBGA



Routing Color Coding
 GREY – IO
 RED – VCC
 GREEN – VSS
 BLUE – Common VCCIO
 CYAN – Other Power

- Routing Assumptions
1. Line width/space – 100 µm/100 µm (4 mils/4 mils)
 2. Hole drill size – 150 µm (6 mils)
 3. Via land size – 300 µm (12 mils)
 4. Via land to line space – 100 µm (4 mils)

1.4. Document Revision History for AN 114: Board Design Guidelines for Intel Programmable Device Packages

Document Version	Changes
2022.05.27	Removed instances of Enpirion from AN 114: Board Design Guidelines for Intel® Programmable Device Packages section.
2019.12.31	Added reference links to the following documents: <ul style="list-style-type: none"> • AN 766: Intel Stratix 10 Devices, High Speed Signal Interface Layout Design Guideline • AN 875: Intel Stratix 10 E-Tile PCB Design Guidelines
2019.04.02	Updated the link for the Manufacturing with Intel Stratix 10 Field Programmable Gate Arrays document.
2018.10.09	<ul style="list-style-type: none"> • Removed Intel Stratix 10 information. For more information about Intel Stratix 10 packages and beyond, refer to the respective individual Manufacturing Advantage Services (MAS) Guidelines document. • Updated the Recommended Pad Sizes for SMD and NSMD Pads table to include 0.80mm UBGA (flip-chip) information.
2018.03.01	<ul style="list-style-type: none"> • Rebranded as Intel. • Renamed the document as Board Design Guidelines for Intel Programmable Device Packages. • Corrected BGA pad opening (A) size of the 0.50 mm MBGA in "Recommended Pad Sizes for SMD and NSMD Pads" table from 0.40 mm to 0.30 mm.

Date	Version	Changes
February 2017	2017.02.24	<ul style="list-style-type: none"> Added the Sample PCB Routing Scheme on 3 Layers for 0.8-mm 169-pin UBGA section. Added the Sample PCB Routing Scheme on 3 Layers for 0.8-mm 324-pin UBGA section. Updated the Recommended Stratix 10 Stencil Design for the NF43, UF50, and HF55 Package figures. Editorial fix to the Surface Land Pad Dimension section. Editorial fix to the Via Capture Pad Layout and Dimension section. Editorial fix to the Recommended Stratix 10 Pad Pattern (PCB Side) section. Minor text edits.
November 2016	2016.11.23	<ul style="list-style-type: none"> Added the Recommended Stratix 10 Pad Pattern (PCB Side) section. Added the Stratix 10 PCB Manufacturing Recommendation section. Added the Sample PCB Routing Scheme on 2 Layers for 0.5-mm 301-pin MBGA section. Added the Sample PCB Routing Scheme on 3 Layers for 0.5-mm 383-pin MBGA section. Added the Sample PCB Routing Scheme on 6 Layers for 0.5-mm 484-pin MBGA section. Added the NSMD and SMD Pads for Stratix 10 Devices figure. Added the Recommended Pad Sizes for Stratix 10 Devices table to include 1.00 mm (flip-chip) for Stratix 10 devices.
December 2014	2014.12.15	<ul style="list-style-type: none"> Added the Recommended Pad Sizes for WLCSP table. Added the Formula for Via Layouts for 0.5-mm MBGA Land Pads table. Added the Formula for Via Layouts for 0.4-mm VBGA Land Pads table. Added the PCB Vendor Specification for a 0.50-mm MBGA table. Added the PCB Vendor Specification for a 0.40-mm VBGA table. Added the Via and Routing Space Available for 0.50-mm MBGA NSMD Land Pads figure. Added the Placement of Via Capture Pad for 0.5-mm MBGA Land Pads figure. Added the Placement of Via Capture Pad for 0.4-mm VBGA Land Pads figure. Added the Typical Via Capture Pad Size for a 0.50-mm MBGA figure. Added the Typical Via Capture Pad Size for a 0.40-mm VBGA figure. Added the Escape Routing for Single Trace for 0.5-mm MBGA figure. Updated the Via and Routing Space Available for 0.80-mm UBGA (BT Substrate) NSMD Land Pads figure.
continued...		

Date	Version	Changes
September 2014	5.3	<ul style="list-style-type: none"> • Dimensions in mm are added to respective figures. • PCB Vendor Specifications for 0.80-mm UBGA (BT Substrate) were updated. • Sample PCB Routing Scheme on 2 Layers for 0.5mm 153-pin MBGA was added. • Sample PCB Routing Scheme on 4 Layers for 0.4mm 81-pin VBGA was added. • Sample PCB Routing Scheme on 2 Layers for 0.4mm 36-pin VBGA was added.
January 2014	5.2	0.80-mm UBGA (BT Substrate) package was added.
December 2007	5.1	Additional samples were added in "Number of PCB Layers" on page 15.
May 2007	5.0	<ul style="list-style-type: none"> • Updated Table 3 to include pad recommendations for 0.5 mm MBGA. • Updated Table 6 to reflect the current PCB vendor capability. • Added the MBGA update to "Number of PCB Layers" on page 15 section. • Added Figures 16 and 17.
February 2006	4.0	Changed name of document to Designing With High-Density BGA Packages for Altera Devices from Designing With FineLine BGA Packages for APEX, FLEX, ACEX, MAX 7000 & MAX 3000 Devices.