13. IEEE 1149.1 (JTAG) Boundary-Scan Testing for MAX II Devices

MII51014-1.7

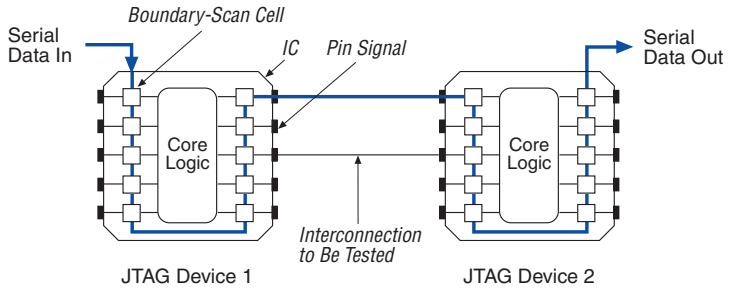
Introduction

As printed circuit boards (PCBs) become more complex, the need for thorough testing becomes increasingly important. Advances in surface-mount packaging and PCB manufacturing have resulted in smaller boards, making traditional test methods (for example, external test probes and "bed-of-nails" test fixtures) harder to implement. As a result, cost savings from PCB space reductions are sometimes offset by cost increases in traditional testing methods.

In the 1980s, the Joint Test Action Group (JTAG) developed a specification for boundary-scan testing that was later standardized as the IEEE Std. 1149.1 specification. This boundary-scan test (BST) architecture offers the capability to efficiently test components on PCBs with tight lead spacing.

This BST architecture can test pin connections without using physical test probes and capture functional data while a device is operating normally. Boundary-scan cells in a device can force signals onto pins, or capture data from pin or core logic signals. Forced test data is serially shifted into the boundary-scan cells. Captured data is serially shifted out and externally compared to expected results. Figure 13–1 shows the concept of boundary-scan testing.

Figure 13–1. IEEE Std. 1149.1 Boundary-Scan Testing



This chapter discusses how to use the IEEE Std. 1149.1 BST circuitry in MAX® II devices. The topics are as follows:

In addition to BST, you can use the IEEE Std. 1149.1 controller for in-system programming for MAX II devices. MAX II devices support IEEE 1532 programming, which utilizes the IEEE Std. 1149.1 Test Access Port (TAP) interface. However, this chapter only discusses the BST feature of the IEEE Std. 1149.1 circuitry.

IEEE Std. 1149.1 BST Architecture

A MAX II device operating in IEEE Std. 1149.1 BST mode uses four required pins, TDI, TDO, TMS, and TCK. Table 13–1 summarizes the functions of each of these pins. MAX II devices do not have a TRST pin.

Table 13–1. EEE Std. 1149.1 Pin Descriptions

Pin	Description	Function
TDI *(1)*	Test data input	Serial input pin for instructions as well as test and programming data. Data is shifted in on the rising edge of TCK.
TDO	Test data output	Serial data output pin for instructions as well as test and programming data. Data is shifted out on the falling edge of TCK. The pin is tri-stated if data is not being shifted out of the device.
TMS *(1)*	Test mode select	Input pin that provides the control signal to determine the transitions of the TAP controller state machine. Transitions within the state machine occur at the rising edge of TCK. Therefore, TMS must be set up before the rising edge of TCK. TMS is evaluated on the rising edge of TCK.
TCK *(2)*	Test clock input	The clock input to the BST circuitry. Some operations occur at the rising edge, while others occur at the falling edge.

Notes to Table 13–1:

(1) The TDI and TMS pins have internal weak pull-up resistors.

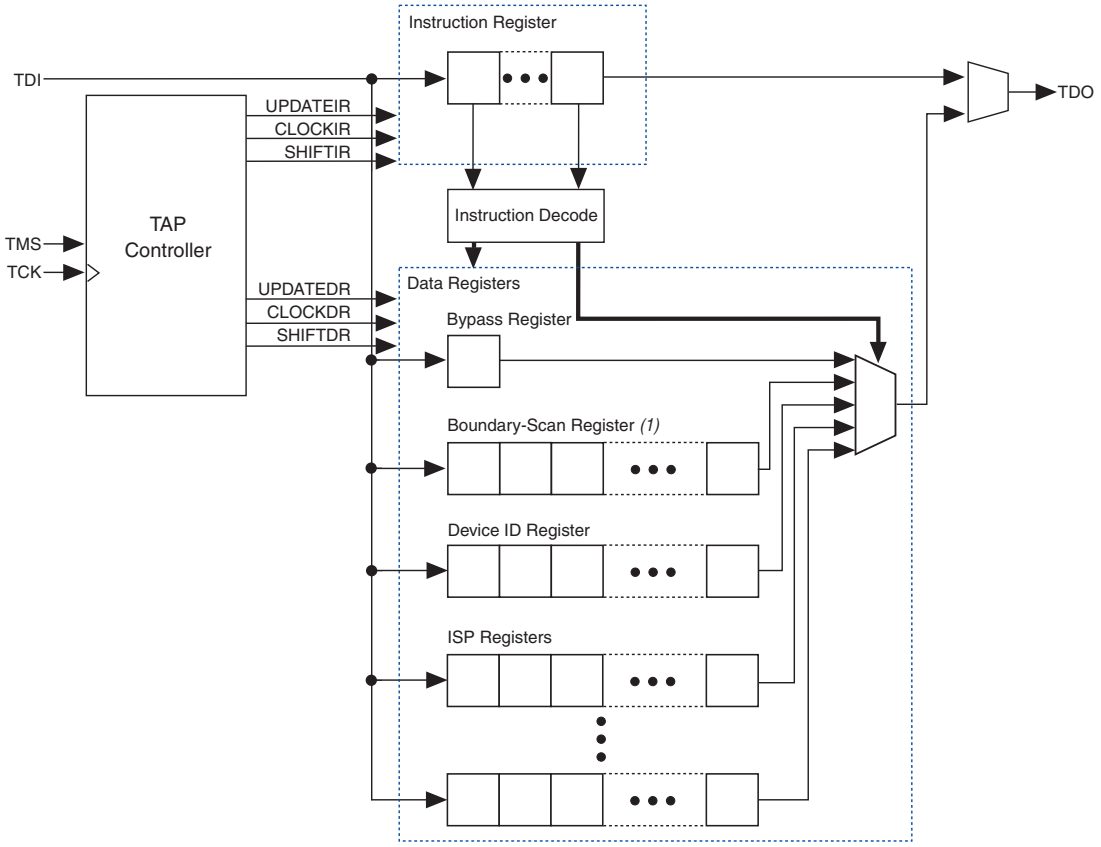
(2) The TCK pin has an internal weak pull-down resistor.

The IEEE Std. 1149.1 BST circuitry requires the following registers:

- The instruction register, which is used to determine the action to be performed and the data register to be accessed.
- The bypass register, which is a 1-bit-long data register used to provide a minimum-length serial path between TDI and TDO.
- The boundary-scan register that is a shift register composed of all the boundary-scan cells of the device.

Figure 13–2 shows a functional model of the IEEE Std. 1149.1 circuitry.

Figure 13–2. IEEE Std. 1149.1 Circuitry



Note to Figure 13–2:

(1) Refer to the *JTAG and In-System Programmability* chapter in the *MAX II Device Handbook* for the boundary-scan register length in MAX II devices.

IEEE Std. 1149.1 boundary-scan testing is controlled by a TAP controller, which is described in "IEEE Std. 1149.1 BST Operation Control" on page 13–6. The TMS and TCK pins operate the TAP controller, and the TDI and TDO pins provide the serial path for the data registers. The TDI pin also provides data to the instruction register, which then generates control logic for the data registers.

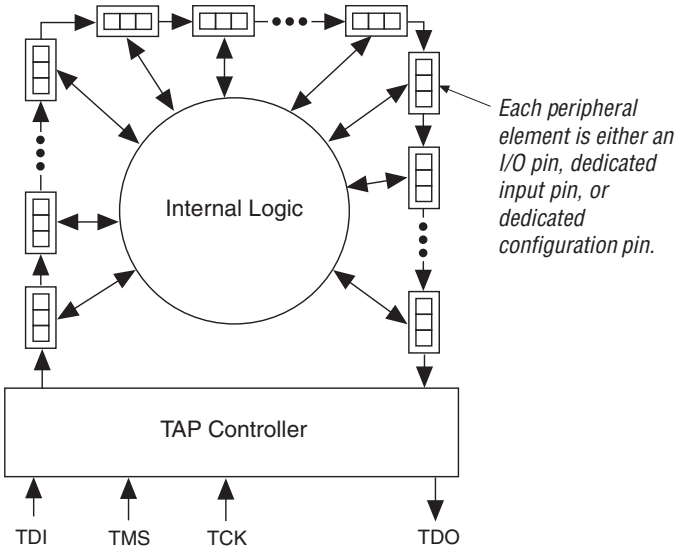
IEEE Std. 1149.1 Boundary-Scan Register

The boundary-scan register is a large serial shift register that uses the TDI pin as an input and the TDO pin as an output. The boundary-scan register consists of 3-bit peripheral elements that are associated with I/O pins of the MAX II devices. You can use the boundary-scan register to test external pin connections or to capture internal data.

Refer to *the JTAG and In-System Programmability* chapter in the *MAX II Device Handbook* for the boundary-scan register length of MAX II devices.

Figure 13–3 shows how test data is serially shifted around the periphery of the IEEE Std. 1149.1 device.

Figure 13–3. Boundary-Scan Register



Boundary-Scan Cells of a MAX II Device I/O Pin

Except for the four JTAG pins and power pins, all pins of a MAX II device (including clock pins) can be used as user I/O pins and have a boundary-scan cell (BSC). The 3-bit BSC consists of a set of capture registers and a set of update registers. The capture registers can connect to internal device data via the OUTJ and OEJ signals, while the update registers connect to external data through the PIN_OUT and PIN_OE signals. The global control signals for the IEEE Std. 1149.1 BST registers (for example, SHIFT, CLOCK, and UPDATE) are generated internally by the TAP controller; the MODE signal is generated by a decode of the instruction register. The data signal path for the boundary-scan register runs from the serial data in (SDI) signal to the serial data out (SDO) signal. The scan register begins at the TDI pin and ends at the TDO pin of the device.

Figure 13–4 shows the User I/O Boundary-Scan Cell of MAX II devices.

Figure 13–4. MAX II Device's User I/O BSC with IEEE Std. 1149.1 BST Circuitry

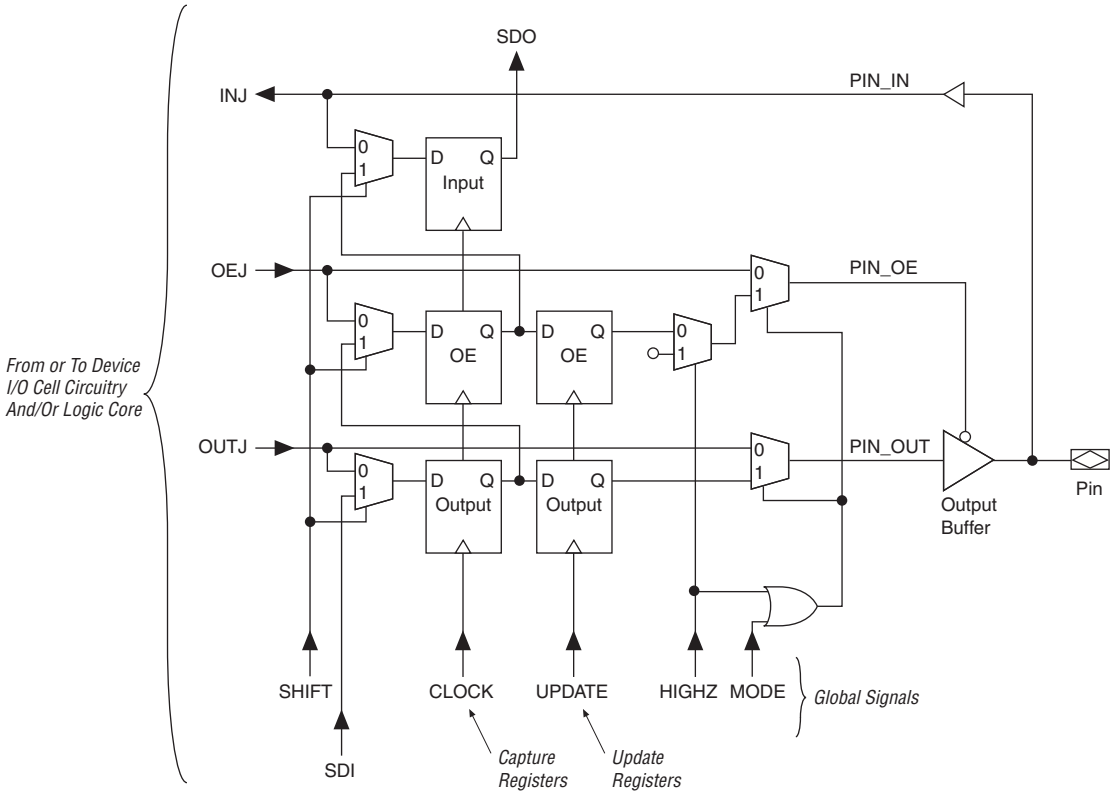


Table 13–2 describes the capture and update register capabilities of all boundary-scan cells within MAX II devices.

Table 13–2. MAX II Device's Boundary-Scan Cell Descriptions *(Note 1)*

Pin Type	Captures			Drives			Notes
	Output Capture Register	OE Capture Register	Input Capture Register	Output Update Register	OE Update Register	Input Update Register	
User I/O	OUTJ	OEJ	PIN_IN	PIN_OUT	PIN_OE	—	Includes User Clocks

Note to Table 13–2:

(1) TDI, TDO, TMS, and TCK pins, and all VCC and GND pin types do not have boundary-scan cells.

JTAG Pins and Power Pins

MAX II devices do not have boundary-scan cells for the dedicated JTAG pins (TDI, TDO, TMS, and TCK) and power pins (VCCINT, VCCIO, GNDINT, and GNDIO).

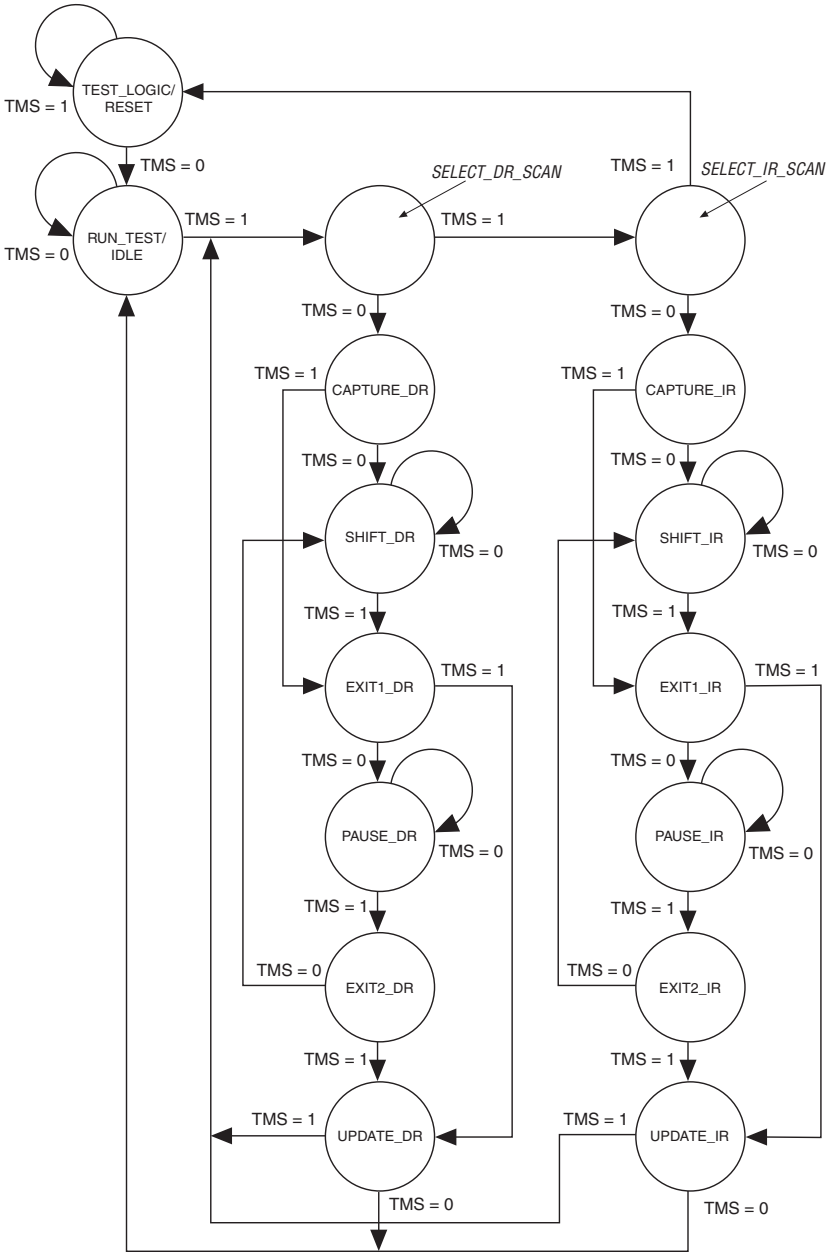
IEEE Std. 1149.1 BST Operation Control

MAX II devices implement the following IEEE Std. 1149.1 BST instructions: SAMPLE/PRELOAD, EXTEST, BYPASS, IDCODE, USERCODE, CLAMP, and HIGHZ. The length of the BST instructions is 10 bits. These instructions are described in detail later in this chapter.

Refer to *the JTAG and In-System Programmability* chapter in the *MAX II Device Handbook* for a summary of the BST instructions and their instruction codes.

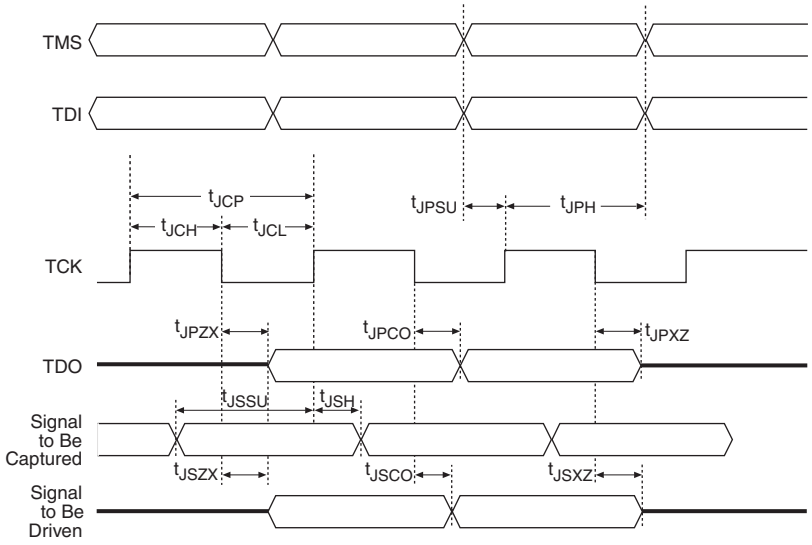
The IEEE Std. 1149.1 TAP controller, a 16-state state machine clocked on the rising edge of TCK, uses the TMS pin to control IEEE Std. 1149.1 operation in the device. Figure 13–5 shows the TAP controller state machine.

Figure 13–5. IEEE Std. 1149.1 TAP Controller State Machine



When the TAP controller is in the TEST_LOGIC/RESET state, the BST circuitry is disabled, the device is in normal operation, and the instruction register is initialized with IDCODE as the initial instruction. At device power-up, the TAP controller starts in this TEST_LOGIC/RESET state. In addition, the TAP controller may be forced to the TEST_LOGIC/RESET state by holding TMS high for five TCK clock cycles. Once in the TEST_LOGIC/RESET state, the TAP controller remains in this state as long as TMS continues to be held high while TCK is clocked. Figure 13–6 shows the timing requirements for the IEEE Std. 1149.1 signals.

Figure 13–6. IEEE Std. 1149.1 Timing Waveforms *(Note 1)*

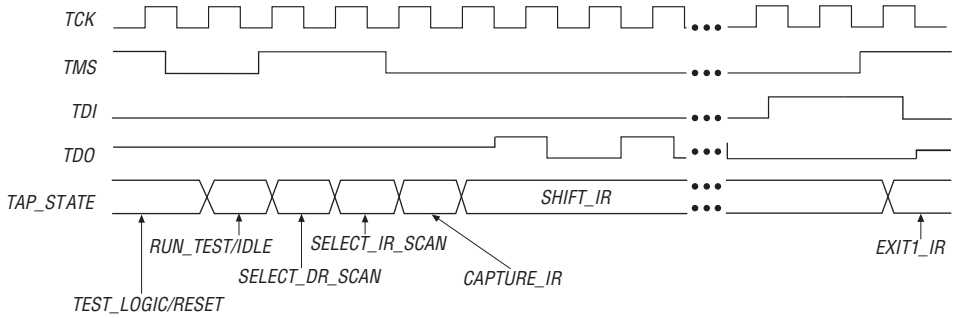


Note to Figure 13–6:

(1) For timing parameter values, refer to the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*.

To start IEEE Std. 1149.1 operation, select an instruction mode by advancing the TAP controller to the shift instruction register (SHIFT_IR) state and shift in the appropriate instruction code on the TDI pin. The waveform diagram in Figure 13–7 represents the entry of the instruction code into the instruction register. It shows the values of TCK, TMS, TDI, and TDO and the states of the TAP controller. From the RESET state, TMS is clocked with the pattern 01100 to advance the TAP controller to SHIFT_IR.

Figure 13–7. Selecting the Instruction Mode



The TDO pin is tri-stated in all states except the SHIFT_IR and SHIFT_DR states. The TDO pin is activated at the first falling edge of TCK after entering either of the shift states and is tri-stated at the first falling edge of TCK after leaving either of the shift states.

When the SHIFT_IR state is activated, TDO is no longer tri-stated, and the initial state of the instruction register is shifted out on the falling edge of TCK. TDO continues to shift out the contents of the instruction register as long as the SHIFT_IR state is active. The TAP controller remains in the SHIFT_IR state as long as TMS remains low.

During the SHIFT_IR state, an instruction code is entered by shifting data on the TDI pin on the rising edge of TCK. The last bit of the opcode must be clocked at the same time that the next state, EXIT1_IR, is activated; EXIT1_IR is entered by clocking a logic high on TMS. Once in the EXIT1_IR state, TDO becomes tri-stated again. TDO is always tri-stated except in the SHIFT_IR and SHIFT_DR states. After an instruction code is entered correctly, the TAP controller advances to perform the serial shifting of test data in one of three modes—SAMPLE/PRELOAD, EXTEST, or BYPASS—that are described below.

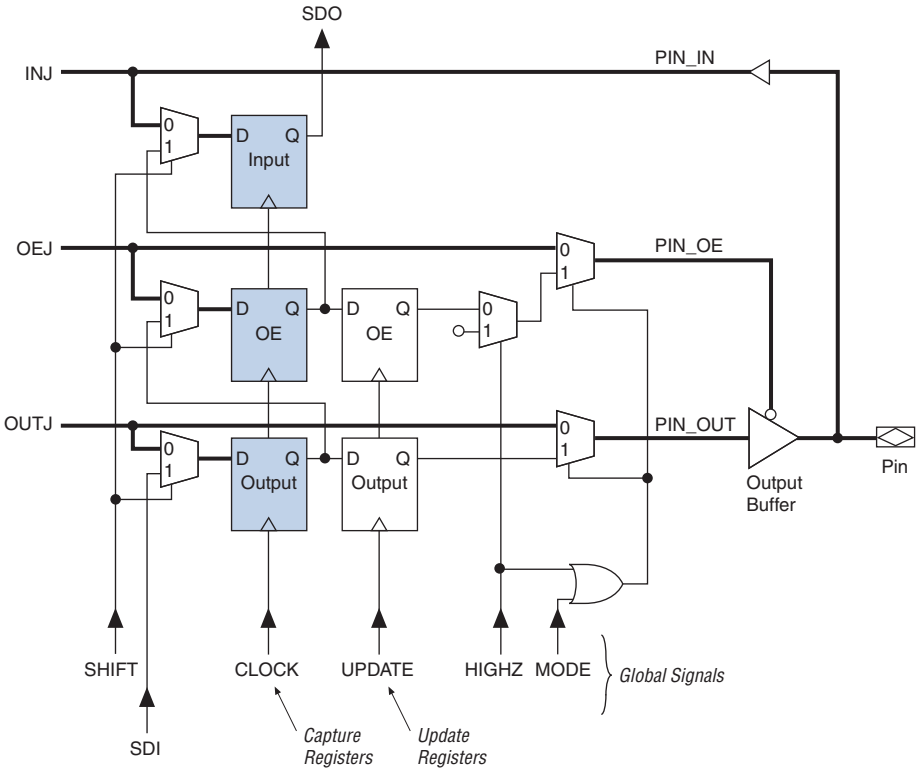
For MAX II devices, there are weak pull-up resistors for TDI and TMS, and pull-down resistors for TCK. However, in a JTAG chain, there might be some devices that do not have internal pull-up or pull-down resistors. In this case, Altera recommends pulling the TMS pin high (through an external 10-kΩ resistor), and pulling TCK low (through an external 1-kΩ resistor) during BST or in-system programmability (ISP) to prevent the TAP controller from going into an unintended state. Pulling-up the TDI signal externally for the MAX II device is optional.

For more information about the pull-up and pull-down resistors, refer to the *In-System Programmability Guidelines for MAX II Devices* chapter in the *MAX II Device Handbook*.

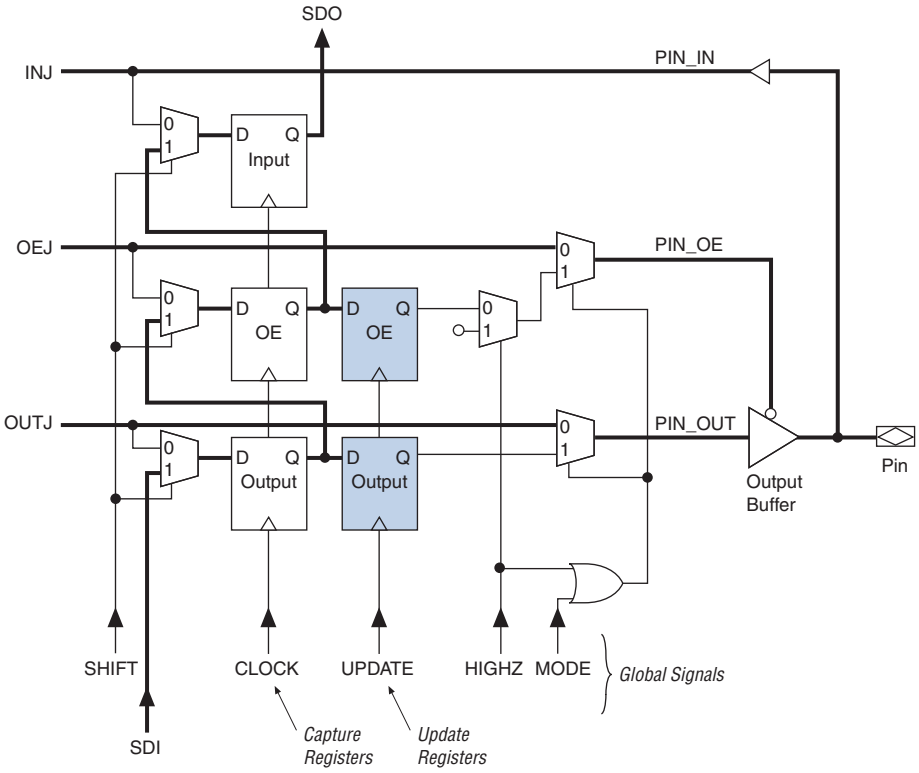
SAMPLE/PRELOAD Instruction Mode

The SAMPLE/PRELOAD instruction mode allows you to take a snapshot of device data without interrupting normal device operation. However, this instruction mode is most often used to preload the test data into the update registers prior to loading the EXTEST instruction. Figure 13–8 shows the capture, shift, and update phases of the SAMPLE/PRELOAD mode.

Figure 13–8. IEEE Std. 1149.1 BST SAMPLE/PRELOAD Mode



(Capture Phase)



(Shift and Update Phase)

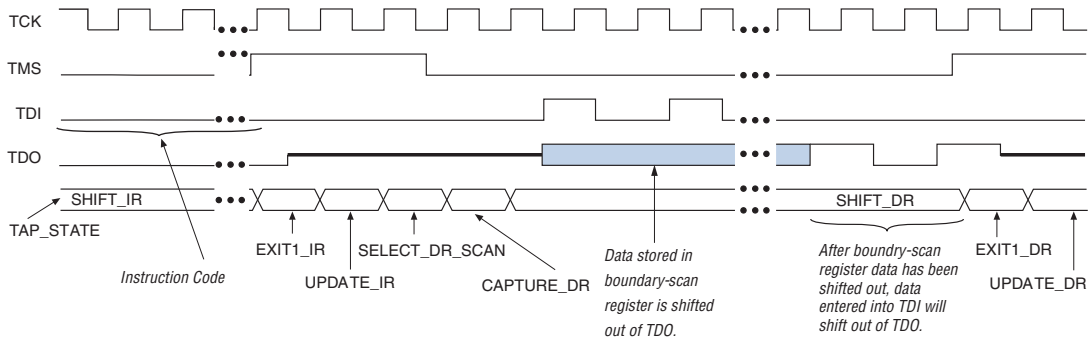
During the capture phase, multiplexers preceding the capture registers select the active device data signals; this data is then clocked into the capture registers. The multiplexers at the outputs of the update registers also select active device data to prevent functional interruptions to the device. During the shift phase, the boundary-scan shift register is formed by clocking data through capture registers around the device periphery and then out of the TDO pin. New test data can simultaneously be shifted into TDI and replace the contents of the capture registers. During the update phase, data in the capture registers is transferred to the update registers. This data can then be used in the EXTEST instruction mode.

Refer to "EXTEST Instruction Mode" on page 13–11 for more information.

Figure 13–9 shows the SAMPLE/PRELOAD waveforms. The SAMPLE/PRELOAD instruction code is shifted in through the TDI pin. The TAP controller advances to the CAPTURE_DR state and then to the SHIFT_DR state, where it remains if TMS is held low. The data shifted out of the TDO pin consists of the data that was present in the capture registers after the capture phase. New test data shifted into the TDI pin appears at the TDO pin after being clocked through the entire boundary-scan register. Figure 13–9 shows that the test data that shifted into TDI does not appear at the TDO pin until after the capture register data that is shifted out. If TMS is held high on two consecutive TCK clock cycles, the TAP controller advances to the UPDATE_DR state for the update phase.

If the device output enable feature is enabled but the DEV_OE pin is not asserted during boundary-scan testing, the OE boundary-scan registers of the boundary-scan cells capture data from the core of the device during SAMPLE/PRELOAD. These values are not high impedance, although the I/O pins are tri-stated.

Figure 13–9. SAMPLE/PRELOAD Shift Data Register Waveforms

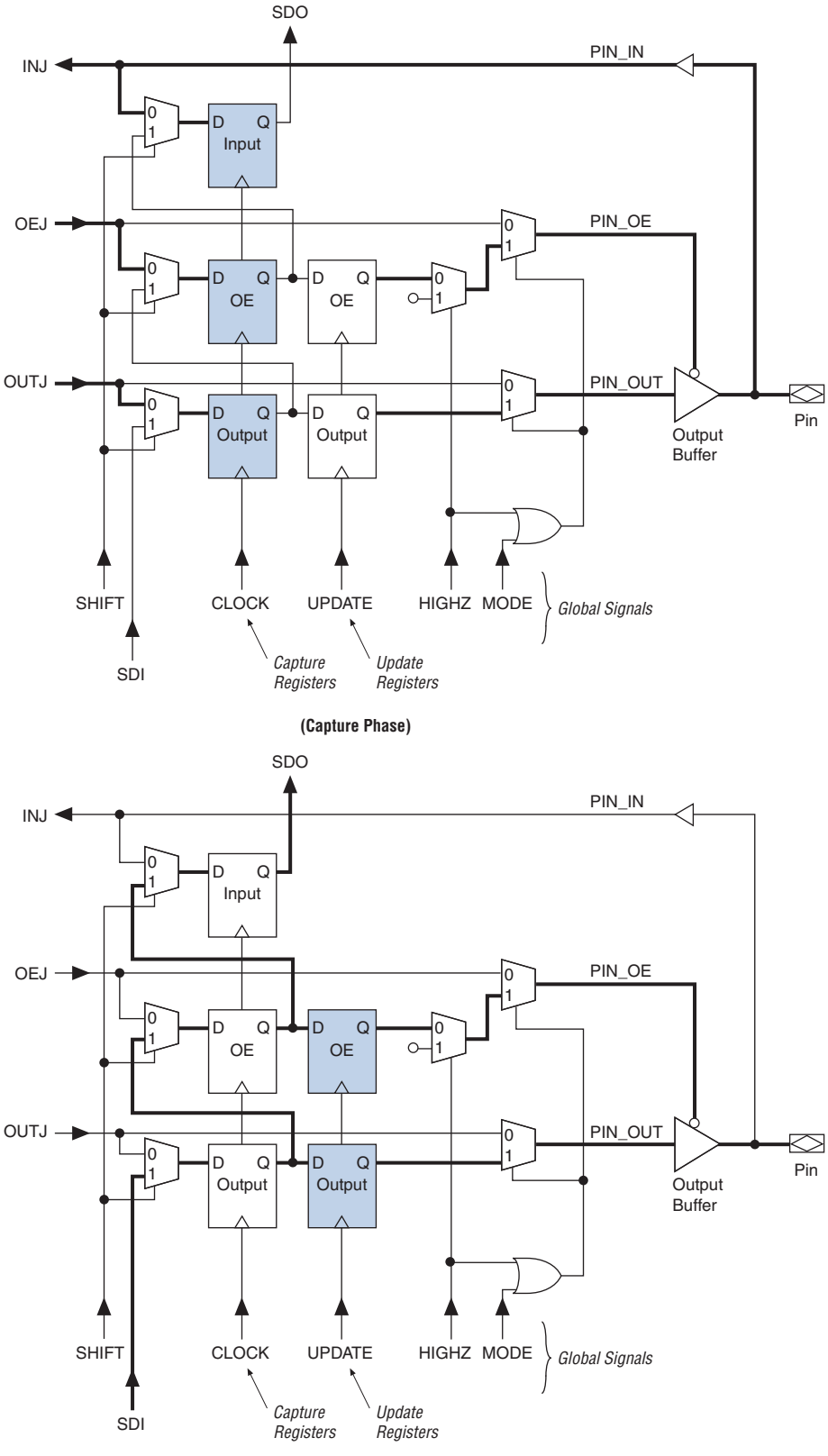


EXTEST Instruction Mode

The EXTEST instruction mode is used primarily to check external pin connections between devices. Unlike the SAMPLE/PRELOAD mode, EXTEST allows test data to be forced onto the pin signals. By forcing known logic high and low levels on output pins, opens and shorts can be detected at pins of any device in the scan chain.

Figure 13–10 shows the capture, shift, and update phases of the EXTEST mode.

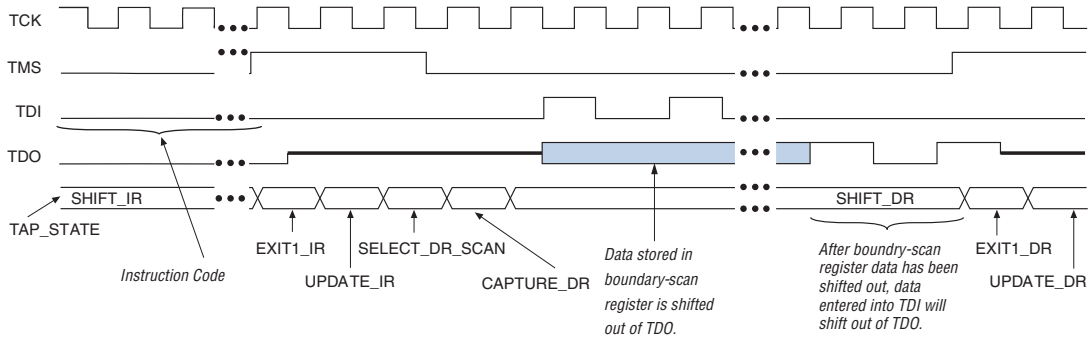
Figure 13–10. IEEE Std. 1149.1 BST EXTEST Mode



EXTEST selects data differently than SAMPLE/PRELOAD. EXTEST chooses data from the update registers as the source of the output and output enable signals. Once the EXTEST instruction code is entered, the multiplexers select the update register data; thus, data stored in these registers from a previous EXTEST or SAMPLE/PRELOAD test cycle can be forced onto the pin signals. In the capture phase, the results of this test data are stored in the capture registers and then shifted out of TDO during the shift phase. New test data can then be stored in the update registers during the update phase.

The waveform diagram in Figure 13–11 resembles the SAMPLE/PRELOAD waveform diagram, except that the instruction code for EXTEST is different. The data shifted out of TDO consists of the data that was present in the capture registers after the capture phase. New test data shifted into the TDI pin appears at the TDO pin after being clocked through the entire boundary-scan register.

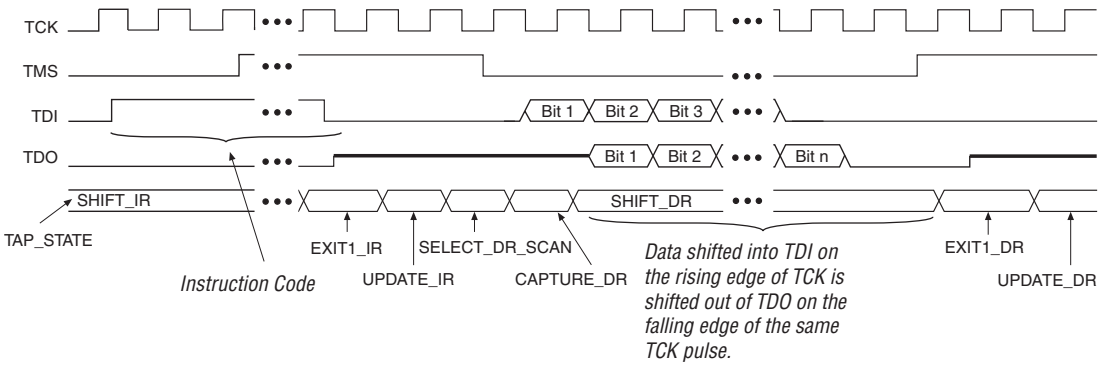
Figure 13–11. EXTEST Shift Data Register Waveforms



BYPASS Instruction Mode

The BYPASS instruction mode is activated with an instruction code made up of only ones. The waveforms in Figure 13–12 show how scan data passes through a device once the TAP controller is in the SHIFT_DR state. In this state, data signals are clocked into the bypass register from TDI on the rising edge of TCK and out of TDO on the falling edge of the same clock pulse.

Figure 13–12. BYPASS Shift Data Register Waveforms



IDCODE Instruction Mode

The IDCODE instruction mode is used to identify the devices in an IEEE Std. 1149.1 chain. When IDCODE is selected, the device identification register is loaded with the 32-bit vendor-defined identification code. The device ID register is connected between the TDI and TDO ports, and the device IDCODE is shifted out.

The IDCODE for MAX II devices are listed in the *JTAG and In-System Programmability* chapter in the *MAX II Device Handbook*.

USERCODE Instruction Mode

The USERCODE instruction mode is used to examine the user electronic signature (UES) within the devices along an IEEE Std. 1149.1 chain. When this instruction is selected, the device identification register is connected between the TDI and TDO ports. The user-defined UES is shifted into the device ID register in parallel from the 32-bit USERCODE register. The UES is then shifted out through the device ID register. The USERCODE information is available to the user only after the device is configured successfully.

The non-volatile USERCODE data is written to the configuration flash memory (CFM) block and then written to the SRAM at power-up. The USERCODE instruction reads the data values from the SRAM. When using real-time ISP to update the CFM block and write new USERCODE data, executing the USERCODE instruction returns the current running design's USERCODE (stored in the SRAM), not the new USERCODE data. The new design's USERCODE, stored in the CFM, can only be read back correctly if a power cycle or forced SRAM download has transpired after the real-time ISP update.

In the Quartus II software, there is an **Auto Usercode** feature where you can choose to use the checksum value of a programming file as the JTAG user code. If selected, the checksum will be automatically loaded to the USERCODE register. On the Assignments menu, click **Device**. In the Device dialog box, click **Device and Pin Options** and click the General tab. Turn on **Auto Usercode**.

CLAMP Instruction Mode

The CLAMP instruction mode is used to allow the state of the signals driven from the pins to be determined from the boundary-scan register while the bypass register is selected as the serial path between the TDI and TDO ports. The state of all signals driven from the output pins will be completely defined by the data held in the boundary-scan register. However, CLAMP will not override the I/O weak pull-up resistor or the I/O bus hold if you have any of them selected.

HIGHZ Instruction Mode

The HIGHZ instruction mode is used to set all of the user I/O pins to an inactive drive state. These pins are tri-stated until a new JTAG instruction is executed. When this instruction is selected, the bypass register is connected between the TDI and TDO ports. HIGHZ will not override the I/O weak pull-up resistor or the I/O bus hold if you have any of them selected.

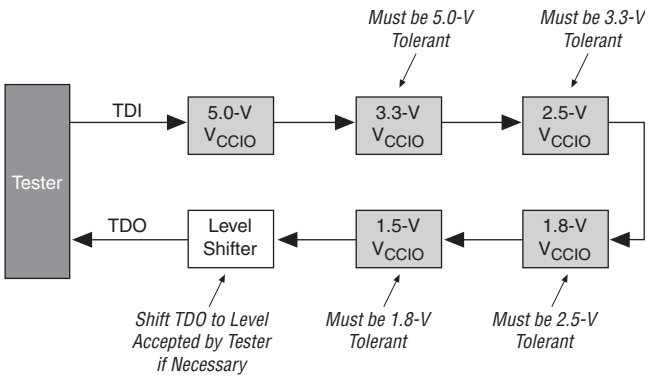
I/O Voltage Support in JTAG Chain

There can be several different Altera or non-Altera devices in a JTAG chain. However, you should be cautious if the chain contains devices that have different V_{CCIO} levels. The TDO pin of a device drives out at the voltage level according to the V_{CCIO} of the device. For MAX II devices, the TDO pin will drive out at the voltage level according to the V_{CCIO} of I/O Bank 1. The devices can interface with each other although they might have different V_{CCIO} levels. For example, a device with 3.3-V V_{CCIO} can drive to a device with 5.0-V V_{CCIO} because 3.3 V meets the minimum VIH on TTL-level input for the 5.0-V V_{CCIO} device. JTAG pins on MAX II devices can support 1.5-, 1.8-, 2.5-, or 3.3-V input levels, depending on the V_{CCIO} voltage of I/O Bank 1.

Refer to the *MAX II Architecture* chapter in the *MAX II Device Handbook* for more information on MultiVoltTM I/O support.

You can interface the TDI and TDO lines of the JTAG pins of devices that have different V_{CCIO} levels by inserting a level shifter between the devices. If possible, the JTAG chain should be built such that a device with a higher V_{CCIO} level drives to a device with an equal or lower V_{CCIO} level. By building the JTAG chain in this manner, a level shifter may be required only to shift the TDO level to a level acceptable to the JTAG tester. Figure 13–13 shows the JTAG chain of mixed voltages and how a level shifter is inserted in the chain.

Figure 13–13. JTAG Chain of Mixed Voltages



BST for Programmed Devices

For a programmed device, the input buffers are turned off by default for I/O pins that are set as output only in the design file. You cannot sample on the programmed device output pins with the default BSDL file when the input buffers are turned off. You can set the Quartus II software to always enable the input buffers on a programmed device so it behaves the same as an unprogrammed device for boundary-scan testing, allowing sample function on output pins in the design. This aspect can cause slight increase in standby current as the unused input buffer is always on.

1. On the Assignments menu, click **Settings.**
2. Under **Category**, select **Assembler**.
3. Turn on **Always Enable Input Buffers**.

Disabling IEEE Std. 1149.1 BST Circuitry

The IEEE Std. 1149.1 BST circuitry for MAX II devices is enabled upon device power-up. Because this circuitry may be used for BST or ISP, this circuitry must be enabled only if these features are used. This section describes how to disable the IEEE Std. 1149.1 circuitry to ensure that the circuitry is not inadvertently enabled when it is not needed.

Table 13–3 shows the pin connections necessary for disabling JTAG in MAX II devices that have dedicated IEEE Std. 1149.1 pins.

Table 13–3. Disabling IEEE Std. 1149.1 Circuitry

JTAG Pins *(1)*			
TMS	TCK	TDI	TDO
VCC *(2)*	GND *(3)*	VCC *(2)*	Leave Open

Notes to Table 13–3:

(1) There is no software option to disable JTAG in MAX II devices. The JTAG pins are dedicated.

(2) VCC refers to V_{CCIO} of Bank 1.

(3) The TCK signal may also be tied high. If TCK is tied high, power-up conditions must ensure that TMS is pulled high before TCK. Pulling TCK low avoids this power-up condition.

Guidelines for IEEE Std. 1149.1 Boundary-Scan Testing

Use the following guidelines when performing boundary-scan testing with IEEE Std. 1149.1 devices:

- If a pattern (for example, a 10-bit 1010101010 pattern) does not shift out of the instruction register via the TDO pin during the first clock cycle of the SHIFT_IR state, the proper TAP controller state has not been reached. To solve this problem, try one of the following procedures:
  - Verify that the TAP controller has reached the SHIFT_IR state correctly. To advance the TAP controller to the SHIFT_IR state, return to the RESET state and clock the code 01100 on the TMS pin.
  - Check the connections to the VCC, GND, and JTAG pins on the device.
- Perform a SAMPLE/PRELOAD test cycle prior to the first EXTEST test cycle to ensure that known data is present at the device pins when the EXTEST mode is entered. If the OEJ update register contains a 0, the data in the OUTJ update register will be driven out. The state must be known and correct to avoid contention with other devices in the system.
- Do not perform EXTEST and SAMPLE/PRELOAD tests during ISP. These instructions are supported before and after ISP but not during ISP.

If problems persist, contact Altera Applications.

Boundary-Scan Description Language (BSDL) Support

The BSDL—a subset of VHDL—provides a syntax that allows you to describe the features of an IEEE Std. 1149.1 BST-capable device that can be tested. Test software development systems then use the BSDL files for test generation, analysis, failure diagnostics, and in-system programming.

For more information, or to receive BSDL files for IEEE Std. 1149.1-compliant MAX II devices, refer to the Altera website at www.altera.com.

Conclusion

The IEEE Std. 1149.1 BST circuitry available in MAX II devices provides a cost-effective and efficient way to test systems that contain devices with tight lead spacing. Circuit boards with Altera and other IEEE Std. 1149.1-compliant devices can use the `EXTEST`, `SAMPLE/PRELOAD`, and `BYPASS`modes to create serial patterns that internally test the pin connections between devices and check device operation.

Institute of Electrical and Electronics Engineers, Inc. IEEE Standard Test Access Port and Boundary-Scan Architecture (IEEE Std. 1149.1-2001). New York: Institute of Electrical and Electronics Engineers, Inc., 2001.

Referenced Documents

This chapter references the following documents:

- *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*
- *In-System Programmability Guidelines for MAX II Devices* chapter in the *MAX II Device Handbook*
- *JTAG and In-System Programmability* chapter in the *MAX II Device Handbook*
- *MAX II Architecture* chapter in the *MAX II Device Handbook*

Document Revision History

Table 13–4 shows the revision history for this chapter.

Table 13–4. Document Revision History

Date and Revision	Changes Made	Summary of Changes
October 2008, version 1.7	■ Updated New Document Format.	—
December 2007, version 1.6	■ Removed Figure 13-14. ■ Updated Figure 13–6. ■ Added "Referenced Documents" section.	—
December 2006, version 1.5	■ Added document revision history.	—
August 2006, version 1.4	■ Updated IEEE Std. 1149.1 BST Operation ■ Control section.	—
July 2006, version 1.3	■ Updated "BST for Programmed Devices" section.	—
June 2005, version 1.2	■ Added a paragraph under the *USERCODE Instruction Mode* section. ■ Added a new section - *BST for Programmed Devices*.	—
January 2005, version 1.1	■ Previously published as Chapter 14. No changes to content.	—
March 2004, version 1.0	■ Initial Release.	—