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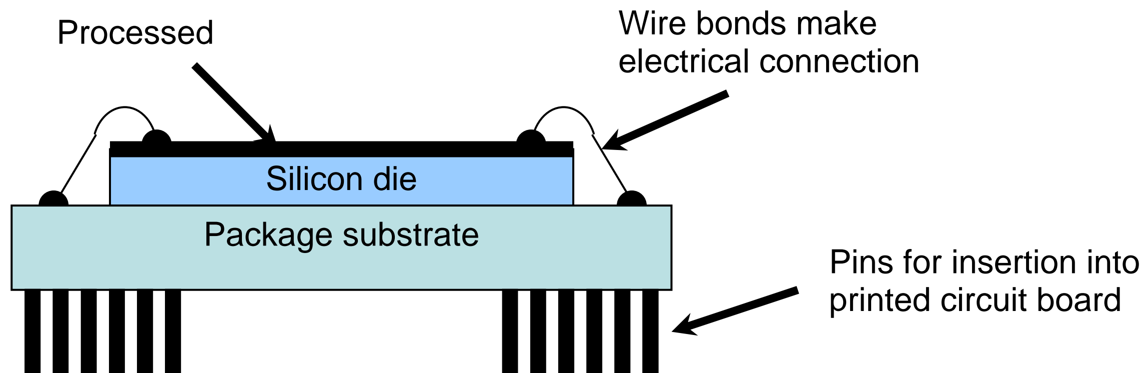
Glossary

GLOSSARY OF TERMS: INTEL FAMILY OF 45 NANOMETER PROCESSORS GO LEAD-FREE

***May 22, 2007* --** Intel Corporation today announced that it is going 100 percent lead-free beginning with its entire family of 45 nanometer (nm) high-k metal gate (Hi-k) processors, including the next-generation Intel® Core™ 2 Duo, Core 2 Quad and Xeon® processor families. Intel will begin 45nm Hi-k production in the second half of this year.

This glossary of terms was developed to clarify terminology used to describe Intel's lead-free technology.

There are two primary ways to connect the silicon die to the package:



Cross-section of wire bond package

Wire bond – In conventional packaging the back of the processed die is attached to the package and electrical connection is made through wires connecting the die to the package. This technique was used in the Intel® Pentium® processors and earlier. Wire bonding is cost-effective, but because signals have to travel over relatively long wires, the maximum frequency of the chip is limited. Also, wires can be attached only on the periphery, limiting the number of interconnects possible.

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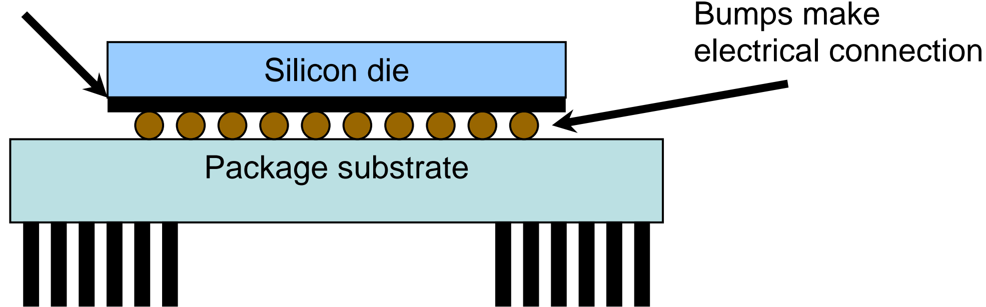
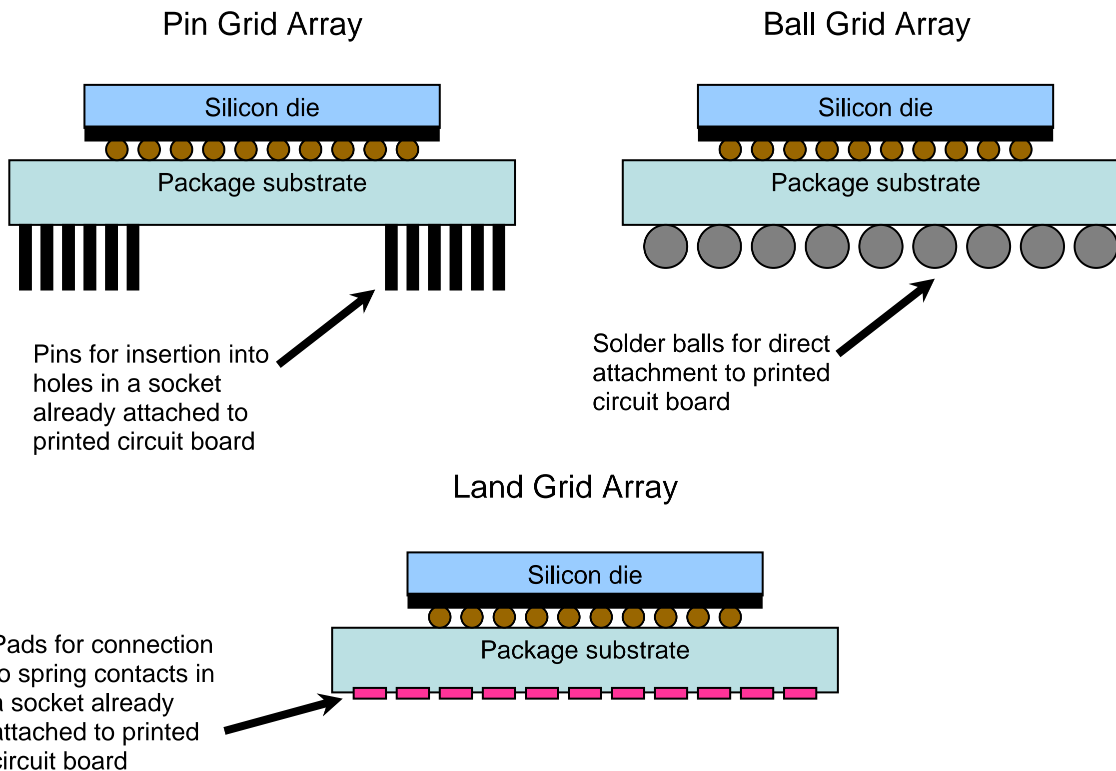


Cross-section of flip-chip package

Flip-chip – Bumps are added to the top of the silicon chip in the last phase of the semiconductor process. The chip is flipped over and the bumps are soldered to the package forming mechanical and electrical connections. There are many advantages over wire bonding: better performance at high frequency (since signals have a shorter distance to travel), plus the bumps can be located anywhere on the surface of the die rather than just on the periphery (this allows far more connections to be made between the die and the package). Also, flip-chip allows a heat spreader and heat sink to be attached to the back of the die, since it is now exposed.

There are 3 primary ways to attach packages to printed circuit boards.



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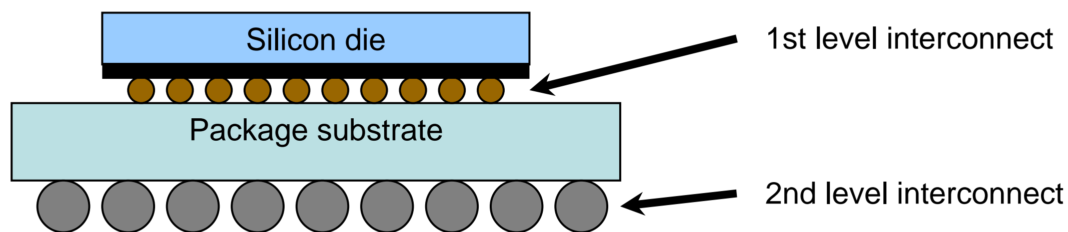
- **Pin Grid Array (PGA)** – Metal pins protrude from the bottom of the package and these are inserted into holes in a socket that was soldered to the board. The socket secures the package in place through pin. Pin grid arrays were first used on Intel386™ processors. Currently, Intel utilizes PGA package/sockets across mobile and server market segments.

- **Ball Grid Array (BGA)** – Solder balls are used to attach the package to pads on the board. BGAs are utilized in applications where size or cost is important because they eliminate the bulk and the cost of a socket. BGAs have the disadvantage that once the attachment is made to the motherboard, the package is difficult to remove. Currently, Intel utilizes BGA packages in flash, chipsets and mobile microprocessors.

- **Land Grid Array (LGA)** – In LGAs, there are no solder balls, but rather pads on the package that are touched by spring contacts in a socket already soldered to the printed circuit board. Since there are no pins, a fastener and loading plate are required to secure the package in place. LGAs utilize a smaller contact pad that enables more electrical connections between the package and the board than PGAs allow. Currently, Intel utilizes LGA package/sockets in the desktop market segment.

Other terms:

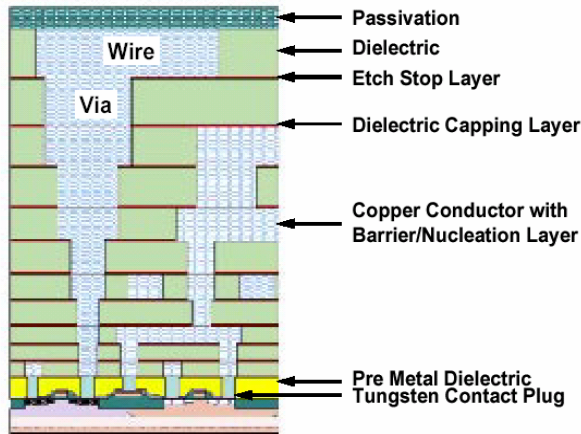


1st level interconnect – The interconnect between the die and the package.

2nd level interconnect – The interconnect between the package and the board. It also includes the interconnect between the package and capacitors (not shown) that are added to filter out spikes in electrical signals.

Coefficient of Thermal Expansion (CTE) - The linear thermal expansion coefficient relates the change in temperature to the change in a material's linear dimensions. It is the fractional change in length per degree of temperature change. The expansion and contraction of material must be considered when designing structures where large changes in dimension due to temperature are expected. The CTE for materials is given in parts per million (PPM) per Celsius degree.

Dielectric Constant - k – "k" refers to a term called a "dielectric constant" and it compares the permittivity of a material to that of free space. A low-k material has lower permittivity than standard materials, and conversely "high-k" has higher permittivity. The lowest possible permittivity is considered free space, a perfect vacuum, or "nothing." It is a measure of how readily a material transfers electric signals. Consider capacitance as proportional to the k value, so a given parallel place capacitor structure built with a low-k value insulator has lower capacitance than one with a high-k value. Here, a low-k inter layer dielectric is compared to a silicon dioxide (SiO_2), which was the traditional Inter Layer Dielectric. When considering high-k metal gates, the effective permittivity of the new transistor gate material is being compared to silicon dioxide (SiO_2). These materials are in different places in the silicon chip and must be optimized differently.



Example silicon cross-section

Inter Layer Dielectric – Processors consist of a network of transistors connected in a specific manner by copper interconnects. An insulating material is used to ensure that these interconnects are not shorted together inadvertently. To optimize the performance of a signal being carried on nearby interconnects, it is desirable to have an insulator to have the lowest possible “k” value.

Element Symbols from the Periodic Table:

Pb = lead
Ag = silver
Sn = Tin
Cu = copper
Si = silicon
O = oxygen

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