Pinned Packaging 13

13.1 Introduction

As Intel microprocessors become faster, more complex and more powerful, the demand on package performance increases. Improvements in microprocessor speed and functionality drive package design improvements in electrical, thermal and mechanical performance. Package electrical and thermal characteristics become attributes of component performance along with the mechanical protection offered by the package.

To meet these requirements, Intel has introduced a variety of innovative package designs. The development of the plastic pin grid array (PPGA) package, PPGA2, and Flip Chip Pin Grid Array (FC-PGA) have provided an improvement path for enhanced power distribution and improved thermal and electrical performance. While each consists of organic package materials, the primary differences within the package is that PPGA utilizes wirebond interconnect technology while the FC-PGA utilizes Flip Chip Interconnect. Externally, the PPGA thermal interface will be made to an integral package heat slug while the FC-PGA thermal interface will be made directly to the die backside. PPGA and FC-PGA are both socket compatible.Table 13-1 summarizes the key attributes of the PPGA package. The following sections detail the physical structure, electrical modeling and performance attributes of the PPGA package.

Table 13-1. PPGA Package Attributes

PPGA Attributes	
Physical	
Appearance	Circuit board, exposed pins
Package Body Material	BT laminate, Ni plated Cu heat slug, epoxy encapsulant, Au bond wires
Body Thickness	3.0 mm (overall, includes heat slug)
Weight	18 grams
Package Trace Metal	Copper
External Heat Slug	Yes
External Capacitors	Yes
Performance	
Thermal (θ_{jc}) with Heat Sink	0.30 - 0.50 °C/W
Power Distribution	Cu traces and multiple planes enhance distribution
Package Trace Propagation Delay	Cu traces have low resistance and reduce delay
Others	
Thermal Interface Used for Heat Sink Attachment	Thermally conductive and electrically non-conductive grease, phase-change material, film, or tape
Board Mount	PPGA socket

***Caution**:* For PPGA packages, electrically conductive surfaces should not touch any part of the processor except the heatslug. For example, an electrically conductive heat sink should not contact the exposed pins, external capacitors, or the exposed metal on the side of the package.

Table 13-2. FC-PGA Package Attributes

FC-PGA Attributes	
Physical	
Appearance	Circuit board - exposed pins, chip components, and die
Package Body Material	Fiber-reinforced resin substrate, epoxy underfill, Au/Ni-plated Kovar pins
Body Thickness	3.18 mm pins + 1.1 mm substrate + 0.83 mm die (5.11 mm total)
Weight	7.5 grams
Package Trace Material	Copper
External Heat Slug	No
External Capacitors and Resistors	Yes (pin side only)
Performance	
Thermal (θjs) with Heat Sink	0.6 °C/W (12-15 lbf. Clip force)
Power Distribution	Cu traces and multiple planes enhance distribution
Package Trace Propagation Delay	Cu traces have low resistance and reduce delay
Other	
Thermal Grease Used for Heat Sink Attachment	Thermally conductive and electrically non-conductive
Board Mount	Socket only
Warning: For FCPGA packages, electrically conductive surfaces should not touch any part of the processor except the die. For example, an electrically conductive heat sink should not contact the exposed pins, external capacitors, or the exposed metal on the side of the package.	

The Micro Pin Grid Array (µPGA) is the latest innovative packaging approach, developed as a conveyance for Organic Land Grid Array (OLGA) package technology CPUs in the thin and light configuration of mobile notebook computers. The µPGA is also known as an Interposer based package.

The interposer is a pinned FR-4 carrier which affords the OLGA package to be surface mounted to the interposer for future socketing by the OEMs. The development of the interposed package is a result from the OEM's requirement for a manufacturing alternative allowing flexibility in selecting whether to surface mount an OLGA or socket onto the motherboard at final assembly.

This High I/O interposed package utilizes a one for one, pin to BGA ball connectivity arrangement. Advantages to this packaging technique, is it's minimally larger surface area than the OLGA CPU itself, and that it attains a height reduction over the earlier Mobile Module used in notebook computers.

The entry of the µPGA packaging technology continues the commitment to provide packaging solutions that meet Intel's rigorous criteria for quality and performance.

Table 13-3 summarizes the key attributes of the PPGA package. The following sections detail the physical structure, electrical modeling and performance attributes of the PPGA package.

Table 13-3. µPGA Package Attributes

	µPGA	
Lead Count	**495**	**615**
Sq./Rect.	R	R
Pitch (mm)	1.27	1.27
Interposer Thickness (mm) nominal	1.0	1.0
Socketable pin length (mm) nominal	1.25	1.25
Weight (grams)		
Max. Footprint (mm) nominal	34.21 x 28.27w	37.51 x 35.56w
Shipping Media		
Trays	X	X
Desiccant		
Comments/Footnotes		

NOTE: Interposer size are Die size dependent. Please contact Intel Technical support for latest specifications

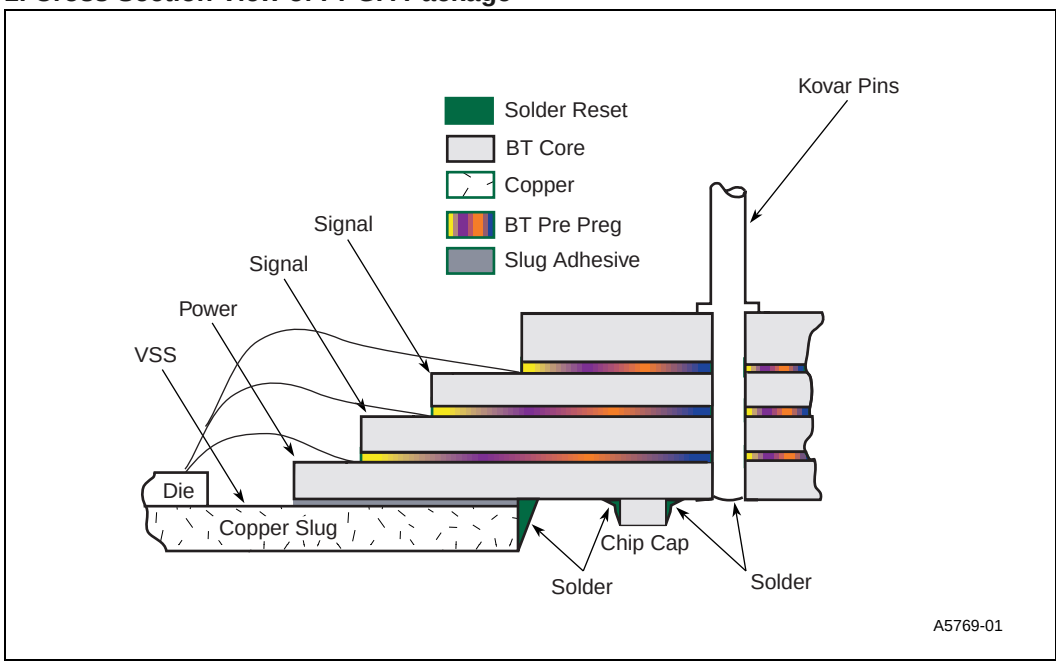
13.2 Packages Geometry And Materials

13.2.1 PPGA

13.2.1.1 Package Materials

The PPGA package body piece part is a pinned laminated printed circuit board (PCB) structure. Figure 13-1 illustrates the cross section of a typical PPGA piece part. The dielectric material, which is chosen for its high temperature stability, is a glass reinforced high glass transition temperature (Tg) Bismaleimide Triazine (BT) with a Tg ranging from 170° C to 190° C. Conductors are copper traces. For bondability the copper (Cu) bond fingers are plated with gold (Au) over nickel (Ni). The heat slug is Ni plated copper, which gives high thermal dissipation. The Kovar pins are plated with Au over Ni and are surrounded by solder after insertion into the PCB substrate.

Figure 13-1. Cross Section View of PPGA Package



13.2.1.2 Package Outline Drawings

The PPGA package in Figure 13-2 includes a nickel plated copper heatslug and eight discrete capacitors. The capacitors are an optional feature used to decouple the power and ground supplies to enhance performance of the packaged device.

Figure 13-2. Top View of a PPGA Package

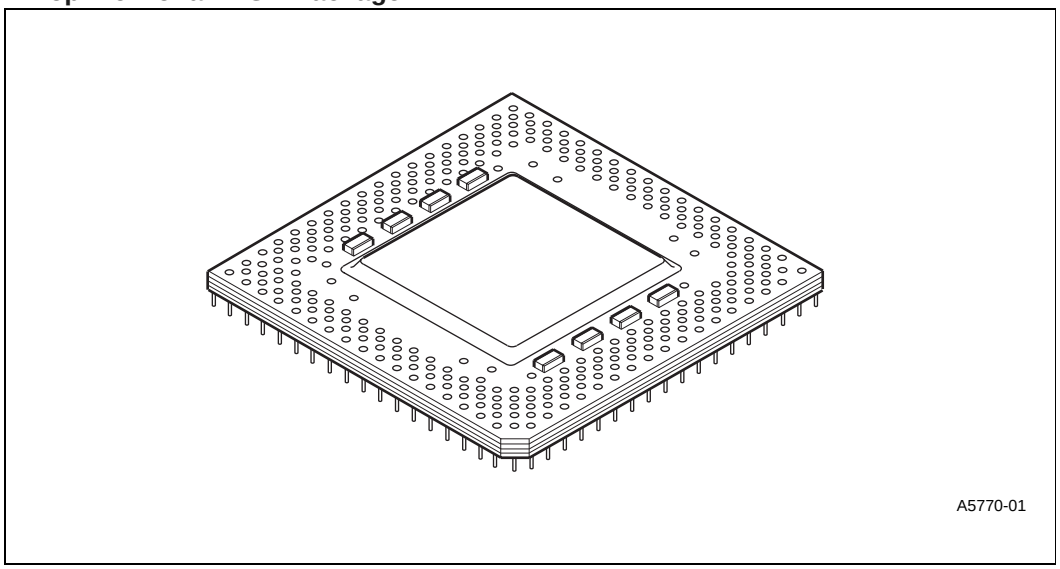


Figure 13-3, Table 13-4 and Table 13-5 illustrate the package outline drawings and dimensions for the 296 lead PPGA package. The package meets JEDEC outline spec MO-128 for pin count and package size. The package is square and 1.95 inches on a side and 3 mm in total thickness. The index corner has a 45° chamfer.

Table 13-4. PPGA Package Drawing Definitions

Symbol	Description of Dimensions
A	Package Body Thickness Including Heat Slug
A_1	Package Body Thickness
A_2	Heat Slug Thickness
B	Pin Diameter
D	Package Body Dimension
D_1	Pin Field Width
D_2	Heat Slug Width
D_3	Heat Slug Center to Package Edge
e1	Pin Pitch
F_1	Outer Chip Cap Heat Slug Center to Package Edge
F_2	Inner Chip Cap Heat Slug Center to Package Edge
L	Pin Length
N	Lead Count
S_1	Outer Pin Center to Package Edge

Figure 13-3. Principal Dimensions

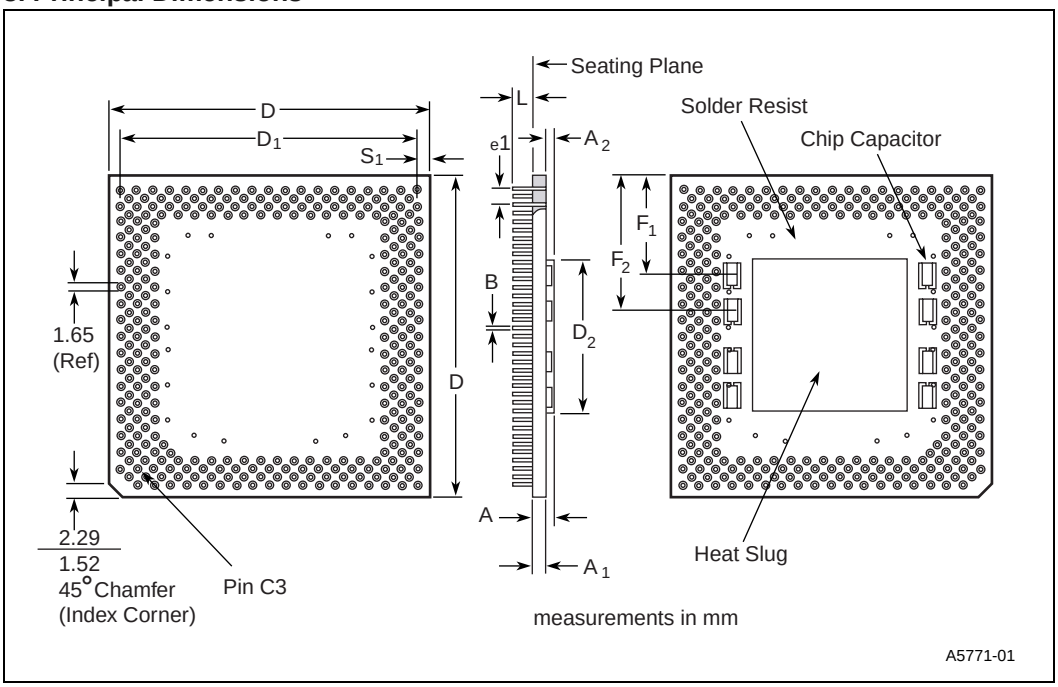


Table 13-5. 296 PPGA Package Dimensions and Tolerances

Family: Plastic Pin Grid Array Package - 296 Lead				
Symbol	**Millimeters**		**Inches**	
	Minimum	**Maximum**	**Minimum**	**Maximum**
A	2.72	3.33	0.107	0.131
A_1	1.83	2.23	0.072	0.088
A_2	1.00		0.039	
B	0.40	0.51	0.016	0.020
D	49.43	49.63	1.946	1.954
D_1	45.59	45.85	1.795	1.805
D_2	23.44	23.95	0.923	0.943
D_3	24.765		0.975	
e1	2.29	2.79	0.090	0.110
F_1	17.56		0.692	
F_2	23.04		0.907	
L	3.05	3.30	0.120	0.130
N	296			
S_1	1.52	2.54	0.060	0.100

NOTES:
1. A_2 Typical
2. F_1 Typical
3. F_2 Typical

Table 13-6. 370 PPGA Package Dimensions and Tolerances

Family: Plastic Pin Grid Array Package - 370 Lead				
Symbol	**Millimeters**		**Inches**	
	Minimum	**Maximum**	**Minimum**	**Maximum**
A	2.72	3.33	0.107	0.131
A_1	1.83	2.23	0.072	0.088
A_2	1.00		0.039	
B	0.40	0.51	0.016	0.020
D	49.43	49.63	1.946	1.954
D_1	45.59	45.85	1.795	1.805
D_2	25.15	25.65	0.990	1.010
D_3	23.495		0.925	
e1	2.29	2.79	0.090	0.110
F_1	17.56		0.692	
F_2	23.04		0.907	
L	3.05	3.30	0.120	0.130
N	370			
S_1	1.52	2.54	0.060	0.100

Table 13-6. 370 PPGA Package Dimensions and Tolerances

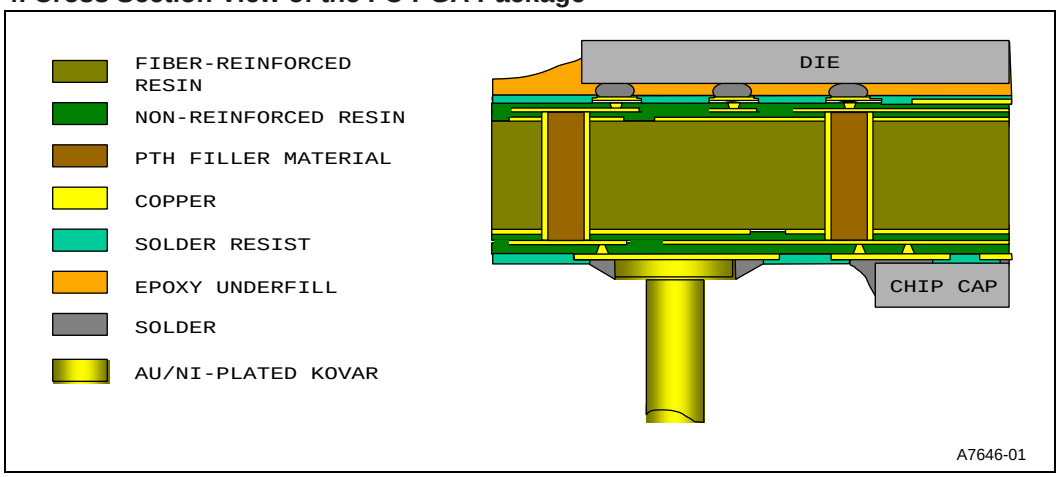
NOTES:
1. A_2 Typical
2. F_1 Typical
3. F_2 Typical

13.2.2 FC-PGA

13.2.2.1 Package Materials and Geometry

The FC-PGA package body piece part is a pinned, laminated printed circuit board (PCB) structure. Figure 13-4 illustrates the cross section of a typical FCPGA piece part. The circuit board is a laminate of two dielectric materials: a glass-reinforced high glass transition temperature (Tg) core with a Tg ranging from 165 °C to 175 °C and outer layers composed of non-reinforced resin. Conductors are copper traces. The Kovar pins are plated with Au over Ni and are attached to the substrate with high-temperature solder.

Figure 13-4. Cross Section View of the FC-PGA Package



13.2.2.2 Package Outline Drawings

The FCPGA package can include a combination of discrete capacitors and resistors. The capacitors are an optional feature used to decouple the power and ground supplies to enhance performance of the packaged device. The resistors have a variety of uses. All discrete components are located within a designated component keepin zone on the pin side of the package.

Figure 13-5. Top/bottom View of an FCPGA Package

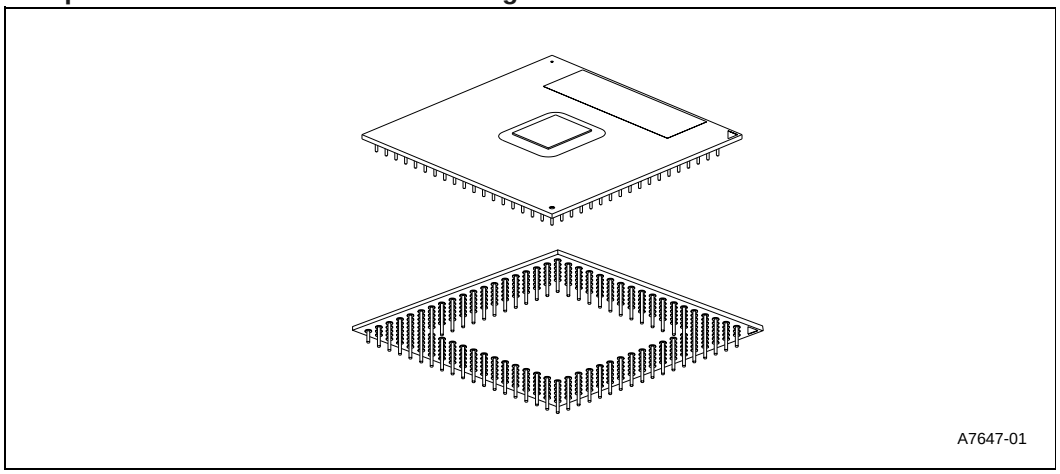


Figure 13-6, Table 13-7 and Table 13-8 illustrate the package outline drawings and dimensions for the 370 lead FCPGA package. The package meets JEDEC outline spec MO-128 for pin count and package size. The package is nominally 1.95 inches (49.53 mm) on each side and .076 inches (1.93 mm) in total thickness (not including the pins). There is no chamfered corner on this package, so pin 1 is indicated by a gold triangle.

Table 13-7. FC-PGA Drawing Symbol Definitions

Symbol	Description of Dimensions
A1	Die Height (including C4 bumps)
A2	Substrate Thickness
B1	Die Length (x-direction)
B2	Die Length (y-direction)
C1	Epoxy Underfill Length (x-direction)
C2	Epoxy Underfill Length (y-direction)
D	Package Body Length
D1	Pin Field Width
G1	Passive Components Keepin Zone Length (x-direction)
G2	Passive Components Keepin Zone Length (y-direction)
G3	Passive Components Keepin Zone Height
H	Pin Pitch
L	Pin Length
ϕP	Pin Diameter
Pin TP	Pin True Position Tolerance

Figure 13-6. FC-PGA principal dimensions

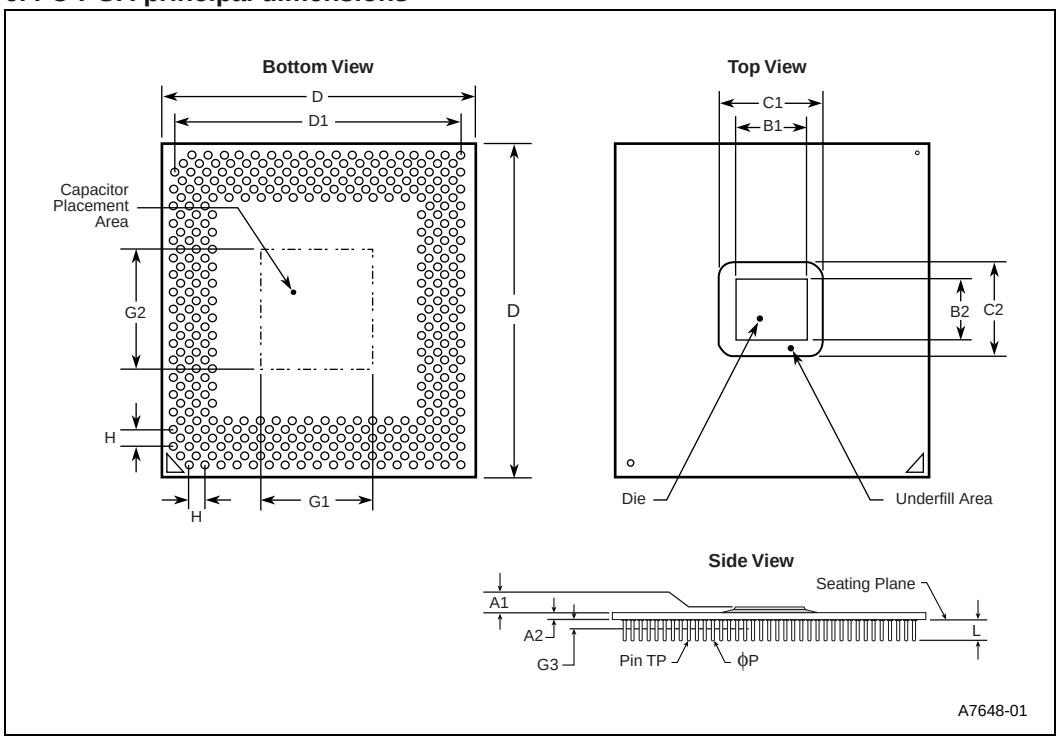


Table 13-8. FC-PGA Package Dimensions

Family: Flip Chip Pin Grid Array Package				
Symbol	**Millimeters**		**Inches**	
	Minimum	**Maximum**	**Minimum**	**Maximum**
A1	0.787	0.889	.031	.035
A2	1.000	1.200	.039	.047
B1	19.838 max		.781 max	
B2	19.838 max		.781 max	
C1	30.480 max		1.200 max	
C2	35.560 max		1.400 max	
D	49.428	49.632	1.946	1.954
D1	45.466	45.974	1.790	1.810
G1	0.000	17.780	0	.700
G2	0.000	17.780	0	.700
G3	0.000	0.889	0	.035
H	2.540 nominal		.100 nominal	
L	3.048	3.302	.120	.130
ϕP	0.431	0.483	.017	.019

13.2.3 µPGA

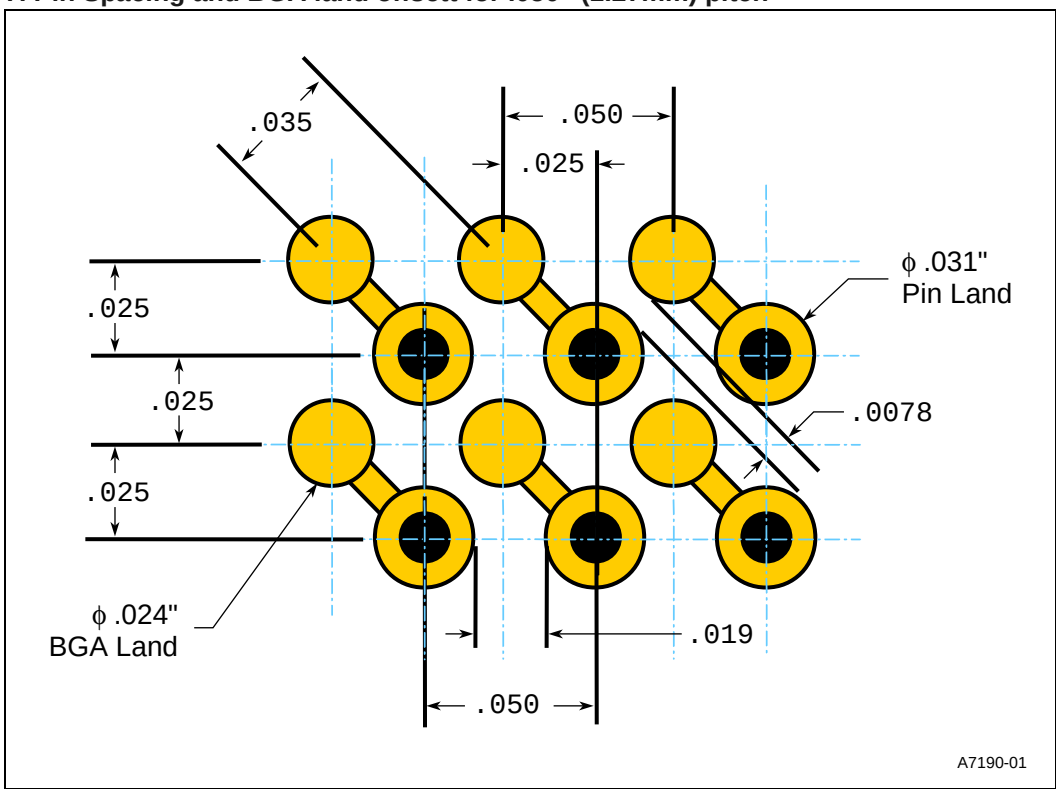
13.2.3.1 Package Materials and Geometry

The interposer as an OLGA carrier, consists of double-sided (¾ oz. per side) copper clad, on glass based, epoxy resin impregnated FR-4 laminate. This substrate utilizes copper alloy or Kovar pins, reflowed into an array of plated through holes within the substrate.

Because of the material likeness between the OLGA package and the Interposer, the assembled package exhibits improved coefficient of thermal expansion (CTE) compliant package properties in an assembled application.

The interposer has a die specific OLGA land pattern of .024" (0.609mm) diameter metal defined lands on .050" (1.27mm) pitch. It correspondingly accommodates a .050" (1.27mm) pitch offset pattern of pin lands. This pin land pattern is offset .025" (0.635mm) in the X and Y directions in relation to the OLGA land pattern. The pin lands and BGA land pairs are connected to each other with a .010" (0.254mm) wide trace. Figure 13-7 illustrates this concept.

Figure 13-7. Pin Spacing and BGA land offsett for .050” (1.27mm) pitch



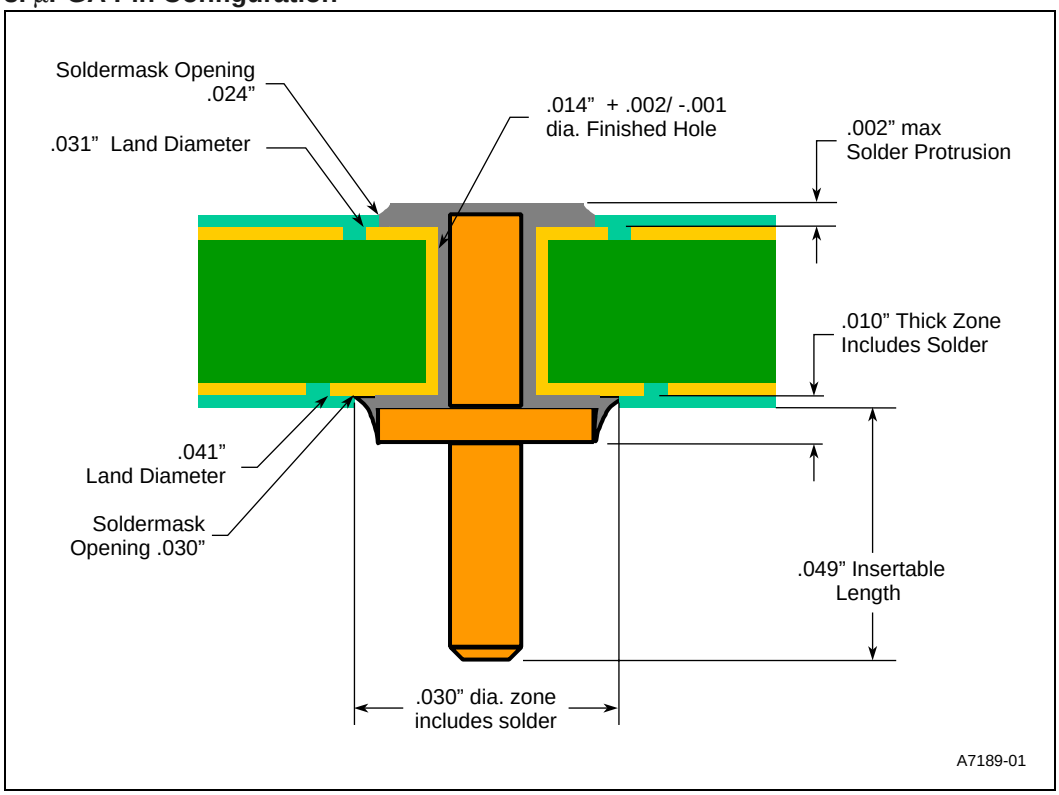
The pin base material is copper alloy (C19400) or Kovar, chosen because of its excellent electrical characteristics and resistance to bending. During manufacturing, the pin wire is extruded through a series of progressive dies to arrive at its configuration. The sharp edges are broken to .002" (0.050mm) typical, and are plated with 80 microinches minimum, of nickel and then overplated with 8 microinches, minimum of gold to ensure like metal contact with the socket contacts. This configuration was specifically developed for the thin and light mobile application.

The pin configuration used with interposer -1 interposers are a contour shoulder type. This configuration is illustrated in Figure 13-8.

These pins are nominally .012" (0.304mm) in diameter, have a .010" (0.254mm) maximum thick and a .024 (0.609mm) nominal, diameter shoulder. The socketable area of the pin, as defined, is from the bottom side of the interposer to the pin tip which is nominally, .049" (1.25mm) in length. This includes a .010" (0.254mm) high X .030" (0.965mm) diameter zone which accommodates the shoulder and solder fillet area when inserted into the socket.

After the pins are fixtured, 95% Sn 5% Sb solder is used to reflow the pins into the interposer. The solder height is maintained at .002" (0.050mm) maximum, above the land array of the pins to ensure no interference with the solderpaste stencil during solder application prior to OLGA assembly.

Figure 13-8. µPGA Pin Configuration



13.2.3.2 Package Outline Drawings

The Interposer -1 configuration is dependent upon the OLGA package used. This section will indicate reference package dimensions for both the 615 pin and 495 pin Interposer applications.

Table 13-9. µPGA Drawing Symbol Definitions

Letter or Symbol	Description of Dimensions
A	Interposer Height Including Insertable Pin Length
A1	Interposer Substrate Thickness
A2	Insertable Pin Length
ØB	Pin Diameter
C	Pin Pitch X and Y
D	Interposer Width "X" Direction
D1	Width of Pin Array
E	Interposer Length "Y" Direction
E1	Length of Pin Array
F	Distance of First Pin Row to Edge in "X" Direction
G	Distance of First Pin Column to Edge in "Y" Direction
H	OLGA Pattern Center Distance to Interposer Edge in the "Y" Direction
J	OLGA Pattern Center Distance to Interposer Edge in the "X" Direction
K	Fiducial to Fiducial Distance in the "Y" Direction
L	Fiducial to Fiducial Distance in the "X" Direction
M	Fiducial to Interposer Edge Distance in the "Y" Direction
N	Fiducial to Interposer Edge Distance in the "X" Direction

Figure 13-9. µPGA 615 Principle Dimensions

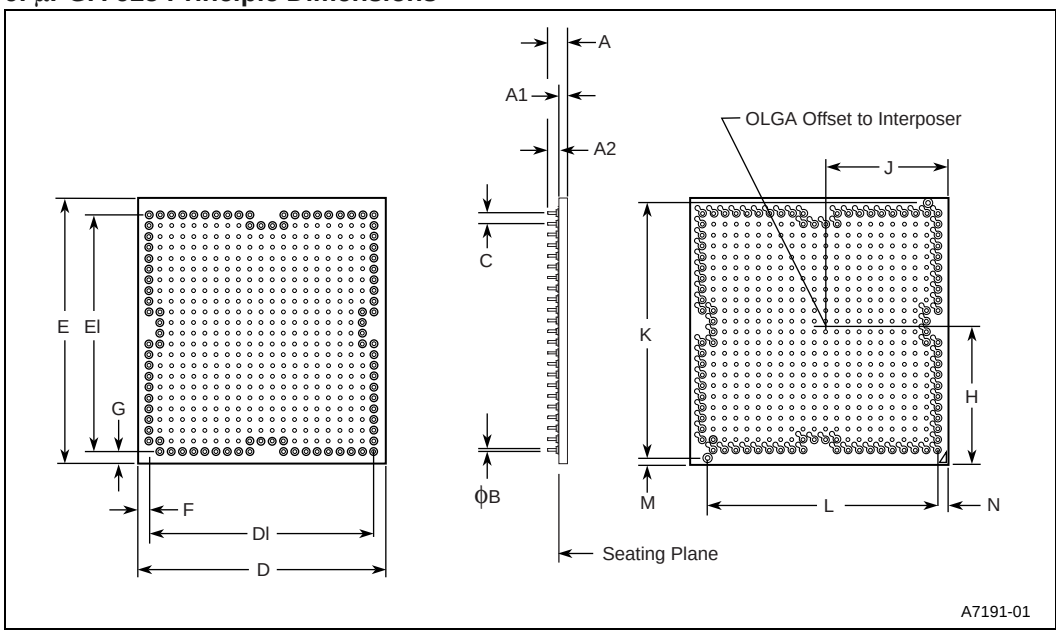


Table 13-10. µPGA 615 Dimensions

		Inches				Millimeters		
	Symbol	Min	Nom	Max	Notes	Min	Nom	Max
Pin Count			615				615	
Interposer Height	A	--	.088	--	1	--	2.23	--
Substrate Thickness	A1	.033	.039	.045	1	0.85	1.00	1.15
Socketable Pin length	A2	.047	.049	.051	1	1.19	1.25	1.31
Pin Diameter	ØB	--	.012	.014	1	--	0.30	0.36
Pin Pitch	C	--	.050	--	1	--	1.27	--
Interposer Width	D	1.276	1.282	1.288	1	32.41	35.56	32.71
Array Width	D1	--	1.200	--	1	--	30.48	--
Interposer Length	E	1.441	1.447	1.453	1	36.60	36.75	36.90
Array Length	E1	--	1.300	--	1	--	33.02	--
Pin to edge distance along "D"	F	--	.077	--	1	--	1.95	--
Pin to edge distance along "E"	G	--	.086	--	1	--	2.18	--
OLGA center "Y" Offset to Interposer edge	H	--	.641	--	1,2	--	16.28	--
OLGA center "X" Offset to Interposer edge	J	--	.723	--	1,3	--	18.36	--
Fiducial "Y" Distance	K	--	1.369	--	1	--	34.77	--
Fiducial "X" Distance	L	--	1.075	--	1	--	27.30	--
Fiducial to edge distance along "E"	M	--	.038	--	1	--	0.96	--
Fiducial to edge distance along "D"	N	--	.105	--	1	--	2.66	--

NOTES:
1. Package dimensions are for reference only. See product drawings for specific dimensions.
2. The offset of the OLGA pattern center to the offset of the pin pattern center in the "Y" direction is .013 inches (0.33mm).
3. The offset of the OLGA pattern center to the offset of the pin pattern center in the "X" direction is .010 inches (0.25mm).

Figure 13-10. µPGA 495 Principle Dimensions

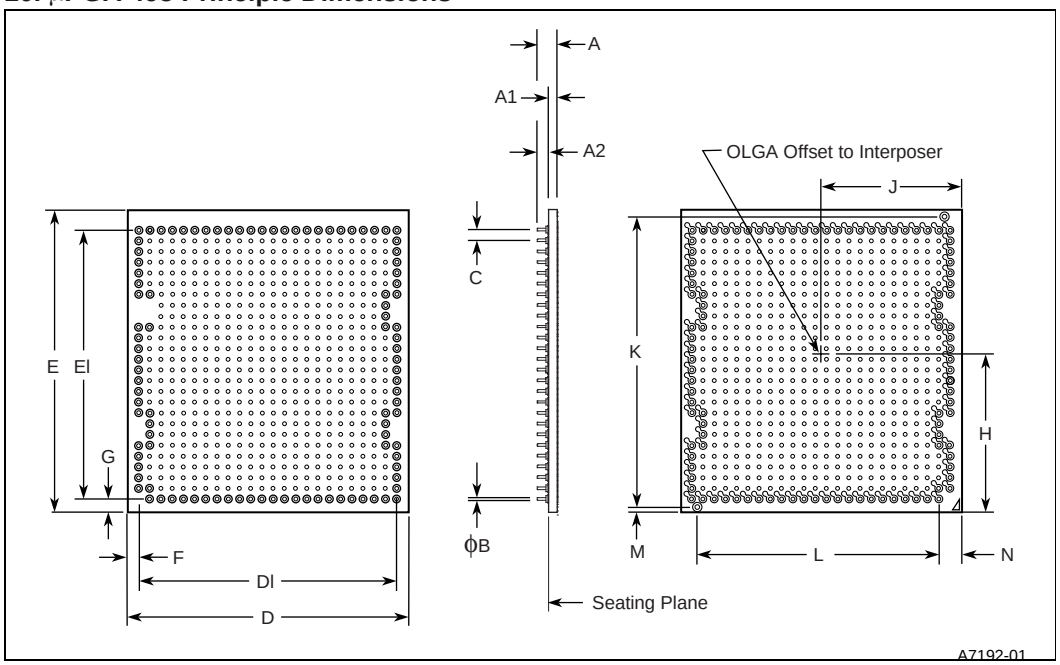


Table 13-11. µPGA 495 Dimensions

		Inches				Millimeters		
	Symbol	**Min**	**Nom**	**Max**	**Notes**	**Min**	**Nom**	**Max**
Pin Count			495				495	
Interposer Height	A	--	.088	--	1	--	2.23	--
Substrate Thickness	A1	.033	.039	.045	1	0.85	1.00	1.15
Socketable Pin length	A2	.047	.049	.051	1	1.19	1.25	1.31
Pin Diameter	ØB	--	.012	.014	1	--	0.30	0.36
Pin Pitch	C	--	.050	--	1	--	1.27	--
Interposer Width	D	1.107	1.113	1.119		28.17	28.27	28.37
Array Width	D1	--	1.000	--	1	--	25.40	--
Interposer Length	E	1.341	1.347	1.353		34.06	34.21	34.36
Array Length	E1	--	1.150	--	1	--	29.21	--
Pin to edge distance along "D"	F	--	.067	--		--	1.70	--
Pin to edge distance along "E"	G	--	.086	--	1	--	2.18	--
OLGA center "Y" Offset to Interposer edge	H	--	.674	--	1,2	--	17.11	--
OLGA center "X" Offset to Interposer edge	J	--	.557	--	1,3	--	14.14	--
Fiducial "Y" Distance	K	--	1.270	--	1	--	32.25	--
Fiducial "X" Distance	L	--	.925	--	1	--	23.49	--
Fiducial to edge distance along "E"	M	--	.038	--	1	--	0.96	--

Table 13-11. µPGA 495 Dimensions

Fiducial to edge distance along "D"	N	--	.096	--	1	--	2.66	--

NOTES:
1. Package dimensions are for reference only. See product drawings for specific dimensions.
2. The offset of the OLGA pattern center to the offset of the pin pattern center in the "Y" direction is .012 inches (0.30mm).
3. The offset of the OLGA pattern center to the offset of the pin pattern center in the "X" direction is .010 inches (0.25mm).

13.3 Applications

Both the PPGA and FC-PGA package has been developed for Intel's advanced microprocessor family of products. They have been designed for use in socketed applications, using socket footprints which are compatible with the Intel ceramic Pin Grid Array package family. While the PPGA package can be used in both Zero and Low Insertion Force sockets (ZIF/LIF), the FC-PGA should only be used in a ZIF socket application.

13.4 Component Assembly Process

13.4.1 PPGA Component Assembly

The PPGA assembly process flow is similar to the CPGA process flow with the exception of the seal operation.

As preparation for die attach, wafers are mounted on a pressure sensitive carrier tape and diced with a high speed saw. The cut wafer is washed with a detergent solution to remove silicon dust.

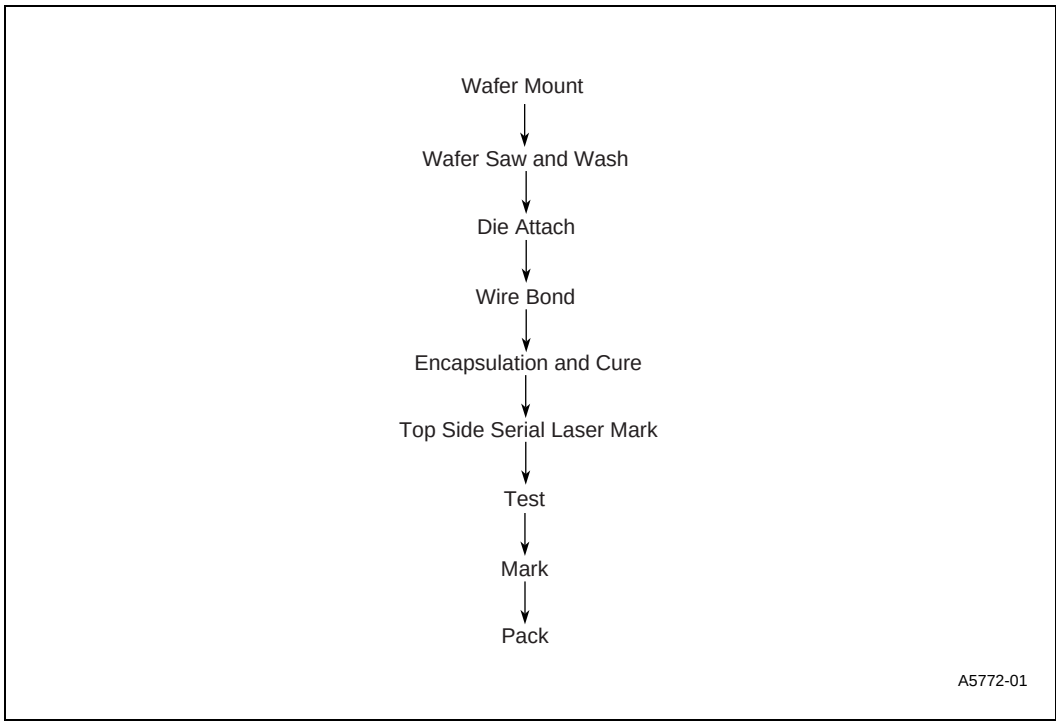
A silver filled epoxy adhesive is applied to the package substrate at die attach. Dice are picked from the wafer and placed on the adhesive. The adhesive is then cured.

The die are connected to the gold plated package leads by way of gold wedge wire bond technology. Bond pad and package lead placement accuracy and wire pull strength monitors ensure high integrity connections.

PPGA packages are encapsulated with silica filled liquid epoxy in contrast to the CPGA lid seal process. The encapsulant provides mechanical and environmental protection for the die and wires. Process trays are moved beneath a valve which fills the package cavity with epoxy and are transferred to an in-line oven in which the epoxy is cured.

A matrix code containing the assembly date code information is marked on the top side of the package using a laser. The mark is inspected for orientation and readability. The packages are then ready for the testing, finishing and packing processes.

Figure 13-11. PPGA Generic Process Flow



13.4.2 FC-PGA Component Assembly

The FCPGA assembly process flow is similar to the OLGA process flow without ball attach and ball inspection steps but with the addition of the pin inspection step.

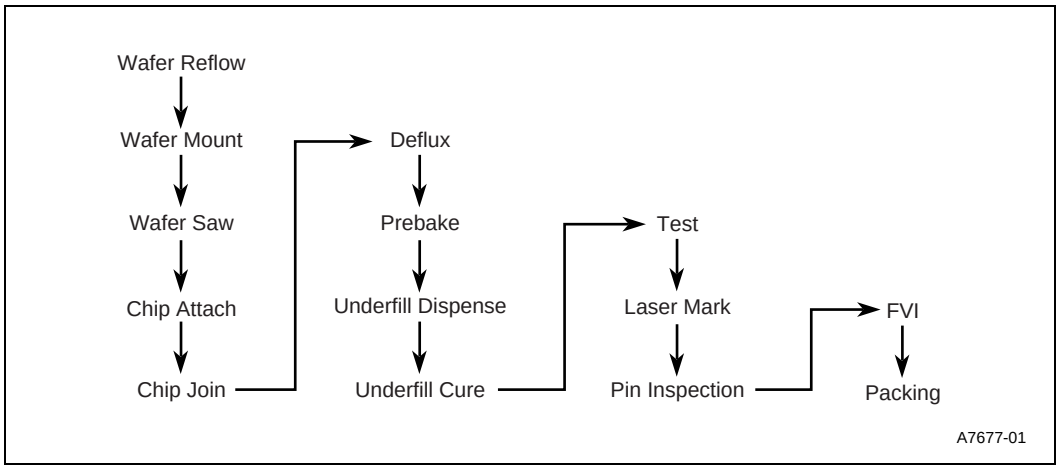
In preparation for chip attach, C4 wafer reflow process is to modify the shape and surface composition of the Pb/Sn bumps from the as-plated state to one acceptable for chip join. The wafers are then mounted on a pressure sensitive carrier tape and diced with a high speed saw. The cut wafer is washed with a detergent solution to remove silicon dust.

Die are picked from the wafer and mounted to the package. The units are then reflowed in a furnace to form C4 solder joints of the die and package.

The FCPGA units are then pre-baked in the oven to remove the moisture from the organic package before epoxy underfill materials is dispensed. The liquid capillary flow pull the underfill materials to fill the gaps around the solder joints in between the die and the package. The epoxy underfill materials are then cured in the oven.

The units are then ready for testing and finishing process. The finishing process includs laser marking the human readable product/assembly/test information along with pin inspection, final visual inspection and pack.

Figure 13-12. FC-PGA Generic Process Flow



13.5 Package Usage

13.5.1 PPGA Package

13.5.1.1 PPGA Package Shipping Media

PPGA shipping trays are compliant to JEDEC standards. All external dimensions of the PPGA tray are the same as the CPGA tray. There is a slight difference in the distance from the top of the tray to the seating plane of the PPGA shipping tray compared to the CPGA shipping tray. The PPGA shipping tray pocket is smaller in the x- and y-axes. This slightly smaller pocket dimension reduces package free-play in the tray. Refer to Chapter 10 for the dimensions of the PPGA shipping tray. PPGAs are shipped in uniquely colored trays separately from CPGAs. This enables manufacturing personnel to readily identify which package type is being placed into manufacture at any time. This shipping media minimizes foreign material and meets ESD safe shipping requirements.

13.5.1.2 PPGA Moisture Sensitivity

PPGA packages have been designed for socketed applications. They are neither shipped in moisture barrier bags, nor is floor life exposure time tracking needed for socketed applications. The maximum body temperature which the component should see is 150° C. The component is neither intended for direct through-hole mounting by wave solder processing nor for exposing the entire package body to surface mount-like reflow profiles. Such thermal profiles are not recommended for PPGA packages.

13.5.1.3 PPGA Socketing

Intel recommends that when performing insertion and extraction, the maximum force should not exceed 100 lbs., and should be applied uniformly. The insertion and extraction tool should take into account the clearance for the external capacitors and heat slug.

PPGA packages may be used in either low insertion force (LIF) or zero insertion force (ZIF) sockets. 296 lead sockets are available for PPGA packaged components from many suppliers. The socket design is a standard footprint on the PCB. Insertion and extraction forces were measured on sockets from various vendors. For all LIF socket designs tested, the maximum insertion force

required was 80 lbs. Avoid uneven loading during insertion. The applied load overcomes the frictional resistance applied to the package pins as they are inserted into the socket. Table 13-12 summarizes the average measured insertion and extraction force for different sockets.

Table 13-12. PPGA Insertion/Extraction Force Measurement

Socket[1]	Average Insertion Force (LB)	Average Extraction Force (LB)
Preci-Con LIF	44.69	57.43
Mill-Max LIF	38.09	49.65
Robinson Nugent LIF	78.35	73.51
AMP LIF	65.06	69.91
Andon LIF	54.26	58.58
Yamaichi ZIFs	n/a	80.94[2]

NOTES:
1. This data does not constitute a recommendation for any specific supplier or part number.
2. This is measured when the lever is actuated to ensure that the package will not be pulled out during shock and vibration test. When the lever is up, the extraction force is "zero".

If the manufacturing flow requires inserting the package after the heat sink is applied to the component, then the same suggested force may be applied uniformly across the top surface of the heatsink.

13.5.2 FC-PGA Package

13.5.2.1 FC-PGA package shipping media

FCPGA shipping trays are of JEDEC style and may be of a thin or thick configuration. All external dimensions and perimeter handling features of the FC-PGA tray are the same as the CO-028 or CO-029 registered standards. All internal features are compliant to Intel Standard requirements. Density of the trays has been optimized and thus negates the possibility of automated empty-tray handling by vacuum pickup features. As is currently true of all new shipping trays, the seating plane has been adjusted to accommodate these packages within the top and bottom planes of a tray with appropriate head clearance. Pocket x, y dimensions are specific by form factor, as specified in the tray drawing, and are larger than previous form factors for PLGA or PPGA. Tray temperature rating for non-SMT products will be an Intel approved low temperature no-bake material.

Shipping trays are no longer color coded by particular product. Color standardization by process type will result in the new low-temperature no-bake trays meeting the requirements of the drawing regardless of form factor. Shipping trays will meet ESD safe shipping requirements.

13.5.2.2 FC-PGA Moisture Sensitivity

13.5.2.3 FC-PGA Socketing

FC-PGA packages use zero insertion force (ZIF) lead sockets which are available from many suppliers. Intel recommends that before performing insertion, the package pins have to be manually aligned to the socket. After insertion, FC-PGA has to be locked using the single lever actuation in the socket. Avoid package walkout (package being pushed upward) during insertion as it may cause unnecessary tilt to the heatsink assembly. Actuating force only require less than 10 lb without lubricant. The movement of the socket cover is limited to the plane parallel to the motherboard.

13.5.3 µPGA Package

The interposer /OLGA package is designed for use in applications where CPU socketability, height, footprint geometry and weight are a high priority. Most importantly, the interposer/OLGA affords the OEMs the option to reflow either the OLGA or a socket to the motherboard at assembly. To accomplish this the objective, it is necessary to have the interposer land diameter equal to that on the motherboard at the CPU location. With this requirement, it is suggested that the OEMs use a .024" diameter metal defined land for the motherboard design. In general, .050" (1.27mm) pitch OLGA designs from Intel, require a .024" metal defined solderable land diameter. The exact diameter for any given OLGA package design should be obtained from Intel prior to the start of the motherboard design to ensure equivalent solderball height after reflow.

13.5.3.1 µPGA Package Shipping Media

The OLGA / Interposer assembly are shipped in a mid temperature thin matrix tray that complies with JEDEC standards. This shipping media minimizes foreign material and meets ESD safe shipping requirements. Typically, JEDEC trays have the same "X" and "Y" outer dimensions and are easily stacked for storage and manufacturing. For tray dimensions please refer to chapter X.X of this data book. The JEDEC trays are returnable to Intel for reuse. Chapter X.X contains detailed information on the return addresses for the different types of shipping trays.

13.5.3.2 µPGA Moisture Sensitivity

Most OLGA components are sensitive to moisture exposure before the reflow temperature exposure. Maintaining proper control of moisture uptake in OLGA components is critical.

13.5.3.3 OLGA to µPGA Assembly

The Pick and place accuracy of the placement system governs the package placement and rotational (theta) alignment. Slightly miss-aligned parts (less than 50% off the center of the land), will automatically self align during reflow due to solder surface tension properties. Grossly miss-aligned OLGA packages to interposer lands (greater than 50% off the center of the land) should be removed prior to reflow as they may develop electrical shorts (as a result to solder bridging) if they are subjected to reflow.

13.5.3.4 µPGA Socketing

Intel recommends that when performing insertion and extraction, the maximum force should not exceed 60 pounds pressure on the die surface, and should be applied uniformly.

13.6 Heat Sink Attachment

Intel recommends that when performing heatsink attach and the package is supported only on its periphery (such as in a shipping tray), the maximum force should not exceed 40 lbs.

13.6.1 Thermal Interface Material

To ensure PPGA packages are mechanically compatible with CPGA, a comprehensive evaluation of the effective method of heat sink attachment has been performed. It is suggested that the interface material used for heat sink attachment should have thermal conductivity greater than 0.8 W/mK, and be electrically non-conductive. The volume resistivity of the material should be greater than $1x10^6$ Ohm-cm.

13.6.2 Clip Design and Attach

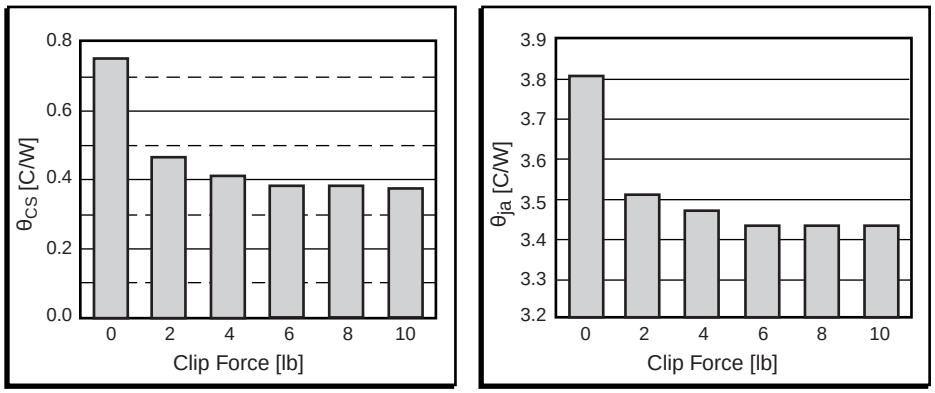
A minimum clip force of five pounds is recommended. Clips retain the heat sink assembly in the socket by exerting a force on the heat sink and the socket. The clip force, in turn, aids in forcing the grease to fill the many microscopic peaks and valleys on the heat sink and package surface, thereby reducing the interface thermal resistance. Since different clip forces result in different amounts of grease squeezed out, the corresponding bond line thickness of the grease will affect thermal performance.

The effect of foil sizes, clip force and voiding on Thermalcote I Conductacoat* thermal performance was also explored. If there is no grease on the Al foil, then voiding will exist in the bond line. This results in higher θ_{ja} values. While up to 30% grease voiding can be tolerated without any impact on PPGA thermal performance, zero voiding is strongly recommended for any heat sink attachment methods.

A larger foil size will cover a larger area with grease, but a smaller foil size is preferred for handling. For example, thermal resistance $\theta_{ja,}$ measured with a standard sized foil (1.0” x 1.0”) is 0.1 C/W to 0.2 C/W lower than the θ_{ja} measured with smaller foil (0.7” x 0.7”). Note that the Al foil is carrier specific for Thermalcote I Conductacoat* grease to aid volume manufacturing. The decision to use Al foils should be based on the OEMs particular heat sink attachment methods and assembly line(s).

Clip force determines the thermal grease bond line thickness and directly impacts thermal performance. To determine the effect of clip force on thermal performance, θ_{ja} and θ_{cs} values for the heat sink assemblies were measured at different clip forces. The actual clip forces of these modified clips were individually measured by using a Material Testing System (MTS) before thermal resistance measurement. All clip forces were also verified by using MTS after thermal resistance measurement. Figure 13-13 shows θ_{ja} and θ_{cs} values versus clip force. If the clip force is higher than five pounds (corresponding to ~ 5 psi), then there is no significant effect of clip force on PPGA thermal performance.

Figure 13-13. Comparison of θcs and θja for Different Clip Forces



NOTES:
θ_{ja} = Junction to Ambient
θ_{cs} = Case to Sink Thermal Resistance (˚CW)

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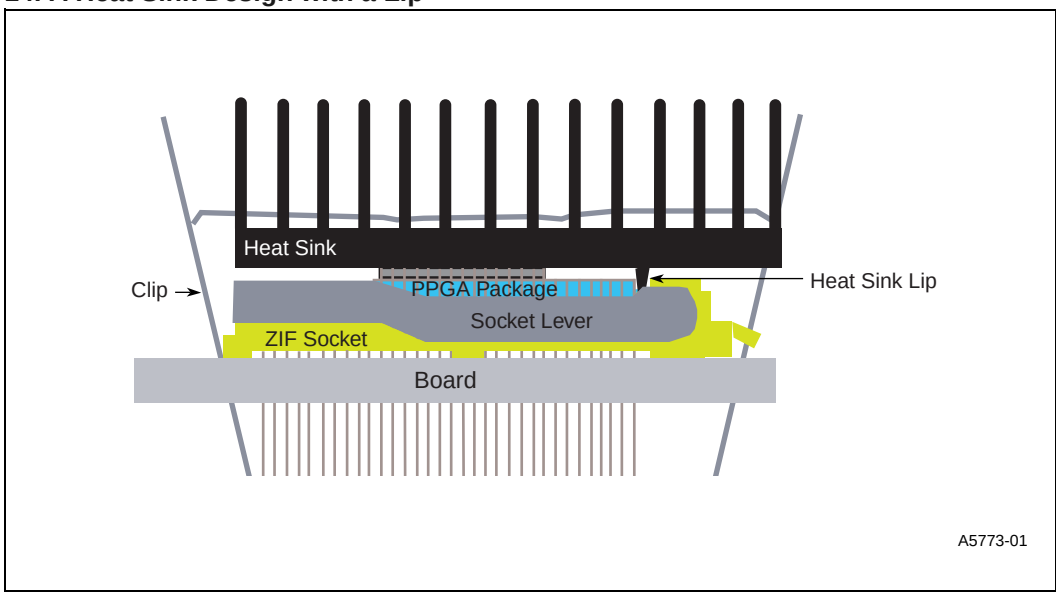
13.6.3 Heat Sink Design

The PPGA package may affect some existing heat sink designs. In one design, shown in Figure 13-14, the heat sink has a lip designed for a CPGA package to prevent movement of the heat sink relative to the package, socket and clip during mechanical shock tests. However, the PPGA package has a heatslug, external capacitors, and exposed pins on the top side of the package. For use on the PPGA package, if the heat sink slips out of its secured position, the lip may touch the exposed pins. Therefore, the lip should be extended to a proper length to lock the heat sink in a secured position. Intel's evaluations indicate that a 50 mil lip is not adequate and that a 70 mil lip is required to ensure reliable performance during shock and vibration testing. Tests also show that the 70 mil lip works well with CPGA packages. In addition, the side of the package is electrically conductive. If the heat sink is electrically conductive, and the lip touches the side of the package, then electrical shorting may occur, causing damage to the processor. In addition, the side of the package has exposed metal that is electrically conductive. If the heat sink is electrically conductive, and the lip touches the side of the package, then electrical shorting may occur, causing damage to the processor. Manufacturers should work with their heat sink suppliers to ensure that their heat sink designs can accommodate both PPGA and CPGA packages.

Figure 13-14. A Heat Sink Design with a Lip



13.6.4 Method for PPGA Heatsink Attach

The impact of the PPGA package on board assembly was studied by assembling PPGA packages into sockets soldered on boards. A suggested sequence for mounting the PPGA packages is:

1. With the package in the socket, place the Conductacoat foil on top of the package.

   The process flow for this step may be slightly different for the ZIF versus LIF sockets. For ZIF sockets the grease foil is placed on the CPU before insertion into the socket. For the LIF sockets place the thermal grease foil on the CPU after it is inserted into the socket. However, use manufacturing controls when stacking up the CPU, thermal interface and the heat sink to avoid foil misplacement on the PPGA slug.

2. Place the heat sink on the package and hook the heat sink clip onto the socket.

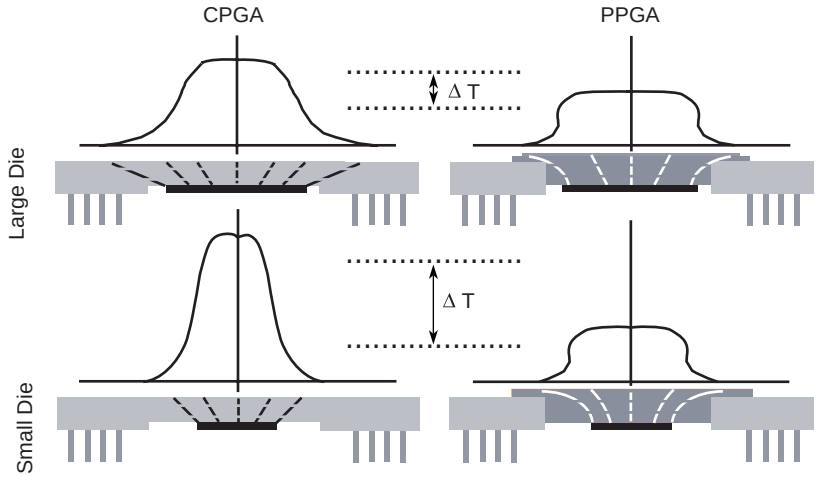
Note: Components on the top, and exposed metal on the side of the PPGA package can be shorted by any electrically conductive material including heat sinks, thermal grease (if electrically conductive) and thermal grease foil carriers.

13.7 PPGA Performance Characteristics

13.7.1 Thermal Characteristics

To improve thermal performance, the PPGA package uses a high thermal conductivity heat slug. The die is attached directly to the nickel plated copper heat slug, resulting in a lower thermal resistance than the comparable ceramic version. By effectively spreading the heat flux, the PPGA package is able to lower its thermal resistance. All data covered in this section is specific for P54CS die size only. However, the trend and advantage of PPGA over CPGA is identical for different die sizes. Similar advantages of PPGA over CPGA can be expected for all the other die sizes. Based on measurements of the components, Figure 13-15 demonstrates the advantage of PPGA over CPGA in terms of thermal resistance.

Figure 13-15. PPGA Has Better Thermal Conduction / Spreading



θ_{ja} of PPGA is about 1.1° C/W lower than that of CPGA. Table 13-13 to Table 13-18 detail the thermal resistance values for the components in ceramic pin grid array and plastic pin grid array packages.

Table 13-13. θ_{ca} [°C/W] for Different Heat Sink Heights and Air Flow Rates (CPGA)

	θ_{ca} [°C/W] vs Air Flow Rate [LFM]					
Heat Sink Height	**0**	**100**	**200**	**400**	**600**	**800**
0.25”	9.4	8.3	6.9	4.7	3.9	3.3
0.35”	9.1	7.8	6.3	4.3	3.6	3.1
0.45”	8.7	7.3	5.6	3.9	3.2	2.8
0.55”	8.4	6.8	5.0	3.5	2.9	2.6
0.65”	8.0	6.3	4.6	3.3	2.7	2.4
0.80”	7.3	5.6	4.2	2.9	2.5	2.3
1.00”	6.6	4.9	3.9	2.9	2.4	2.1
1.20”	6.2	4.6	3.6	2.7	2.3	2.1
1.40”	5.7	4.2	3.3	2.5	2.2	2.0
1.50”	5.5	4.1	3.1	2.4	2.2	2.0
None	14.5	13.8	12.6	10.5	8.6	7.5

NOTE:
1. θ_{ca} is case-to-ambient thermal resistance. θ_{ca} values shown in this table are typical values. The actual θ_{ca} values depend on the heat sink fin design, the interface between heat sink and package, the air flow in the system, and thermal interactions between CPU and surrounding components through the PCB and the ambient.

Table 13-14. θ_{jc} [°C/W] for a CPGA Package with and without a Heat Sink (CPGA)

	No Heat Sink	With Heat Sink
Average θ_{jc}	1.7	1.25

Table 13-15. θ_a [°C/W] for Different Heat Sink Heights and Air Flow Rates (CPGA)

	θ_{ja} [°C/W] vs Air Flow Rate [LFM]					
Heat Sink Height	**0**	**100**	**200**	**400**	**600**	**800**
0.25”	10.6	9.5	8.1	5.9	5.1	4.5
0.35”	10.3	9.0	7.5	5.5	4.8	4.3
0.45”	9.9	8.5	6.8	5.1	4.4	4.0
0.55”	9.6	8.0	6.2	4.7	4.1	3.8
0.65”	9.2	7.5	5.8	4.5	3.9	3.6
0.80”	8.5	6.8	5.4	4.1	3.7	3.5
1.00”	7.8	6.1	5.1	4.1	3.6	3.3
1.20”	7.4	5.8	4.8	3.9	3.5	3.3
1.40”	6.9	5.4	4.5	3.7	3.4	3.2
1.50”	6.7	5.3	4.3	3.6	3.4	3.2
None	16.2	15.5	14.3	12.2	10.3	9.2

Table 13-16. θ_{ca} [°C/W] for Different Heat Sink Heights and Air Flow Rates (PPGA)

	θ_{ca} [°C/W] vs Air Flow Rate [LFM]					
Heat Sink Height	**0**	**100**	**200**	**400**	**600**	**800**
0.25”	9.0	7.9	6.5	4.3	3.5	2.9
0.35”	8.7	7.4	5.9	3.9	3.2	2.7
0.45”	8.3	6.9	5.2	3.5	2.8	2.4
0.55”	8.0	6.4	4.6	3.1	2.5	2.2
0.65”	7.6	5.9	4.2	2.9	2.3	2.0
0.80”	6.9	5.2	3.8	2.5	2.1	1.9
1.00”	6.2	4.5	3.5	2.5	2.0	1.7
1.20”	5.8	4.2	3.2	2.3	1.9	1.7
1.40”	5.3	3.8	2.9	2.1	1.8	1.6
1.50”	5.1	3.7	2.7	2.0	1.8	1.6
None	13.0	12.3	11.4	8.0	6.6	5.7

NOTE: θ_{ca} is case-to-ambient thermal resistance. θ_{ca} values shown in this table are typical values. The actual θ_{ca} values depend on the heat sink fin design, the interface between heat sink and package, the air flow in the system, and thermal interactions between CPU and surrounding components through the PCB and the ambient.

Table 13-17. θ_{jc} [°C/W] for a PPGA CPGA Package with and without a Heat Sink (PPGA)

	No Heat Sink	With Heat Sink
Average θ_{jc}	1.3	0.50

Table 13-18. θ_{ja} [°C/W] for Different Heat Sink Heights and Air Flow Rates (PPGA)

	θ_{ja} [°C/W] vs Air Flow Rate [LFM]					
Heat Sink Height	**0**	**100**	**200**	**400**	**600**	**800**
0.25”	9.5	8.4	7.0	4.8	4.0	3.4
0.35”	9.2	7.9	6.4	4.4	3.7	3.2
0.45”	8.8	7.4	5.7	4.0	3.3	2.9
0.55”	8.5	6.9	5.1	3.6	3.0	2.7
0.65”	8.1	6.4	4.7	3.4	2.8	2.5
0.80”	7.4	5.7	4.3	3.0	2.6	2.4
1.00”	6.7	5.0	4.0	3.0	2.5	2.2
1.20”	6.3	4.7	3.7	2.8	2.4	2.2
1.40”	5.8	4.3	3.4	2.6	2.3	2.1
1.50”	5.6	4.2	3.2	2.5	2.3	2.1
None	14.3	13.6	12.7	9.3	7.9	7.0

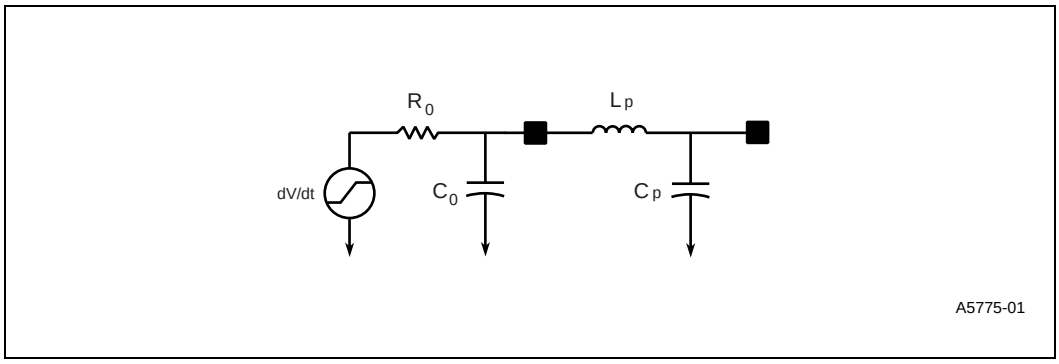
13.8 Electrical Characteristics

Electrical characteristic are discussed below. For more indepth coverage of electrical information please refer to Chapter 4: Performance Characteristics of IC Packages.

13.8.1 I/O Buffer

The package I/O model for components in PPGA packages is shown in Figure 13-16 as a first order buffer model. R_0 and C_0 values are independent of the package. Lp is the package inductance and includes bond wire inductance, trace inductance, pin inductance and socket inductance. Cp is the package capacitance and consists primarily of trace capacitance and socket capacitance. In this model, an effective inductance is used for the bond wire. Both self and mutual inductance are taken into account. The pin and its socket are considered as a single entity and a typical inductance value of 4.5 nH is used. A typical value of 1.0 pF is used for the socket capacitance.

Figure 13-16. First Order I/O Buffer Model for PPGA



13.8.2 Signal Quality

Intel has performed noise measurements on components in both CPGA and PPGA packages. The results show that at the component level, the PPGA packages are comparable to the CPGA packages. In addition, the results indicate that all PPGA parts have a higher mean-core-power supply level than CPGA parts.

13.8.3 EMI

The Federal Communications Commission (FCC) has set limits on the maximum radiation from electrical systems. Each component in a system should not exceed the level that is allocated to it. Electromagnetic Interference (EMI) levels from components in CPGA and PPGA packages have been measured with and without heat sinks attached. Measurements were performed up to a core clock frequency of 280 MHz. EMI levels are well below critical levels at all clock speeds tested. There is no significant EMI performance difference between CPGA and PPGA.

13.9 Revision History

- Added µPGA
- Added FC-PGA
- General review of chapter with modifications