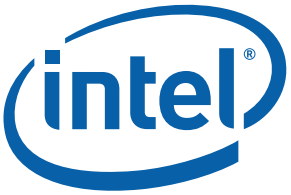

Intel® Xeon® Processor D-1500 NS Product Family and Intel® Xeon® Processor D-1600 NS Product Family

Datasheet - Volume 3 of 4: Electrical

April 2019

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Revision History

Document Number	Revision Number	Description	Date
336288	001	• Initial release of the document.	July 2017
336288	002	• Updated Section 1.1.2 on Intel® QuickAssist Technology. • Updated Table 5.3 Storage Condition Ratings.	February 2018
336288	003	• Added LAN1_MDC1_LED1_1 to strap Table 2-24. • Removed pins from Table 2-24 that are not H/W straps.	March 2019
336288	004	• Added Statement of Volatility (SOV) in Section 1.3. • Removed pin D71 from Table 2-25. • Added information about D-1600 NS Processor Family SKUs electrical.	March 2019
336288	005	• Update Intel QuickData supported features in Section 1.2.1 • Updated description of LAN_NCSI_RXD0 and LAN_NCSI_RXD1 in Table 2-24. • Updated VCCRTC specifications in Table 4-1.	April 2019

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1 Introduction

The datasheet addendum provides functional descriptions of the Intel® Xeon® Processor D-1500 NS product family and Intel® Xeon® Processor D-1600 NS product family as they differ from the Intel® Xeon® processor D-1500 product family. This document is distributed as a part of the complete document consisting of six volumes.

Note: The Intel® Xeon® processor D-1500 NS product family and Intel® Xeon® Processor D-1600 NS product family are also referred to as the "SoC" throughout this document.

1.1 Changes to Thermal Design Power (TDP) Workload

The Intel® Xeon® D-1600 NS Processor Family has been optimized for use in some networking and storage applications. The workload assumed for maintaining the marked frequency (also called P1) at TDP is an average across the SPECint_rate2006 benchmark suite.

Note: The SPECint* benchmark is composed of 12 different sub-benchmarks.

For SKUs that offer Intel® QuickAssist Technology (Intel® QAT), it is assumed the Intel QAT engines are running a maximal Pubic Key Exchange (PKE) workload in addition to the processor core workload. The Intel® Xeon® D-1500 NS Processor Family and Intel® Xeon® D-1500 Processor Family assumed a more compute intensive core workload for the TDP operating point. Therefore, this new family of application optimized SKUs may not maintain their marked frequency while running some standard server test loads (SPECint, SPECfp*, or POV-Ray for example). Throttling can occur even if there is thermal margin to T_{CASE_MAX} as TDP is enforced by the SoC.

Intel recommends potential customers perform performance testing before committing to a design using these new processors and not rely solely on experience and frequency scaling projections to estimate expected performance.

1.2 Major Differences from the Intel® Xeon® Processor D-1500 Product Family

The high level differences between the Intel® Xeon® processor D-1500 product family and the Intel® Xeon® processor D-1500 NS and D-1600 product families are given below.

- SKUs with up to 8 cores are supported.
- Removed existing 10GBASE-KX4 ports.
- Added two 10GBASE-KR ports.
- Added two Ethernet MACs supporting the additional 10GBASE-KR ports.
- Replaced Intel® QuickData Technology version 3.3 with version 3.2
- Added Intel® QuickAssist Technology hardware version 1.7

1.2.1 Intel® QuickData Technology Version 3.2

The Intel QuickData Technology DMA engine supports 8 DMA channels. Its PCI configuration registers occupy functions 0-7 of device 4 on CPUBUSNO(0). PCI Device IDs are 6F20-6F27.

Only data movement commands are supported. RAID, XOR, and CRC opcodes are not supported.

Data movement commands only support memory-to-memory and memory-to-MMIO operations. MMIO-to-MMIO and MMIO-to-memory operations are not supported.

1.2.2 Intel® QuickAssist Technology

The integrated Intel® QuickAssist Technology (Intel® QAT) provides acceleration functions that can be used by the Intel® architecture cores. The acceleration services can be accessed by a standard PCIe* driver. To enhance communication between the Intel architecture and the Intel QAT, the Intel QAT implements rings via the ring controller to route messages between them.

Applications running on the Intel architecture core(s) can make use of the acceleration by calling the Intel QuickAssist Technology Application Programming Interfaces (APIs). The APIs communicate with the Intel QuickAssist Technology hardware via the PCI configuration space access and assisted rings stored in system memory.

Refer to the *Intel® QuickAssist Technology API Programmer's Guide*, which is incorporated herein by reference, and available at:

- https://01.org/packet-processing/intel%C2%AE-quickassist-technology-drivers-and-patches

Features

This product contains Intel® QuickAssist Technology hardware version 1.7.

- Symmetric cryptographic functions
  - Cipher operation
  - Hash/authenticate operation
  - Cipher-hash combined operation
  - Key derivation operation
- Public key functions
  - RSA operation
  - Diffie-Hellman operation
  - Digital signature standard operation
  - Key derivation operation
  - Elliptic curve cryptography: ECDSA and ECDH
- Compression/Decompression
  - Deflate

1.2.3 Integrated 10GbE Controllers

There are four 10 GbE Media Access Control (MACs) supporting a 10GBASE_KR Physical Layer. The physical layer supports speeds of 10 GbE and 1 GbE. Each physical interface provides the following electrical modes:

- 10GBASE-KR for backplane applications (IEEE* 802.3 clause 72)
- 1000BASE-KX for backplane applications (IEEE 802.3 clause 70)
- 10GBASE-KR interface to SFI PHY (Inphi CS4227)
- 10GBASE-KR interface to 10GBASE-T PHY (Intel X557-AT or X557-AT2)

The four MACs are grouped into two pairs of MACs. Signals unique to pair are prefixed with LAN0_ and LAN1_. Signals which are shared among all four ports (NC-SI and SMBUS management interface) begin with LAN_.

Both ports associated with LAN0 must be configured identically (that is, both for 10GBASE-KR, both for SFI, or both for 10GBASE-T). Similarly, both ports of LAN1 must have an identical configuration. However, LAN0 and LAN1 may be configured independently.

1.3 Electrical Specification Introduction

This addendum of the *Intel® Xeon® Processor D-1500 product family* Datasheet provides DC electrical specifications and signal definitions of the processor.

The target audience for this document is primarily system architects and board designers who are planning to develop a SoC-based microserver solution. Additionally, this document is also used by other system engineers such as system test engineers, software developers, and BIOS developers.

Note: The data contained within this document is preliminary and is subject to change.This data is the most accurate information available by the publication date. Electrical DC specifications are based on estimated I/O buffer behavior.

1.4 Statement of Volatility (S0V)

The Intel® Xeon® Processor D-1500 NS product family and Intel® Xeon® Processor D-1600 NS product family does not retain any end-user data when powered down.

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2 Signal Names and Descriptions

2.1 Overview

This chapter provides a detailed description of the signals and bootstrap definitions for the SoC. The signals are arranged in functional groups according to their associated interface.

Each signal description table has the following headings:

- **Signal:** The name of the signal.
- **Description:** A brief explanation of the signal function.
- **Power Rail:** Power rails used to supply power to the I/O signal are defined in Table 2-1.

Table 2-1. Buffer Power Rails

Power Rail	Description
VCCIO	1.05 I/O rail for the PCH. This rail is off in the S4 and S5 power states.
VCCIOIN	1.05V I/O rail for CPU.This rail is active in the S4 and S5 power states.
VCC	1.05V Core rail. This rail is inactive in the S4 and S5 power states, but powered in S0.
VCCSUS3_3	3.3V SUS rail. This rail is active in the S4 and S5 power states.
VCC3_3	3.3V Core rail. This rail is inactive in the S4 and S5 power states, but powered in S0.
VCCRTC	3.3V RTC Power rail
VDDQ	DDR4/DDR3L I/O Voltage (1.2V/1.35V)

Technology	Voltage (VDDR)	Speeds (MT/s)
DDR4	1.20V	1600, 1866, 2133
DDR3L	1.35V	1333, 1600

- **Direction and Type:** The buffer direction and type.
  - Buffer direction is input (I), output (O), or bi-directional (I/O or IO).
  - Buffer Types are defined in Table 2-2.

Table 2-2. Buffer Types

Buffer Type	Buffer Description
CMOS	CMOS buffers: 1.05V
CMOS_OD	Open Drain CMOS (ODCMOS) buffers: 1.05V tolerant
DDR4	DDR4 Buffer: 1.2V
SSTL	Source Series Terminated Logic (JEDEC SSTL_15)
PCI Express	PCI Express interface signals. These signals are compatible with PCI Express 3.0 Signaling Environment AC Specifications and are AC coupled. The buffers are not 3.3V tolerant. Refer to the PCIe specification.
Asynchronous	Signal has no timing relationship with any system reference clock.
Analog	Analog reference or output. May be used as a threshold voltage or for buffer compensation.

2.2 Name Convention

Table 2-3 provides the legend for interpreting the I/O Type field that appears the tables in this section.

Table 2-3. Signal Type Definitions

Type	Description
# or _N	Active low signal
CMOS	CMOS buffers
DDR	Double Data Rate
I	Input pin
I/O or IO	Bi-directional Input/Output pin
I/OD	Bi-directional Input/Open Drain output pin
NC	No Connection to pin
O	Output pin
OD	Open Drain output pin
NCTF/TP	Non Critical To Function pins/Test Point pins.
RSVD	Reserved Pin. This signal must be connected as described in signal description.
T/S	Tri-State pin

2.3 System DDR Memory Signals

Table 2-4. DDR Memory Signals (Sheet 1 of 4)

Signal Name	I/O Type	I/O Buffer Type	Internal Resistor PU/PD	Power Rail	Description
DDR Reference Clocks					
DDR{0/1}_CLK_DN[3:0] DDR{0/1}_CLK_DP[3:0]	O	SSTL		VDDQ	DDR4 Differential Clock: All address and control input signals are sampled on the crossing of the positive edge of CLK_DP and negative edge of CLK_DN. Output (read) data is referenced to the crossings of CLK_DP and CLK_DN (both directions of crossing).

Table 2-4. DDR Memory Signals (Sheet 2 of 4)

Signal Name	I/O Type	I/O Buffer Type	Internal Resistor PU/PD	Power Rail	Description
DDR Command Signals					
DDR{0/1}_MA[13:0] DDR{0/1}_MA14_WE_N DDR{0/1}_MA15_CAS_N DDR{0/1}_MA16_RAS_N	O	SSTL		VDDQ	**Memory Address**. Selects the Row address for Reads and writes, and the column address for activates. Also used to set values for DRAM configuration registers. MA[16], MA[15], and MA[14] are MUXed with RAS_N, CAS_N, and WE_N, respectively. **DDR4 Write Enable**: (active low). Used with CAS#, RAS#, and CS# to define commands. RAS, CAS, and WE (along with CS) define the command being entered. **DDR4 Column Address Strobe**: (active low). Used with CAS#, RAS#, and CS# to define commands. RAS, CAS, and WE (along with CS) define the command being entered. **DDR4 Row Address Strobe**: (active low). Used with CAS# and RAS# (along with CS#) to define commands. RAS, CAS, and WE (along with CS) define the command being entered. ***Note:*** If the SoC is configured to support DDR3 interface, DDR{0/1}_MA14_WE_N, DDR{0/1}_MA15_CAS_N and DDR{0/1}_MA16_RAS_N are mapped as DDR{0/1}_WE_N, DDR{0/1}_CAS_N and DDR{0/1}_RAS_N in DDR3 interface, respectively.
DDR{0/1}_BA[1:0]	O	SSTL		VDDQ	Bank Address. Defines the bank which is the destination for the current Activate, Read, Write, or Precharge command.
DDR{0/1}_BG[0]_BA[2] DDR{0/1}_BG[1]_MA[14]	O	SSTL		VDDQ	Bank Group. Defines which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRC cycle. ***Note:*** If the SoC is configured to support DDR3 interface, DDR{0/1}_BG[0]_BA[2] and DDR{0/1}_BG[1]_MA[14] are mapped as DDR{0/1}_BA[2] and DDR{0/1}_MA[14] in DDR3 interface, respectively.
DDR{0/1}_ACT_N_MA[15]	O	SSTL		VDDQ	Activate. When asserted, indicated MA[16:14] are command signals (RAS_N, CAS_N, WE_N). ***Note:*** If the SoC is configured to support DDR3 interface, this pin DDR{0/1}_ACT_N_MA[15] is mapped as DDR{0/1}_MA[15] in DDR3 interface.
DDR{0/1}_PAR	O	SSTL		VDDQ	Even parity across Address and Command.
DDR Control Signals					
DDR{0/1}_CS_N[1:0] DDR{0/1}_CS_N[5:4]	O	SSTL		VDDQ	DDR4 Chip Select: (active low). Each signal selects one rank as the target of the command and address. These signals determine whether a command is valid in a given cycle for the devices connected to it. All commands are masked when CS# is registered HIGH. CS# provides for external Rank selection on systems with multiple Ranks. CS# is considered part of the command code.

Table 2-4. DDR Memory Signals (Sheet 3 of 4)

Signal Name	I/O Type	I/O Buffer Type	Internal Resistor PU/PD	Power Rail	Description
DDR{0/1}_CKE[3:0]	O	SSTL		VDDQ	DDR4 Clock Enable: (active high). CKE is used for power control of the DRAM devices. For the DRAM Devices: CKE HIGH activates, and CKE LOW deactivates, internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Pre-charge Power Down and Self-Refresh operation (all banks idle) or Active Power Down (row Active in any bank). CKE is synchronous for a power down entry and exit, and for self-refresh entry. CKE is asynchronous for self-refresh exit. After VREF has become stable during the power-on and initialization sequence, it must be maintained for proper operation of the CKE receiver. For proper self-refresh entry and exit, VREF must be maintained to this input. CKE must be maintained HIGH throughout read and write accesses. Input buffers, excluding CLK_DP/DN, ODT, and CKE are disabled during power down. Input buffers, excluding CKE, are disabled during self-refresh.
DDR{0/1}_ODT[3:0]	O	SSTL		VDDQ	DDR4 On-Die Termination Enable: (active high). Enables DRAM on die termination during Data Write or Data Read transactions. ODT (registered HIGH) enables termination resistance internal to the DDR device SDRAM. When the ODT feature is enabled, it is dynamically enabled for the receiver of the data. The SoC does this internally for read data returning from the DRAM devices. For write data to the DRAM devices, the ODT pins are asserted to enable ODT within the DRAM devices themselves. Because ODT consumes power, when the feature is enabled, it is control dynamically by the SoC. ODT impacts the DQ, DQS, and DM signals. The ODT pin is ignored by the DDR devices if the EMR(1) is programmed to disable ODT. One pin per rank.
DDR Data Signals					
DDR{0/1}_DQ[63:0]	I/O	SSTL		VDDQ	DDR4 Data Bus: Memory read and write data. Data signal interface to the SDRAM data bus. These 64-bit signals have 8-byte lanes, and each byte lane has a corresponding strobe pair.
DDR{0/1}_DQS_DP[17:0] DDR{0/1}_DQS_DN[17:0]	I/O	SSTL		VDDQ	Data strobes. Differential pair, Data/ECC Strobe. Differential strobes latch data/ECC for each DRAM. Different numbers of strobes are used depending on whether the connected DRAMs are x4,x8. Driven with edges in center of data, receive edges are aligned with data edges.
DDR{0/1}_ECC[7:0]	I/O	SSTL		VDDQ	Check bits. An error correction code is driven along with data on these lines for DIMMs that support that capability.

Table 2-4. DDR Memory Signals (Sheet 4 of 4)

Signal Name	I/O Type	I/O Buffer Type	Internal Resistor PU/PD	Power Rail	Description
DDR Miscellaneous Signals					
DDR{0/1}_ALERT_N/ PAR_ERR_N	I	SSTL		VDDQ	DDR4 Alert: it has multi functions such as CRC error flag, Command and Address Parity error flag. If there is error in CRC, then ALERT_N goes low for the period time interval and goes back high. If there is an error in Command Address Parity Check, then ALERT_N goes LOW for a relatively long period until the on going DRAM internal recovery transaction is complete. ***Note:*** If the SoC is configured to support DDR3 interface, this pin is mapped as DDR{0/1}_PAR_ERR_N for DDR 3 interface. It indicates Parity Error detected by the DIMM (one for each channel).
DRAM_PWR_OK	I	CMOS		VCCIOIN	Power good for VCCD rail used by the DRAM. This is an input signal used to indicate to the VCCD power supply is stable for memory channels.
DDR_PWRGOOD	I	CMOS		VCCIOIN	Power good for both VCCD and VCCIN power rails.
DDR3_4_STRAP	I	CMOS	PU 3.5K-6.5K	VCCIOIN	DDR3 and DDR4 selection strap. If this pin is pulled low = DDR3; if this pin is pulled high = DDR4.
DDR_RCOMP[2:0]	I	CMOS		VCCIOIN	System memory impedance compensation. Impedance compensation must be terminated on the system board using a precision resistor.
DDR_SCL	I/OD	CMOS OD		VCCIOIN	SMBus clock for the dedicated interface to the serial presence detect (SPD) and thermal sensors (TSoD) on the DIMMs.
DDR_SDA	I/OD	CMOS OD		VCCIOIN	SMBus Data for the dedicated interface to the serial presence detect (SPD) and thermal sensors (TSoD) on the DIMMs.
DDR_VREF	O	Analog		N/A	Voltage reference for the Command/Address to the DIMMs.
DDR_VREFDQ[1:0]	O	Analog		N/A	Voltage reference for system memory reads/ writes.
DDR_RESET_N	O	CMOS 1.2V		VCCD	System memory reset: Reset signal from processor to DRAM devices on the DIMMs.

2.4 PCI Express* 3.0 Interface Signals

Table 2-5. PCI Express Signals (Sheet 1 of 2)

Signal Name	I/O Type	I/O Buffer Type	Power Rail	Description
PE1_RX_DN[15:0] PE1_RX_DP[15:0]	I	PCI Express*	VCCIOIN	PCIe* Receive Data Input
PE1_TX_DN[15:0] PE1_TX_DP[15:0]	O	PCI Express	VCCIOIN	PCIe Transmit Data Output
PE2_RX_DN[7:0] PE2_RX_DP[7:0]	I	PCI Express	VCCIOIN	PCIe Receive Data Input

Table 2-5. PCI Express Signals (Sheet 2 of 2)

Signal Name	I/O Type	I/O Buffer Type	Power Rail	Description
PE2_TX_DN[7:0] PE2_TX_DP[7:0]	O	PCI Express	VCCIOIN	PCIe Transmit Data Output
PE_HP_SCL	I/OD	Open Drain CMOS	VCCIOIN	PCI Express Hot-Plug SMBus Clock: Provides PCI Express hot-plug support via a dedicated SMBus interface. Requires an external General Purpose Input/Output (GPIO) expansion device on the platform.
PE_HP_SDA	I/OD	Open Drain CMOS	VCCIOIN	PCI Express Hot-Plug SMBus Data: Provides PCI Express hot-plug support via a dedicated SMBus interface. Requires an external General Purpose Input/Output (GPIO) expansion device on the platform.

2.5 PECI Signal

Table 2-6. PECI Signals

Signal Name	I/O Type	I/O Buffer Type	Internal Resistor PU/PD	Power Rail	Description
PECI_CPU	I/O	CMOS		VCCIOIN	Platform Environment Control Interface (PECI) is the serial sideband interface to the SoC integrated processor and is used primarily for thermal, power and error management.
PECI_PCH	I/O	CMOS	PD 350 Ohm	P1V05_PROC_IO	Platform Environment Control Interface (PECI) is the serial sideband interface to the SoC integrated PCH.

2.6 JTAG and TAP Signals

Table 2-7. JTAG Signals (Sheet 1 of 2)

Signal Name	I/O Type	I/O Buffer Type	Internal Resistor PU/PD	Power Rail	Description
JTAG_TCK_CPU	I	CMOS	PD 3.5K-6.5K	VCCIOIN	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
JTAG_TRST_N_CPU	I	CMOS	PU 3.5K-6.5K	VCCIOIN	TRST_N (Test Reset) resets the Test Access Port (TAP) logic. TRST_N must be driven low during power on reset.
JTAG_TMS_CPU	I	CMOS	PU 3.5K-6.5K	VCCIOIN	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
JTAG_TDI_CPU	I	CMOS	PU 3.5K-6.5K	VCCIOIN	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
JTAG_TDO_CPU	O	CMOS OD		VCCIOIN	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
PRDY_N	O	CMOS		VCCIOIN	Probe Mode Ready is a processor output used by debug tools to determine processor debug readiness.
PREQ_N	I/O	CMOS		VCCIOIN	Probe Mode Request is used by debug tools to request debug operation of the processor.

Table 2-7. JTAG Signals (Sheet 2 of 2)

Signal Name	I/O Type	I/O Buffer Type	Internal Resistor PU/PD	Power Rail	Description
BPM_N[7:0]	I/O	CMOS OD		VCCIOIN	Breakpoint and Performance Monitor Signals: I/O signals from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance. These are 100 MHz signals.
JTAG_TCK_PCH	I	CMOS	PD 10K-45K ohm	VCCIOIN	**Test Clock Input (TCK):** The test clock input provides the clock for the JTAG test logic.
JTAG_TDO_PCH	O	CMOS OD		VCCIOIN	**Test Data Output (TDO):** TDO is the serial output for test instructions and data from the test logic defined in this standard.
JTAG_TMS_PCH	I	CMOS	PU 10K - 45K ohm	VCCIOIN	**Test Mode Select (TMS):** The signal is decoded by the Test Access Port (TAP) controller to control test operations.
JTAG_TDI_PCH	I	CMOS	PU 10K - 45K ohm	VCCIOIN	**Test Data Input (TDI):** Serial test instructions and data are received by the test logic at TDI
DEBUG_EN_N	I	CMOS	PU 3.5K-6.5K	VCCIOIN	This pin is used to force debug to be enabled when the Intel® In-Target Probe (Intel® ITP) is connected to the main board. This allows debug to occur beginning from cold boot.
PWR_DEBUG_N	I	CMOS	PU 3.5K-6.5K	VCCIOIN	Debug signal for power debug using Intel ITP.
EAR_N	I	CMOS	PU 3.5K-6.5K	VCCIOIN	External Alignment of Reset, used to bring the processor up into a deterministic state.

2.7 UART Signals

Table 2-8. UART Signals

Signal Name	I/O Type	I/O Buffer Type	Internal Resistor PU/PD	Power Rail	Description
UART_RXD[1:0]	I	CMOS		VCCIOIN	Receiver input for UART port 0 and 1. Serial receive data.
UART_TXD[1:0]	O	CMOS		VCCIOIN	Transmitter output for UART port 0 and 1. Serial transmit data.

2.8 Serial Interrupt Signals

Table 2-9. Serial Interrupt Request Interface Signals

Signal Name	I/O Type	Internal Resistor PU/PD	Power Rail	Description
SERIRQ_DATA	I/O	PU 3.5K-6.5K	VCCIOIN	Serial Interrupt Request Data signal
SERIRQ_DIR	O	N/A	VCCIOIN	Serial Interrupt Request Direction signal: Input/Output direction control for the SERIRQ_DATA pin.
SERIRQ_CLK	I	PD 3.5K-6.5K	VCCIOIN	33 MHz Serial Interrupt Request Clock signal. SoC integrated 33 MHz clock could be the clock source.

2.9 SVID Signals

Table 2-10. SVID Signals

Signal Name	I/O Type	Internal Resistor PU/PD	Power Rail	Description
SVID_ALERT_N	I		VCCIOIN	SVID Alert (Serial Voltage Identification Alert): (active low). Used by VR to signal that the prior request has not reached the requested operating point.
SVID_DATA	I/OD		VCCIOIN	SVID Data (Serial Voltage Identification Data): Bi-Directional signal. Used as data communication interface between the SoC and VR.
SVID_CLK	OD		VCCIOIN	SVID Clock (Serial Voltage Identification Clock): The SoC and VR use this clock for communication on the SVID Data bus. SoC SVID requests are driven out on SVID Data with this clock and are registered in the VR using this for the clock. When the VR responds, it also uses this clock to drive the data.

2.10 Miscellaneous Signals

Table 2-11. Misc. Signals (Sheet 1 of 5)

Signal Name	I/O Type	Internal Resistor PU/PD	Power Rail	Description
CATERR_N	I/O		VCCIOIN	Indicates that the system has experienced a fatal or catastrophic error and cannot continue to operate. The processor will assert CATERR_N for unrecoverable machine check errors and other internal unrecoverable errors. It is expected that every processor in the system will wire-OR CATERR_N for all processors. Since this is an I/O ball, external agents are allowed to assert this ball which will cause the processor to take a machine check exception. This signal is sampled after PWRGOOD assertion. CATERR_N is used for signaling the following types of errors: • Legacy MCERRs, CATERR_N is asserted for 16 BCLKs. • Legacy IERRs, CATERR_N remains asserted until warm or cold reset.
ERROR_N[2:0]	OD		VCCIOIN	Error status signals for integrated I/O (IIO) unit: • 0 = Hardware correctable error (no operating system or firmware action necessary) • 1 = Non-fatal error (operating system or firmware action required to contain and recover) • 2 = Fatal error (system reset likely required to recover)
PMSYNC_CPU	I		VCCIOIN	Power Management Sync. A sideband signal to communicate power management status from the integrated PCH to the integrated processor in SoC.
MEM_HOT_N	I/O		VCCIOIN	Memory throttle control. Signals that a DIMM is exceeding its temperature limit. MEM_HOT_N signal has two modes of operation - input and output mode. Input mode is externally asserted and is used to detect external events such as VR_HOT# from the memory voltage regulator and causes the processor to throttle the appropriate memory channels. Output mode is asserted by the processor known as level mode. In level mode, the output indicates that a particular branch of memory subsystem is hot.

Table 2-11. Misc. Signals (Sheet 2 of 5)

Signal Name	I/O Type	Internal Resistor PU/PD	Power Rail	Description
THERMTRIP_N	OD		P1V05_ PROC_IO	Assertion of THERMTRIP_N (Thermal Trip) indicates one of two possible critical over-temperature conditions: One, the processor junction temperature has reached a level beyond which permanent silicon damage may occur and Two, the system memory interface has exceeded a critical temperature limit set by BIOS. Measurement of the processor junction temperature is accomplished through multiple internal thermal sensors that are monitored by the Digital Thermal Sensor (DTS). Simultaneously, the Power Control Unit (PCU) monitors external memory temperatures via the dedicated SMBus interface to the DIMMs. If any of the DIMMs exceed the BIOS defined limits, the PCU will signal THERMTRIP_N to prevent damage to the DIMMs. Once activated, the processor will stop all execution and shut down all PLLs. To further protect the processor, its core voltage (V_{CCIN}), V_{CCD}, V_{CCIOIN} supplies must be removed following the assertion of THERMTRIP_N. Once activated, THERMTRIP_N remains latched until RESET_N is asserted. While the assertion of the RESET_N signal may de-assert THERMTRIP_N, if the processor's junction temperature remains at or above the trip level, THERMTRIP_N will again be asserted after RESET_N is de-asserted. This signal can also be asserted if the system memory interface has exceeded a critical temperature limit set by BIOS.
PWRGOOD_CPU	I		VCCIOIN	PWRGOOD_CPU is an integrated processor input. The processor requires this signal to be a clean indication that all processor clocks and power supplies are stable and within their specifications. “Clean” implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD_CPU can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD_CPU. PWRGOOD_CPU transitions from inactive to active when all supplies except VCCIN are stable. The signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
PROCHOT_N	I/OD		VCCIOIN	PROCHOT_N will go active when the integrated processor temperature monitoring sensor detects that the integrated processor has reached its maximum safe operating temperature. This indicates that the integrated processor Thermal Control Circuit has been activated, if enabled. This signal can also be driven to the integrated processor to activate the Thermal Control Circuit. This signal is sampled after PWRGOOD assertion. If PROCHOT_N is asserted at the deassertion of RESET_N, the processor will tristate its outputs.
BIST_ENABLE	I	PU 3.5K-6.5K	VCCIOIN	BIST Enable Strap. Input which allows the platform to enable or disable built-in self test (BIST) on the processor. This signal is pulled up on the die.
BMCINIT	I	PD 3.5K-6.5K	VCCIOIN	BMC Initialization Strap. Indicates whether Service Processor Boot Mode should be used. • 0: Service Processor Boot Mode Disabled. • 1: Service Processor Boot Mode Enabled. In this mode of operation, the processor performs the absolute minimum internal configuration and then waits for the service processor to complete its initialization. The socket boots after receiving a “GO” handshake signal via a firmware scratchpad register. This signal is pulled down on the die.
FIVR_FAULT	O		VCCIOIN	Indicates THERMTRIP was signaled due to an internal error with the integrated voltage regulator rather than an over temperature condition. Must be qualified with THERMTRIP_N assertion.
SAFE_MODE_BOOT	I	PD 3.5K-6.5K	VCCIOIN	Safe Mode Boot Strap. SAFE_MODE_BOOT allows the processor to wake up safely by disabling all clock gating. This allows BIOS to load registers or patches if required. This signal is sampled after PWRGOOD assertion. The signal is pulled down on the die.

Table 2-11. Misc. Signals (Sheet 3 of 5)

Signal Name	I/O Type	Internal Resistor PU/PD	Power Rail	Description
TXT_AGENT	I	PD 3.5K-6.5K	VCCIOIN	Intel® Trusted Execution Technology (Intel® TXT) Agent Strap 0 = Default. The socket is not the Intel TXT Agent. 1 = The socket is the Intel TXT Agent. This signal is pulled down on the die.
TXT_PLTEN	I	PU 3.5K-6.5K	VCCIOIN	Intel TXT Platform Enable Strap 0 = The platform is not Intel TXT enabled. 1 = Default. The platform is Intel TXT enabled. When this is set, Intel TXT functionality requires user to explicitly enable Intel TXT via BIOS setup. This signal is pulled up on the die.
TEST[1:0]	O	None	VCCIOIN	Test[1:0] must be individually connected to an appropriate power source or ground through a resistor for proper SoC operation.
SLP_S3_CPU_N	I	None	VCCIOIN	S3 Sleep Control coming from integrated PCH to integrated processor
RSMRST_CPU_N	I	None	VCCIOIN	Resume Well Reset for CPU logic
THROTTLE_PECI_ID2	O		VCCIOIN	Signal from SoC integrated processor to integrated PCH for throttling. Also this pin is a strap for PECI ID[2] and it is sampled at rising edge of LAN_PWRGOOD.
PCHHOT_CPU_N	I	None	VCCIOIN	SoC integrated PCH Hot indication to integrated processor
RESET_CPU_N	I	None	VCCIOIN	Global reset signal coming from integrated PCH to integrated processor.
PROCPWRGD_PCH	O	None	P1V05_PROC_IO	This pin is connected to integrated processor to indicate the integrated processor power is valid.
ADR_COMPLETE	O	None	VCCIOIN	Asynchronous DRAM Self-Refresh Complete
ADR_IN	I	PD 3.5K-6.5K	VCCIOIN	Asynchronous DRAM Self-Refresh Request
PM_SYNC_PCH	O	None	P1V05_PROC_IO	**Power Management Sync:** Provides state information from the integrated PCH to the integrated processor.
THERMTRIP_PCH_N	I	None	P1V05_PROC_IO	**Thermal Trip**: When low, this signal indicates that a thermal trip from the integrated processor occurred, and the integrated PCH will immediately transition to a S5 state. The integrated PCH will not wait for the integrated processor stop grant cycle since the processor has overheated.
SOC_IREF	I	None	VCCVRM	SoC Internal Reference Voltage
SOC_RCOMP	I	None	VCCVRM	SoC Impedance Compensation Input
MFG_MODE_STRAP	I	9K-50K PD	VCCSUS3_3	Flash Descriptor Security Override This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal weak pull-down is disabled after PLTRST_N de-asserts, but the signal will be strongly driven low instead. 2. Asserting MFG_MODE_STRAP pin high on the rising edge of PWROK will also halt Intel ME after chipset bring up and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug. 3. This signal is in the Suspend well.
RTCRST_N	I	None	RTC	**RTC Reset:** When asserted, this signal resets register bits in the RTC well. ***Notes:*** 1. Unless CMOS is being cleared (only to be done in the G3 power state), the RTCRST_N input must always be high when all other RTC power planes are on. 2. In the case where the RTC battery is dead or missing on the platform, the RTCRST_N pin must rise before the DPWROK pin.

Table 2-11. Misc. Signals (Sheet 4 of 5)

Signal Name	I/O Type	Internal Resistor PU/PD	Power Rail	Description
SRTCRST_N	I	None	RTC	**Secondary RTC Reset:** This signal resets the manageability register bits in the RTC well when the RTC battery is removed. ***Notes:*** 1. The SRTCRST_N input must always be high when all other RTC power planes are on. 2. In the case where the RTC battery is dead or missing on the platform, the SRTCRST_N pin must rise before the RSMRST_N pin.
INTVRMEN	I	None	RTC	**Internal Voltage Regulator Enable:** When pulled high, this signal enables the internal 1.05 V regulators for the Suspend well in the integrated PCH. This signal must remain asserted for the VRMs to behave properly (no glitches allowed). This signal does not have an internal resistor; an **external** resistor is **required**. 0 = DCPSUS1, DCPSUS2 and DCPSUS3 are powered from an external power source (should be connected to an external VRM). External VR powering option is for Mobile Only; Desktop/Server/ Workstation should not pull the strap low. 1 = Integrated VRMs enabled. DCPSUS1, DCPSUS2 and DCPSUS3 can be left as No Connect. ***Notes:*** 1. This signal is always sampled. 2. This signal is in the RTC well.
PME_N	I/OD	15K-40K PU	VCCSUS3_3	**PCI Power Management Event**: PCI peripherals drive PME_N to wake the system from low-power states S1–S5. PME_N assertion can also be enabled to generate an SCI from the S0 state. In some cases the integrated PCH may drive PME_N active due to an internal wake event. The integrated PCH will not drive PME_N high, but it will be pulled up to VccSUS3_3 by an internal pull-up resistor. PME_N is still functional and can be used with PCI legacy mode on platforms using a PCIe-to-PCI bridge. Downstream PCI devices would need to have PME_N routed from the connector to the PCH PME_N pin.
DSWODVREN	I	None	RTC	**DeepSx Well Internal Voltage Regulator Enable:** This signal enables the internal DSW 1.05V regulators and must be always pulled-up to VCCRTC. DeepSx Well On Die Voltage Regulator Enable. This signal does not have an internal resistor; an **external** resistor is **required**. 0 = **Disable** Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This mode is only supported for testing environments. 1 = **Enable** DSW 3.3V-to-1.05V Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This must always be pulled high on production boards. ***Notes:*** 1. This signal is always sampled. 2. This signal is in the RTC well.
SPKR	O	15K-40K PD	VCC3_3	**Speaker:** The SPKR signal is the output of counter 2 and is internally "ANDed" with Port 61h Bit 1 to provide Speaker Data Enable. This signal drives an external speaker driver device, which in turn drives the system speaker. Upon PLTRST_N, its output state is 0. ***Note:*** SPKR is sampled as a functional strap. There is a weak integrated pull-down resistor on SPKR pin which is disabled after PLTRST_N de-asserts.
GPIO35_NMI_N	IO/OD	15K-40K PU in NMI mode Only	VCC3_3	**NMI_N:** This is an NMI event indication to an external controller (such as a BMC) on server/workstation platforms. When operating as NMI event indication pin function (enabled when "NMI SMI Event Native GPIO Enable" soft strap [PCHSTRP9:bit 16] is set to 1), the pin is an open drain (OD).
GPIO20_SMI_N	IO/OD	15K-40K PU in SMI mode Only	VCC3_3	**SMI_N:** This is an SMI event indication to an external controller (such as a BMC) on server/workstation platforms. When operating as SMI event indication pin function (enabled when "NMI SMI Event Native GPIO Enable" soft strap [PCHSTRP9:bit 16] is set to 1), the pin is an open drain (OD).

Table 2-11. Misc. Signals (Sheet 5 of 5)

Signal Name	I/O Type	Internal Resistor PU/PD	Power Rail	Description
SUS_STAT_N_GPIO61	O/IO	None	VCCSUS3_3	**Suspend Status:** This signal is asserted by the PCH to indicate that the system will be entering a low power state soon. This can be monitored by devices with memory that need to switch from normal refresh to suspend refresh mode. It can also be used by other peripherals as an indication that they should isolate their outputs that may be going to powered-off planes. This pin may also be used as GPIO61.
SLP_WLAN_N_GPIO29_MGPIO3	O/IO	None	VCCSUS3_3	**WLAN Sub-System Sleep Control:** When SLP_WLAN_N is asserted, power can be shut off to the external wireless LAN device. SLP_WLAN_N will always will be de-asserted in S0. ***Note:*** The selection between native and GPIO mode is based on a soft strap. The soft strap default is '0', SLP_WLAN_N mode. The native and GPIO functionality is only available when the SUS well is powered. Set soft strap to '1' to use the GPIO mode.
BMBUSY_N_GPIO0	I/IO	None	VCC3_3	**Bus Master Busy:** Generic bus master activity indication driven into the PCH. This signal can be configured to set the PM1_STS.BM_STS bit. The signal can also be configured to assert indications transmitted from the integrated PCH to the integrated processor using the PMSYNCH pin.

2.11 USB Interface

Note: The USB2.0 signals in the integrated PCH integrate pull-down resistors and provide an output driver impedance of 45 Ω that requires no external series resistor. No external pull-up/pull-down resistors should be added to the USB2.0 signals. USB ports not needed can be left floating as No Connect.

Note: The voltage divider formed by the device pull-up and the host pull-down will guarantee the data wire will park at a safe voltage level, which is below the VBUS value. This ensures that the host/hub will not see 5V at the wire when inter-operating with devices that have VBUS at 5V.

Note: All USB 2.0 register addresses throughout the EDS correspond to the external pin names. Refer to the table below to know exactly how the USB pins are mapped to the different internal ports within the xHCI and EHCI controllers.

Table 2-12. USB Interface Signals (Sheet 1 of 2)

Name	xHCI Port	EHCI Port	Type	Description
USB2_DP0 USB2_DN0	0	0	I/O	**USB 2.0 Port 0 Transmit/Receive Differential Pair 0:** This USB 2.0 signal pair can be routed to xHCI or EHCI Controller 1 through software and should map to a USB connector with one of the overcurrent OC Pins 0-3.
USB2_DP1 USB2_DN1	1	1	I/O	**USB 2.0 Port 1 Transmit/Receive Differential Pair 1:** This USB 2.0 signal pair can be routed to xHCI or EHCI Controller 1 through software and should map to a USB connector with one of the overcurrent OC Pins 0-3.
USB2_DP2 USB2_DN2	2	2	I/O	**USB 2.0 Port 2 Transmit/Receive Differential Pair 2:** This USB 2.0 signal pair can be routed to xHCI or EHCI Controller 1 through software and should map to a USB connector with one of the overcurrent OC Pins 0-3.
USB2_DP3 USB2_DN3	3	3	I/O	**USB 2.0 Port 3 Transmit/Receive Differential Pair 3:** This USB 2.0 signal pair can be routed to xHCI or EHCI Controller 1 through software and should map to a USB connector with one of the overcurrent OC Pins 0-3.
USB3_TX_DP1 USB3_TX_DN1	1	N/A	O	**USB 3.0 Differential Transmit Pair 1:** These are USB 3.0-based outbound high-speed differential signals, mapped to High Speed I/O (HSIO) Port #1 and the xHCI Controller. It should map to a USB connector with one of the overcurrent (OC) pins 0 - 7.

Table 2-12. USB Interface Signals (Sheet 2 of 2)

Name	xHCI Port	EHCI Port	Type	Description
USB3_RX_DP1 USB3_RX_DN1	1	N/A	I	**USB 3.0 Differential Receive Pair 1: T**hese are USB 3.0-based inbound high-speed differential signals, mapped to High Speed I/O (HSIO) Port #1 and the xHCI Controller. It should map to a USB connector with one of the OC (overcurrent) pins 0 - 7.
USB3_TX_DP2 USB3_TX_DN2	2	N/A	O	**USB 3.0 Differential Transmit Pair 2:** These are USB 3.0-based outbound high-speed differential signals, mapped to High Speed I/O (HSIO) Port #2 and the xHCI Controller. It should map to a USB connector with one of the OC (overcurrent) pins 0 - 7.
USB3_RX_DP2 USB3_RX_DN2	2	N/A	I	**USB 3.0 Differential Receive Pair 2:** These are USB 3.0-based inbound high-speed differential signals, mapped to High Speed I/O (HSIO) Port #2 and the xHCI Controller. It should map to a USB connector with one of the OC (overcurrent) pins 0 - 7.
USB3_TX_DP5 USB3_TX_DN5	5	N/A	O	**USB 3.0 Differential Transmit Pair 5:** These are USB 3.0-based outbound high-speed differential signals, mapped to High Speed I/O (HSIO) Port #3 and the xHCI Controller. It should map to a USB connector with one of the OC (overcurrent) pins 0–7.
USB3_RX_DP5 USB3_RX_DN5	5	N/A	I	**USB 3.0 Differential Receive Pair 5:** These are USB 3.0-based inbound high-speed differential signals, mapped to High Speed I/O (HSIO) Port #3 and the xHCI Controller. It should map to a USB connector with one of the OC (overcurrent) pins 0–7.
USB3_TX_DP6 USB3_TX_DN6	6	N/A	O	**USB 3.0 Differential Transmit Pair 6:** These are USB 3.0-based outbound high-speed differential signals, mapped to High Speed I/O (HSIO) Port #4 and the xHCI Controller. It should map to a USB connector with one of the OC (overcurrent) pins 0–7.
USB3_RX_DP6 USB3_RX_DN6	6	N/A	I	**USB 3.0 Differential Receive Pair 6:** These are USB 3.0-based inbound high-speed differential signals, mapped to High Speed I/O (HSIO) Port #4 and the xHCI Controller. It should map to a USB connector with one of the OC (overcurrent) pins 0–7.
OC0#/GPIO59 OC1#/GPIO40 OC2#/GPIO41 OC3#/GPIO42 OC4#/GPIO43 OC5#/GPIO9 OC6#/GPIO10 OC7#/GPIO14	N/A	N/A	I	**Overcurrent Indicators**: These signals set corresponding bits in the USB controllers to indicate that an over-current condition has occurred. OC[7:0]# is the default (Native) function for these pins but they may be configured as GPIOs instead. OC pins are 3.3V tolerant. Sharing of OC pins is required to cover all USB connectors but no more than 1 OC line may be connected to a USB connector. OC[3:0]# should be connected with USB 2.0 ports 0–3 and any 4 of USB 3.0 ports. OC[7:4]# should be connected with any 4 of USB 3.0 ports.
USB2_RBIAS	N/A	N/A	O	**USB Resistor Bias:** Analog connection point for an external resistor that is used to set transmit currents and internal load resistors. It is recommended that a 22.6 Ω±1% resistor to ground be connected to this pin.
USB2_RBIAS#	N/A	N/A	I	**USB Resistor Bias Complement:** Analog connection point for an external resistor that is used to set transmit currents and internal load resistors. This signal should be connected directly to USBRBIAS.

2.12 SATA Signals

Table 2-13. SATA2 Signals (Sheet 1 of 2)

Signal Name	I/O Type	Internal Resistor PU/PD	Power Rail	Description
SATA_TX_DP0 SATA_TX_DN0	O	N/A	VCCIO	**Serial ATA Differential Transmit Pair 0:** These outbound SATA Port 0 high-speed differential signals support 1.5 Gb/s, 3 Gb/s and 6 Gb/s, and are mapped to HSIO Port 15. In compatible mode, SATA Port 0 is the primary master of SATA Controller 1.
SATA_RX_DP0 SATA_RX_DN0	I	N/A	VCCIO	**Serial ATA Differential Receive Pair 0:** These inbound SATA Port 0 high-speed differential signals support 1.5 Gb/s, 3 Gb/s and 6 Gb/s, and are mapped to HSIO Port 15. In compatible mode, SATA Port 0 is the primary master of SATA Controller 1.
SATA_TX_DP1 SATA_TX_DN1	O	N/A	VCCIO	**Serial ATA Differential Transmit Pair 1:** These outbound SATA Port 1 high-speed differential signals support 1.5 Gb/s, 3 Gb/s and 6 Gb/s, and are mapped to HSIO Port 16. In compatible mode, SATA Port 1 is the secondary master of SATA Controller 1.
SATA_RX_DP1 SATA_RX_DN1	I	N/A	VCCIO	**Serial ATA Differential Receive Pair 1:** These inbound SATA Port 1 high-speed differential signals support 1.5 Gb/s, 3 Gb/s and 6 Gb/s, and are mapped to HSIO Port 16. In compatible mode, SATA Port 1 is the secondary master of SATA Controller 1.
SATA_TX_DP2 SATA_TX_DN2	O	N/A	VCCIO	**Serial ATA Differential Transmit Pair 2:** These outbound SATA Port 2 high-speed differential signals support 1.5 Gb/s, 3 Gb/s and 6 Gb/s, and are mapped to HSIO Port 17. In compatible mode, SATA Port 2 is the primary slave of SATA Controller 1.
SATA_RX_DP2 SATA_RX_DN2	I	N/A	VCCIO	**Serial ATA Differential Receive Pair 2:** These inbound SATA Port 2 high-speed differential signals support 1.5 Gb/s, 3 Gb/s and 6 Gb/s, and are mapped to HSIO Port 17. In compatible mode, SATA Port 2 is the primary slave of SATA Controller 1.
SATA_TX_DP3 SATA_TX_DN3	O	N/A	VCCIO	**Serial ATA Differential Transmit Pair 3:** These outbound SATA Port 3 high-speed differential signals support 1.5 Gb/s, 3 Gb/s and 6 Gb/s, and are mapped to HSIO Port 18. In compatible mode, SATA Port 3 is the secondary slave of SATA Controller 1.
SATA_RX_DP3 SATA_RX_DN3	I	N/A	VCCIO	**Serial ATA Differential Receive Pair 3:** These inbound SATA Port 3 high-speed differential signals support 1.5 Gb/s, 3 Gb/s and 6 Gb/s, and are mapped to HSIO Port 18. In compatible mode, SATA Port 3 is the secondary slave of SATA Controller 1.
SATA_TX_DP4 SATA_TX_DN4	O	N/A	VCCIO	**Serial ATA Differential Transmit Pair 4:** These outbound SATA Port 4 high-speed differential signals support 1.5 Gb/s, 3 Gb/s and 6 Gb/s, and are mapped to HSIO Port 13. In compatible mode, SATA Port 4 is the primary master of SATA Controller 2. ***Note:*** Use FITC to set the soft straps that select this port as PCIe Port 1. Default configuration is SATA Port 4.
SATA_RX_DP4 SATA_RX_DN4	I	N/A	VCCIO	**Serial ATA Differential Receive Pair 4:** These inbound SATA Port 4 high-speed differential signals support 1.5 Gb/s, 3 Gb/s and 6 Gb/s, and are mapped to HSIO Port 13. In compatible mode, SATA Port 4 is the primary master of SATA Controller 2. ***Note:*** Use FITC to set the soft straps that select this port as PCIe Port 1. Default configuration is SATA Port 4.
SATA_TX_DP5 SATA_TX_DN5	O	N/A	VCCIO	**Serial ATA Differential Transmit Pair 5:** These outbound SATA Port 5 high-speed differential signals support 1.5 Gb/s, 3 Gb/s and 6 Gb/s, and are mapped to HSIO Port 14. In compatible mode, SATA Port 5 is the secondary master of SATA Controller 2. ***Note:*** Use FITC to set the soft straps that select this port as PCIe Port 2. Default configuration is SATA Port 5.
SATA_RX_DP5 SATA_RX_DN5	I	N/A	VCCIO	**Serial ATA Differential Receive Pair 5:** These inbound SATA Port 5 high-speed differential signals support 1.5 Gb/s, 3 Gb/s and 6 Gb/s, and are mapped to HSIO Port 14. In compatible mode, SATA Port 5 is the secondary master of SATA Controller 2. ***Note:*** Use FITC to set the soft straps that select this port as PCIe Port 2. Default configuration is SATA Port 5.

Table 2-13. SATA2 Signals (Sheet 2 of 2)

Signal Name	I/O Type	Internal Resistor PU/PD	Power Rail	Description
SATA0GP / GPIO21	I	None	VCC3_3	**Serial ATA 0 General Purpose:** When configured as SATA0GP, this is an input pin that is used as an interlock switch status indicator for SATA Port 0. Drive the pin to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open. The default use of this pin is GPIO21.
SATA1GP / GPIO19	I	15K-40K PU	VCC3_3	**Serial ATA 1 General Purpose:** When configured as SATA1GP, this is an input pin that is used as an interlock switch status indicator for SATA Port 1. Drive the pin to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open. The default use of this pin is GPIO19.
SATA2GP / GPIO36	I	15K-40K PD	VCC3_3	**Serial ATA 2 General Purpose:** When configured as SATA2GP, this is an input pin that is used as an interlock switch status indicator for SATA Port 2. Drive the pin to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open. The default use of this pin is GPIO36.
SATA3GP / GPIO37	I	15K-40K PD	VCC3_3	**Serial ATA 3 General Purpose:** When configured as SATA3GP, this is an input pin that is used as an interlock switch status indicator for SATA Port 3. Drive the pin to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open. The default use of this pin is GPIO37.
SATA4GP / GPIO16	I	15K-40K PU	VCC3_3	**Serial ATA 4 General Purpose:** When configured as SATA4GP, this is an input pin that is used as an interlock switch status indicator for SATA Port 4. Drive the pin to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open. The default use of this pin is GPIO16.
SATA5GP /GPIO49	I	15K-40K PU	VCC3_3	**Serial ATA 5 General Purpose:** When configured as SATA5GP, this is an input pin that is used as an interlock switch status indicator for SATA Port 5. Drive the pin to '0' to indicate that the switch is closed and to '1' to indicate that the switch is open. The default use of this pin is GPIO49.
SATALED#	OD	None	VCC3_3	**Serial ATA LED:** This signal is an open-drain output pin driven during SATA command activity. It is to be connected to external circuitry that can provide the current to drive a platform LED. When active, the LED is on. When tri-stated, the LED is off. An external pull-up resistor to Vcc3_3 is required.
SCLOCK /GPIO22	OD	None	VCC3_3	**SGPIO Reference Clock:** The SATA controller uses rising edges of this clock to transmit serial data, and the target uses the falling edge of this clock to latch data. The SClock frequency supported is 32 kHz. If SGPIO interface is not used, this signal can be used as GPIO22.
SLOAD / GPIO38	OD	None	VCC3_3	**SGPIO Load:** The controller drives a '1' at the rising edge of SCLOCK to indicate either the start or end of a bit stream. A 4-bit vendor specific pattern will be transmitted right after the signal assertion. If SGPIO interface is not used, this signal can be used as GPIO38.
SDATAOUT0 / GPIO39 SDATAOUT1 / GPIO48	OD	None	VCC3_3	**SGPIO Dataout:** Driven by the controller to indicate the drive status in the following sequence: drive 0, 1, 2, 3, 4, 5, 0, 1, 2... If SGPIO interface is not used, the signals can be used as GPIO.
SATA_RCOMP	I	None	VCCVRM	**Impedance Compensation Input:** Connected to a 7.5 kΩ (1%) precision external pull-up resistor to 1.5V.
SATA_IREF	I	None	VCCVRM	**Internal Reference Voltage:** Connect directly to 1.5V.

2.13 Clock Signals

Table 2-14. Clock Signals

Signal Name	I/O Type	Internal Resistor PU/PD	Power Rail	Description
CLKOUT_ITPXDP_DP CLKOUT_ITPXDP_DN	O	None	VCCIO	100 MHz PCIe 3.0 specification compliant differential output to processor XDP/Intel ITP connector on platform.
CLKIN_GND[4:1]_DP CLKIN_GND[4:1]_DN	I	None	VCCIO	Unused. Tie each signal to GND through a 10 kΩ resistor.
XTAL25_IN	I	None		Connection for 25 MHz crystal to integrated PCH oscillator circuit
XTAL25_OUT	O	None		Connection for 25 MHz crystal to integrated PCH oscillator circuit
REFCLK14IN	I	None	VCC3_3	Unused. Tie signal to GND through a 10 kΩ resistor.
CLKOUT_PEG_DP CLKOUT_PEG_DN	O	None	VCCIO	100 MHz PCIe 3.0 specification compliant differential output to a PCI Express device
CLKOUT_PCIE_P[7:0] CLKOUT_PCIE_N[7:0]	O	None	VCCIO	100 MHz PCIe 2.0 and PCIe 3.0 specification compliant differential output to PCI Express devices
CLKOUT_PCI[4:0]	O	10K-45K PD	VCC3_3	Single-Ended, 33 MHz outputs to various PCI connectors/devices. One of these signals must be connected to **CLKIN_PCILOOPBACK** to function as a 33 MHz clock loopback. This allows skew control for variable lengths of **CLKOUT_PCI[4:0]**.
CLKOUTFLEX1 / GPIO65; CLKOUTFLEX3 / GPIO67	O	10K-45K PD	VCC3_3	Configurable as a GPIO or as a programmable output clock which can be configured by using FITC to set ICC settings as one of the following: Default configuration is 33 MHz. • 33 MHz • 14.318 MHz • 48/24 MHz • DC Output logic '0'
DIFFCLK_BIASREF	I/O	None	VCCVRM	**Differential Clock Bias Reference**: Connected to an external precision resistor (7.5 K ohm ±1%) to 1.5V.
CLKIN_PCILOOPBACK	I	None	VCC3_3	33 MHz clock feedback input, to reduce skew between integrated PCH on-die 33 MHz clock and 33 MHz clock observed by connected devices.
ICLK_IREF	I/O	None	VCCVRM	**Internal Clock Bias Reference:** Connect directly to a quiet 1.5V supply.
RTCX1	I	None	RTC	**Crystal Input 1:** This signal is connected to the 32.768 kHz crystal. If no external crystal is used, then RTCX1 can be driven with the desired clock rate. **Max voltage allowed on this pin is 1.2V**.
RTCX2	O	None	RTC	**Crystal Input 2:** This signal is connected to the 32.768 kHz crystal. If no external crystal is used, then RTCX2 must be left floating. **Max voltage allowed on this pin is 1.2V**.

2.14 PCI Express Gen2 Interface Signals

Table 2-15. PCIe Express Gen 2 Interface Signals

Signal Name	I/O Type	Internal Resistor PU/PD	Power Rail	Description
PCIE_TX_DP[7:0]	O	N/A	VCCIO	PCI Express Transmit: Differential-pair output. 2.5 GT/s and 5.0 GT/s data rates supported.
PCIE_TX_DN[7:0]	O	N/A	VCCIO	PCI Express Transmit: Differential-pair output. 2.5 GT/s and 5.0 GT/s data rates supported.
PCIE_RX_DP[7:0]	I	N/A	VCCIO	PCI Express Receive: Differential-pair input. 2.5 GT/s and 5.0 GT/s data rates supported.
PCIE_RX_DN[7:0]	I	N/A	VCCIO	PCI Express Receive: Differential-pair input. 2.5GT/s and 5.0GT/s data rates supported.
PCIE_IREF	I	None	VCCVRM	Internal Reference Voltage: Connected directly to 1.5V
PCIE_RCOMP	I	None	VCCVRM	Impedance Compensation Input: Connected to a 7.5 K ohm (1%) precision external pull-up resistor to 1.5V

2.15 LPC Interface Signals

Table 2-16. LPC Signals

Signal Name	I/O Type	Internal Resistor PU/PD	Power Rail	Description
LAD[3:0]	I/O	15K-40K PU	VCC3_3	**LPC Multiplexed Command, Address, Data:** For LAD[3:0], internal pull-ups are provided.
LFRAME#	O	None	VCC3_3	**LPC Frame:** LFRAME# indicates the start of an LPC cycle, or an abort.
LDRQ0# LDRQ1#/GPIO23	I	15K-40K PU	VCC3_3	**LPC Serial DMA/Master Request Inputs:** LDRQ[1:0]# are used to request DMA or bus master access. These signals are typically connected to an external Super I/O device. An internal pull-up resistor is provided on these signals. LDRQ1# may optionally be used as GPIO23.

2.16 Power Management Signals

Table 2-17. Power Management Signals (Sheet 1 of 3)

Signal Name	I/O Type	Internal Resistor PU/PD	Power Rail	Description
APWROK	I	None	VCCSUS3_3	Active Sleep Well (ASW) Power OK: When asserted, this signal indicates that power to the ASW sub-system is stable. The ASW power rail is connected together with VCCIOIN power rail. APWROK may be tied together with PCH_PWROK signal in the Intel® Xeon® Processor D-1500 NS Product Family-based platform.
DPWROK	I	None	RTC	**DPWROK:** Power OK Indication for the VccDSW3_3 voltage rail. In Intel® Xeon® Processor D-1500 NS Product Family-based platform Deep Sleep Power rail is not supported, this input is tied together with RSMRST_N on platforms that do not support DeepSx. This signal is in the RTC well.
DRAMPWROK_PCH	OD	None	VCCIOIN	**DRAM Power OK:** This signal should connect to the SoC integrated processor's DRAM_PWR_OK pin. The integrated PCH asserts this pin to indicate when DRAM power is stable. This pin requires an external pull-up to VCCIOIN.

Table 2-17. Power Management Signals (Sheet 2 of 3)

Signal Name	I/O Type	Internal Resistor PU/PD	Power Rail	Description
SLP_A_N	O	None	VCCSUS3_3	**SLP_A_N:** This signal is used to control power to the active sleep well (ASW) of the PCH. This signal is unused.
SLP_S3_N	O	None	VCCSUS3_3	**S3 Sleep Control:** SLP_S3_N is for power plane control. This signal shuts off power to all non-critical systems when in S3 (Suspend To RAM), S4 (Suspend to Disk), or S5 (Soft Off) states
SLP_S4_N	O	None	VCCSUS3_3	**S4 Sleep Control**: SLP_S4_N is for power plane control. This signal shuts power to all non-critical systems when in the S4 (Suspend to Disk) or S5 (Soft Off) state. ***Note:*** This pin must be used to control the DRAM power in order to use the PCH's DRAM power-cycling feature
SLP_SUS_N	O	None	VCCSUS3_3	**DeepSx Indication:** DeepSx is not supported, this pin can be left unconnected.
SYS_PWROK	I	None	VCCSUS3_3	**System Power OK:** This generic power good input to the integrated PCH is driven and utilized in a platform-specific manner. While PWROK always indicates that the core wells of the PCH are stable, SYS_PWROK is used to inform the PCH that power is stable to some other system component(s) and the system is ready to start the exit from reset.
SYS_RESET_N	I	None	VCC3_3	**System Reset**: This signal forces an internal reset after being debounced. The integrated PCH will reset immediately if the SMBus is idle; otherwise, it will wait up to 25 ms ±2 ms for the SMBus to idle before forcing a reset on the system
SUSACK_N	I	9K-50K PU	VCCSUS3_3	**SUSACK_N:** Intel® Xeon® Processor D-1500 Product Family-based platform doesn't support Deep Sleep Power state. This pin is not used.
SUSWARN_N_SUSPWRDNACK_GPIO30	O	None	VCCSUS3_3	**SUSWARN_N:** This signal is multiplexed with GPIO30 and SUSPWRDNACK. Intel® Xeon® Processor D-1500 Product Family-based platform doesn't support Deep Sleep Power state.
PCH_PWROK	I	None	VCCSUS3_3	**Power OK:** When asserted, PCH_PWROK is an indication to the integrated PCH that all of its core power rails have been stable for at least 5 ms. PCH_PWROK can be driven asynchronously. When PCH_PWROK is negated, the integrated PCH asserts PLTRST_N. ***Notes:*** 1. It is required that the power rails associated with PCI/PCIe (typically the 3.3 V, 5 V, and 12 V core well rails) have been valid for 99 ms prior to PCH_PWROK assertion in order to comply with the 100 ms PCI 2.3/PCIe* 2.0 specification on PLTRST_N de-assertion. 2. PWROK must not glitch, even if RSMRST_N is low.
PWRBTN_N	I	15K-40K PU	VCCSUS3_3	**Power Button:** The Power Button will cause SMI# or SCI to indicate a system request to go to a sleep state. If the system is already in a sleep state, this signal will cause a wake event. If PWRBTN# is pressed for more than 4 seconds, this will cause an unconditional transition (power button override) to the S5 state. Override will occur even if the system is in the S1–S4 states. This signal has an internal pull-up resistor and has an internal 16 ms de-bounce on the input.
RSMRST_N	I	None	RTC	**Resume Well Reset:** This signal resets the resume power plane logic of the PCH. This signal must be asserted for at least 10 ms after the suspend power wells are valid. When de-asserted, this signal is an indication that the suspend power wells are stable.
PLTRST_PROC_N	O	None	VCCIO	**Platform Reset Processor:** A 1.0V copy of PLTRST_N pin. This signal is the main host platform reset and should directly connect to the integrated processor pin RESET_CPU_N. No on-board logic is required to level shift the voltage of this signal.

Table 2-17. Power Management Signals (Sheet 3 of 3)

Signal Name	I/O Type	Internal Resistor PU/PD	Power Rail	Description
PLTRST_N	O	None	VCCSUS3_3	**Platform Reset:** The integrated PCH asserts PLTRST_N to reset devices on the platform (such as SIO, LAN, integrated processor, and so on). The integrated PCH asserts PLTRST_N during power-up and when S/W initiates a hard reset sequence through the Reset Control register (I/O port CF9h). The integrated PCH drives PLTRST_N active a minimum of 1 ms when initiated through the Reset Control register (I/O port CF9h). ***Note:*** PLTRST_N is in the VccSUS3_3 well.
LAN_PHY_PWR_CTRL _GPIO12	O	None	VCCSUS3_3	**LAN PHY Power Control:** LAN_PHY_PWR_CTRL should be connected to LAN_DISABLE_N on the PHY. Integrated PCH will drive LAN_PHY_PWR_CTRL low to put the PHY into a low power state when functionality is not needed. ***Notes:*** 1. LAN_PHY_PWR_CTRL can only be driven low if SLP_LAN_N is de-asserted. 2. Signal can instead be used as GPIO12.
RI_N	I	None	VCCSUS3_3	**Ring Indicate:** This signal is an input from a modem. It can be enabled as a wake event, and this is preserved across power failures.
SUSCLK_GPIO62	I/O	15K-40K PU	VCCSUS3_3	**Suspend Clock:** This clock is an output of the RTC generator circuit to use by other chips for refresh clock. This pin may also be used as GPIO62.
WAKE_N	I/O	15K-40K PD	VCCSUS3_3	**PCI Express* Wake Event in Sx:** This signal is in SUS and behaves as an input pin in Sx states. Sideband wake signal on PCI Express asserted by components requesting wake up. PCIe OBFF on this pin has been de-featured and is not supported.
LAN_PWRGOOD	I	None	VCCIOIN	Power good indication that all power rails to SoC South Complex are good.
WAKELAN_N	O	None	VCCIOIN	This is an indication from SoC South Complex (SC) to the integrated PCH that SC receives the magic packet from 10 GbE interface.
TD_IREF	I	None	N/A	This pin requires an 8.2K 1% pull-down resistor tied to ground. It provides a reference current for a thermal diode in the PCH logic.

2.17 Interrupt Signals

Table 2-18. Interrupt Signals

Signal Name	I/O Type	Internal Resistor PU/PD	Power Rail	Description
SERIRQ	I/OD	None	VCC3_3	**Serial Interrupt Request:** This pin implements the serial interrupt protocol.
PIRQ[D:A]_N	I/OD	None	VCC3_3	**PCI Interrupt Requests:** In non-APIC mode, the PIRQx_N signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14, or 15. Each PIRQx_N line has a separate Route Control register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQA_N is connected to IRQ16, PIRQB_N to IRQ17, PIRQC_N to IRQ18, and PIRQD# to IRQ19. This frees the legacy interrupts.
PIRQ[H:E]_N/GPIO[5:2]	I/OD	None	VCC3_3	**PCI Interrupt Requests:** In non-APIC mode, the PIRQx# signals can be routed to interrupts 3, 4, 5, 6, 7, 9, 10, 11, 12, 14, or 15. Each PIRQx_N line has a separate Route Control register. In APIC mode, these signals are connected to the internal I/O APIC in the following fashion: PIRQE_N is connected to IRQ20, PIRQF_N to IRQ21, PIRQG_N to IRQ22, and PIRQH_N to IRQ23. This frees the legacy interrupts. If not needed for interrupts, these signals can be used as GPIO.

2.18 GPIO Signals

The following table summarizes the GPIOs in the PCH. The control for the GPIO signals is handled through an independent 128-byte I/O space. The base offset for this space is selected by the GPIO_BAR register in D31:F0 configuration space.

Highlights of GPIO features:

a. Only GPIO[31:1] are blink-capable.

b. When the default of a multiplexed GPIO is Native but the desired functionality is GPIO, care should be taken to ensure the signal is stable until it is initialized to GPIO functionality.

c. Glitch-less Output means the signal is ensured to be stable (no glitch) during power on and when switching mode of operation from Native to GPIO or GPIO to Native. Glitch-less Input means the signal has built-in de-glitch protection that gates the input signal until power has become stable (the input is ignored during this time).

d. The following GPIOs are capable of generating SMI_N, SCI, or NMI: GPIO[60, 57, 43, 27, 22, 21, 19, 17, 15, 14, 12:0].

e. GPIO_USE_SEL[31:0], GPIO_USE_SEL2[63:32] and GPIO_USE_SEL3[75:64] select whether the pin is selected to function as GPIO (GPIO_USE_SEL[x] = 1) or Native (GPIO_USE_SEL[x] = 0). However, the PCH Soft Straps (SPI Flash) take precedence if there is a mismatch with GPIO_USE_SEL.

f. GP_IO_SEL[31:0], GP_IO_SEL[63:32] and GP_IO_SEL[75:64] select whether the pin is an output (GP_IO_SEL[x] = 0) or an input (GP_IO_SEL[x] = 1). The value written to or reported in this register is invalid when the pin is programmed to Native function.

g. If the corresponding GPIO has been set as an input, and GPI_ROUT has been programmed for NMI functionality, the GPI_NMI_EN[15:0] is used to allow active-high or active-low NMI events (depending on the polarity selected by GPI_INV[31:0]).

h. All the GP_RST_SEL registers are only resettable by RSMRST_N. GPIO Configuration registers within the Core Well are reset whenever PWROK is de-asserted.

i. GPIO Configuration registers within the Suspend Well are reset when RSMRST_N is asserted, CF9h reset (06h or 0Eh), or SYS_RESET_N is asserted. However, CF9h reset and SYS_RESET_N events can be masked from resetting the Suspend well GPIO by programming appropriate GPIO Reset Select (GPIO_RST_SEL) registers.

j. GPIO24 is an exception to the other GPIO Signals in the Suspend Well and is not reset by CF9h reset (06h or 0Eh).

Table 2-19. General Purpose I/O Signals (Sheet 1 of 4)

Name	Power Well	Default (Note 2)	GPI Event	Glitch-less (Note 6)		Description
				Input	Output	
GPIO0	Core	GPI	Yes	No	No	Multiplexed with BMBUSY_N.
GPIO1	Core	GPI	Yes	Yes	No	Multiplexed with TACH1.
GPIO2[8]	Core	GPI	Yes	No	No	Multiplexed PIRQE_N.
GPIO3[8]	Core	GPI	Yes	No	No	Multiplexed PIRQF_N.
GPIO4[8]	Core	GPI	Yes	No	No	Multiplexed PIRQG_N.
GPIO5[8]	Core	GPI	Yes	No	No	Multiplexed PIRQH_N.

Table 2-19. General Purpose I/O Signals (Sheet 2 of 4)

Name	Power Well	Default (Note 2)	GPI Event	Glitch-less (Note 6)		Description
				Input	Output	
GPIO6	Core	GPI	Yes	Yes	No	Multiplexed with TACH2.
GPIO7	Core	GPI	Yes	Yes	No	Multiplexed with TACH3.
GPIO8	Sus	GPO	Yes	No	No	Unmultiplexed
GPIO9	Sus	Native	Yes	No	No	Multiplexed with OC5#. When configured as GPIO, default direction is Input (GPI).
GPIO10	Sus	Native	Yes	No	No	Multiplexed with OC6#. When configured as GPIO, default direction is Input (GPI).
GPIO11	Sus	Native	Yes	Yes	No	Multiplexed with SMBALERT#. When configured as GPIO, default direction is Input (GPI).
GPIO12[10]	SUS	Native	Yes	No	No	Multiplexed with LAN_PHY_PWR_CTRL. GPIO / Native functionality is controlled using soft strap. When configured as GPIO, default direction is Output (GPO).
GPIO14	Sus	Native	Yes	No	No	Multiplexed with OC7#. When configured as GPIO, default direction is Input (GPI).
GPIO15	SUS	GPO	Yes	No	Yes	Unmultiplexed
GPIO16[10]	Core	GPI	No	No	No	Multiplexed with SATA4GP.
GPIO17	Core	GPI	Yes	Yes	No	Multiplexed with TACH0.
GPIO18	Core	Native	No	No	No	Multiplexed with PCIECLKRQ1_N. External pull up resistor required for Native function. When configured as GPIO, default direction is Output (GPO).
GPIO19[5]	Core	GPI	Yes	No	No	Multiplexed with SATA1GP.
GPIO20[14]	Core	Native	No	No	No	When configured as GPIO, default direction is Output (GPO). Also available as SMI_N.
GPIO21	Core	GPI	Yes	No	No	Multiplexed with SATA0GP.
GPIO22	Core	GPI	Yes	No	No	Multiplexed with SCLOCK.
GPIO23	Core	Native	No	No	No	Multiplexed with LDRQ1_N.
GPIO24[1]	SUS	GPO	No	No	Yes	Unmultiplexed
GPIO25	SUS	Native	No	No	No	Unmultiplexed (Native function not supported but pin defaults to native mode and be configured for GPIO.)
GPIO26	SUS	Native	No	No	No	Unmultiplexed (Native function not supported but pin defaults to native mode and be configured for GPIO.)
GPIO27	SUS	GPI	No	No	No	Unmultiplexed
GPIO28	SUS	GPO	No	No	Yes	Unmultiplexed
GPIO29[10,13]	SUS	Native	No	No	Yes	Multiplexed with SLP_WLAN_N. GPIO/Native functionality is controlled using soft strap. When configured as GPIO, default direction is output (GPO).
GPIO30	Sus	Native	No	No	Yes	Multiplexed with SUSPWRDNACK, SUSWARN_N. SUSPWRDNACK mode is the default mode of operation. When configured as GPIO, default direction is Input (GPI).
GPIO31[3]	SUS	GPI	No	No	Yes	***Notes:*** 1. Toggling this pin at a frequency higher than 10 Hz is not supported. 2. GPIO_USE_SEL[31] is internally hardwired to a 1b, which means GPIO mode is permanently selected and cannot be changed.
GPIO32[4]	Core	GPO	No	No	No	Unmultiplexed

Table 2-19. General Purpose I/O Signals (Sheet 3 of 4)

Name	Power Well	Default (Note 2)	GPI Event	Glitch-less (Note 6)		Description
				Input	Output	
GPIO33[5]	Core	GPO	No	No	No	Unmultiplexed
GPIO35	Core	GPO	No	No	Yes	Also available as NMI_N.
GPIO36[5]	Core	GPI	No	No	No	Multiplexed with SATA2GP.
GPIO37[5]	Core	GPI	No	No	No	Multiplexed with SATA3GP.
GPIO38	Core	GPI	No	No	No	Multiplexed with SLOAD.
GPIO39	Core	GPI	No	No	No	Multiplexed with SDATAOUT0.
GPIO40	Sus	Native	No	No	No	Multiplexed with OC1#. When configured as GPIO, default direction is Input (GPI).
GPIO41	Sus	Native	No	No	No	Multiplexed with OC2#. When configured as GPIO, default direction is Input (GPI).
GPIO42	Sus	Native	No	No	No	Multiplexed with OC3#. When configured as GPIO, default direction is Input (GPI).
GPIO43	Sus	Native	Yes	No	No	Multiplexed with OC4#. When configured as GPIO, default direction is Input (GPI).
GPIO44	Sus	Native	No	No	No	Unmultiplexed (native function not supported but pin defaults to native mode and be configured for GPIO.)
GPIO45	Sus	Native	No	No	No	Unmultiplexed (native function not supported but pin defaults to native mode and be configured for GPIO.)
GPIO46	Sus	Native	No	No	No	Unmultiplexed (native function not supported but pin defaults to native mode and be configured for GPIO.)
GPIO48	Core	GPI	No	No	No	Multiplexed with SDATAOUT1.
GPIO49[10]	Core	GPI	No	Yes	No	Multiplexed with SATA5GP.
GPIO50	Core	GPI	No	No	No	Unmultiplexed
GPIO51[5]	Core	GPO	No	No	No	Unmultiplexed
GPIO52	Core	GPI	No	No	No	Unmultiplexed
GPIO53[5]	Core	GPO	No	No	No	Unmultiplexed
GPIO54	Core	GPI	No	No	No	Unmultiplexed
GPIO55[5]	Core	GPO	No	No	No	Unmultiplexed
GPIO57[9]	Sus	GPI	Yes	No	Yes	Unmultiplexed. Can be re-purposed for NFC interface input.
GPIO58	Sus	Native	No	Yes	No	Multiplexed with SML1CLK. When configured as GPIO, default direction is Input (GPI).
GPIO59	Sus	Native	No	No	No	Multiplexed with OC0#. When configured as GPIO, default direction is Input (GPI).
GPIO60	Sus	Native	Yes	Yes	No	Multiplexed with SML0ALERT#. When configured as GPIO, default direction is Input (GPI).
GPIO61	Sus	Native	No	No	Yes	Multiplexed with SUS_STAT_N. When configured as GPIO, default direction is Output (GPO).
GPIO62[5,11]	Sus	Native	No	No	No	Multiplexed with SUSCLK. When configured as GPIO, default direction is Output (GPO).

Table 2-19. General Purpose I/O Signals (Sheet 4 of 4)

Name	Power Well	Default (Note 2)	GPI Event	Glitch-less (Note 6)		Description
				Input	Output	
GPIO65	Core	Native	No	No	No	Multiplexed with CLKOUTFLEX1. When configured as GPIO, default direction is Output (GPO).
GPIO67	Core	Native	No	No	No	Multiplexed with CLKOUTFLEX3. When configured as GPIO, default direction is Output (GPO).
GPIO68	Core	GPI	No	Yes	No	Multiplexed with TACH4.
GPIO69	Core	GPI	No	Yes	No	Multiplexed with TACH5.
GPIO70[10]	Core	Native	No	Yes	No	Multiplexed with TACH6.
GPIO71[10]	Core	Native	No	Yes	No	Multiplexed with TACH7.
GPIO72[4]	SUS	Native	No	No	No	Unmultiplexed
GPIO74[9,11,15]	Sus	Native	No	Yes	No	Multiplexed with SML1ALERT_N/TEMP_ALERT_N. When configured as GPIO, default direction is Input (GPI). Can be re-purposed for NFC interface input.
GPIO75	Sus	Native	No	Yes	No	Multiplexed with SML1DATA. When configured as GPIO, default direction is Input (GPI).

Notes:
1. GPIO24 register bits are not cleared by CF9h reset by default, it is programmable through GP_RST_SEL[24].
2. Internal pull up or pull down may be present when Native functionality is selected.
3. Internal pull down resistor may be enabled in Deep Sx mode based on DSX_CFG configuration bit, as follows: '1' (pin will be driven by platform in Deep Sx) -> Z; - '0' (pin will NOT be driven by platform in Deep Sx) -> Internal pull-down. Refer to the DSX_CFG register (RCBA+3334h) for more details.
4. For pins that are available as GPIO-only: if the power-on default is Native, the BIOS is still required to configure the pin as GPIO by writing to the pin's GPIO_USE_SEL register, even though the pin is only available as GPIO.
5. A functional strap also exists on this pin.
6. Glitch-less inputs are guaranteed, by circuit design, to de-glitch the input. Glitch-less outputs are guaranteed, by circuit design, to not generate any glitches on the output during power-on.
7. The GPIO pins which are capable of generating NMI message when it is configured as input, its GPI_ROUT register is configured NMI functionality and its corresponding GPI NMI Enable (GNE) bit is set. The NMI event is positive edge trigger based on the signal and after GPI Inversion logic.
8. When GPIO[5:2] are configured as output GPIOs, they behave in an open drain manner.
9. GPIO 74 or GPIO 57 can be used for NFC on a platform. The NFC option can be set through FITC in Intel ME configuration settings.
10. For GPIOs where GPIO vs Native Mode is configured using SPI Soft Strap, the corresponding GPIO_USE_SEL bits for these GPIOs have no effect. The GPIO_USE_SEL bits for these GPIOs may change to reflect the Soft-Strap configuration even though GPIO Lockdown Enable (GLE) bit is set.
11. GPIO62 defaults as Native SUSCLK. If this pin is to be configured as GPIO, it is required that the board ensure that the 32.768 kHz toggle rate does not affect the receiving logic of the pin until it is set as GPIO.
12. When switching from GPIO at logic 1 to the native functionality, the pin must not glitch low.
13. A soft strap (PMC_SOFT_STRAP_2 register[7] GP23MGPIO3_SLPWLAN_SEL) to enable switching between SLP_WLAN_N (default) or GP29/MPGIO3. By default the strap is 0b, which enables the SLP_WLAN_N pin function when SUS well is up. When soft strap is loaded and value is 1b, the pin returns to its regular GPIO or MGPIO mode while SLP_WLAN_N function no longer exists. Also take into account of Note 11.
14. When strapped as SMI_N, the pin is automatically configured as open drain. The SMI_N function is not the same as the SMI_N events that the GPIOs can be configured to generate, as described in GPI_ROUT and ALT_GPI_SMI_EN.
15. The choice of which native mode, SML1ALERT_N or TEMP_ALERT_N, is determined by a soft strap.

2.19 MGPIO Signals

The following signals can be optionally used by the Intel® Management Engine (Intel® ME) supported applications and appropriately configured by Intel ME Firmware. When configured and used as a manageability function, the associated host GPIO functionality is no longer available. If the manageability function is not used in a platform, the signal can be used as a host General Purpose I/O or a native function.

The manageability signals are referred to as Intel ME GPIO pins (MGPIO pins), which are GPIO pins that can be controlled through Intel ME FW.

Table 2-20. MGPIO Conversion Table

MGPIO	GPIO	Well	Default Usage
1	30	SUS	SUSWARN_N or SUSPWRDNACK
2	31	SUS	GPIO
4	60	SUS	SML0ALERT_N
5	57	SUS	GPIO (assumes GPIO57 is not setup for NFC)
6	27	DSW	Intel ME Wake Input
8	74	SUS	SML1ALERT_N/TEMP_ALERT_N
9	16	Core	SATA4GP
10	49	Core	SATA5GP
11	58	SUS	SML1CLK
12	75	SUS	SML1DATA

2.20 System Management Interface Signals

Table 2-21. SMBus and SMLink Signals

Signal Name	I/O Type	Internal Resistor PU/PD	Power Rail	Description
INTRUDER_N	I	None	RTC	**Intruder Detect:** This signal can be set to disable the system if box detected open. This signal status is readable, so it can be used like a GPI if the Intruder Detection is not needed.
SMBALERT_N_GPIO11	OD	None	VCCSUS3_3	**SMBus Alert:** This signal is used to wake the system or generate SMI_N. This signal may be used as GPIO11.
SMBCLK	I/OD	None	VCCSUS3_3	**SMBus Clock:** External pull-up resistor is required.
SMBDATA	I/OD	None	VCCSUS3_3	**SMBus Data:** External pull-up resistor is required.
SML0ALERT_N_GPIO60_MGPIO4	OD	None	VCCSUS3_3	**SMLink Alert 0:** Output of the integrated LAN controller to external PHY. External pull-up resistor is required. This signal can instead be used as GPIO60. Also, alert for the ME SMBus controller to optional Embedded Controller or BMC.
SML0CLK	I/OD	None	VCCSUS3_3	**System Management Link 0 Clock:** SMBus link to external PHY. SMBus link to optional Embedded Controller or BMC.External pull-up is required.
SML0DATA	I/OD	None	VCCSUS3_3	**System Management Link 0 Data:** SMBus link to external PHY. SMBus link to optional Embedded Controller or BMC.External pull-up is required.
SML1ALERT_N_PCHHOT_N_GPIO74	OD	None	VCCSUS3_3	**SMLink Alert 1:** A soft-strap determines the native function SML1ALERT_N or TEMP_ALERT_N usage. When soft-strap is 0, function is SML1ALERT_N, when soft-strap is 1, function is TEMP_ALERT_N. This pin can also be set to function as GPIO74. External pull-up resistor is required on this pin.
SML1CLK_GPIO58_MGPIO11	I/OD	None	VCCSUS3_3	**System Management Link 1 Clock:** External pull-up resistor is required. This signal can instead be used as GPIO58.
SML1DATA_GPIO75_MGPIO12	I/OD	None	VCCSUS3_3	**System Management Link 1 Data:** External pull-up resistor is required. This signal can instead be used as GPIO75.

2.21 SPI Signals

Table 2-22. SPI Signals

Signal Name	I/O Type	Internal Resistor PU/PD	Power Rail	Description
SPI_CLK	O	15K-40K PU	VCCSUS3_3	**SPI Clock**: SPI clock signal, during idle the bus owner will drive the clock signal low. Supported frequencies are 20 MHz, 33 MHz and 50 MHz.
SPI_CS0_N	O	15K-40K PU	VCCSUS3_3	**SPI Chip Select 0**: Used to select the primary SPI Flash device. ***Note:*** This signal cannot be used for any other type of device than SPI Flash.
SPI_CS1_N	O	15K-40K PU	VCCSUS3_3	**SPI Chip Select 1**: Used to select an optional secondary SPI Flash device. ***Note:*** SPI_CS1_N cannot be used for any other type of device than SPI Flash.
SPI_CS2_N	O	15K-40K PU	VCCSUS3_3	**SPI Chip Select 2:** Used to select the TPM device if it is connected to the SPI interface, it cannot be used for any other type of device than TPM. ***Note:*** TPM can be configured through soft straps to operate over LPC or SPI, but no more than 1 TPM is allowed in the system.
SPI_MOSI_IO0	I/O	15K-40K PU	VCCSUS3_3	**SPI Master OUT Slave IN**: Defaults as a data output pin for PCH in Dual Output Fast Read mode. Can be configured with a soft strap as a bidirectional signal (SPI_IO0) to support the new Dual I/O Fast Read, Quad IO Fast Read and Quad Output Fast Read modes.
SPI_MISO_IO1	I/O	15K-40K PU	VCCSUS3_3	**SPI Master IN Slave OUT**: Defaults as a data input pin for PCH in Dual Output Fast Read mode. Can be configured with a soft strap as a bidirectional signal (SPI_IO1) to support the new Dual I/O Fast Read, Quad IO Fast Read and Quad Output Fast Read modes.
SPI_IO2	I/O	15K-40K PU	VCCSUS3_3	**SPI Data I/O:** A bidirectional signal used to support the new Dual I/O Fast Read, Quad IO Fast Read and Quad Output Fast Read modes. This signal is not used in Dual Output Fast Read mode.
SPI_IO3	I/O	15K-40K PU	VCCSUS3_3	**SPI Data I/O:** A bidirectional signal used to support the new Dual I/O Fast Read, Quad IO Fast Read and Quad Output Fast Read modes. This signal is not used in Dual Output Fast Read mode.

2.22 Integrated PCH Functional Straps

The SoC integrated PCH implements hardware functional straps that are used to configure specific functions very early in the boot process, before BIOS or software intervention. Some are sampled at the rising edge of PCH_PWROK, while others at the rising edge of RSMRST_N to select configurations (except as noted), and then revert later to their normal usage. When descriptor mode is enabled, the PCH will read Soft Strap data out of the SPI device prior to the de-assertion of reset to both the Intel Management Engine and the host system. In some cases, the soft strap data may override the hardware functional straps.

Table 2-23. SoC Integrated PCH Functional Strap Definitions (Sheet 1 of 3)

<table>
<tr><th>Signal</th><th>Usage</th><th>When Sampled</th><th>Comment</th></tr>
<tr><td>SATA1GP / GPIO19</td><td>Boot BIOS Strap bit 0
(BBS0)</td><td>Rising edge of PCH_PWROK</td><td>This signal has a weak internal pull-up.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 1 strap.
<table>
<tr><th>Bit11</th><th>Bit 10</th><th>Boot BIOS Destination</th></tr>
<tr><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>SPI (default)</td></tr>
<tr><td>0</td><td>0</td><td>LPC</td></tr>
</table>
Notes:
1. The internal pull-up is disabled after PLTRST_N de-asserts.
2. If option 00 (LPC) is selected, the BIOS may still be placed on LPC, but the platform is required to have SPI FLASH connected directly to the PCH SPI bus with a valid descriptor in order to boot.
3. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel ME or integrated GbE LAN.
4. This signal is in the core well.</td></tr>
<tr><td>GPIO51</td><td>Boot BIOS Strap bit 1
(BBS1)</td><td>Rising edge of PCH_PWROK</td><td>This signal has a weak internal pull-up.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Config Registers: Offset 3410h:Bit 11). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.
<table>
<tr><th>Bit11</th><th>Bit 10</th><th>Boot BIOS Destination</th></tr>
<tr><td>0</td><td>1</td><td>Reserved</td></tr>
<tr><td>1</td><td>0</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>SPI (default)</td></tr>
<tr><td>0</td><td>0</td><td>LPC</td></tr>
</table>
Notes:
1. The internal pull-up is disabled after PLTRST_N de-asserts.
2. If option 00 (LPC) is selected, the BIOS may still be placed on LPC, but the platform is required to have SPI Flash connected directly to the PCH's SPI bus with a valid descriptor in order to boot.
3. Boot BIOS Destination Select to LPC/PCI by functional strap or using Boot BIOS Destination Bit will not affect SPI accesses initiated by Intel ME or integrated GbE LAN.
4. This signal is in the core well.</td></tr>
<tr><td>SATA3GP / GPIO37</td><td>TLS Confidentiality</td><td>Rising edge of PCH_PWROK</td><td>This signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).
Notes:
1. The internal pull-down is disabled after PLTRST_N de-asserts.
2. This signal is in the core well.</td></tr>
</table>

Table 2-23. SoC Integrated PCH Functional Strap Definitions (Sheet 2 of 3)

Signal	Usage	When Sampled	Comment
MFG_MODE_STRAP	Flash Descriptor Security Override	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = **Enable** security measures defined in the Flash Descriptor. 1 = **Disable** Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. ***Notes:*** 1. The internal pull-down is disabled after PLTRST_N de-asserts. 2. Asserting MFG_MODE_STRAP high on the rising edge of PWROK will also halt Intel ME after SoC bring up and disable runtime Intel ME features. This is a debug mode and must not be asserted after manufacturing/debug. 3. This signal is in the suspend well.
INTVRMEN	Integrated VRM Enable	Always	This signal does not have an internal resistor; an **external** resistor is **required**. 0 = DCPSUS1, DCPSUS2 and DCPSUS3 are powered from an external power source (should be connected to an external VRM). It should not pull the strap low. 1 = Integrated VRMs enabled. DCPSUS1, DCPSUS2 and DCPSUS3 can be left as No Connect. ***Notes:*** 1. This signal is always sampled. 2. This signal is in the RTC well.
GPIO62 / SUSCLK	PLL On-Die Voltage Regulator Enable	Rising edge of RSMRST_N	This signal has a weak internal pull-up. 0 = **Disable** PLL On-Die voltage regulator. 1 = **Enable** PLL On-Die voltage regulator. ***Notes:*** 1. The internal pull-up is disabled after RSMRST_N de-asserts. 2. This signal is in the suspend well.
DSWODVREN	DeepSx Well On-Die Voltage Regulator Enable	Always	This signal does not have an internal resistor; an **external** resistor is **required**. 0 = **Disable** Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This mode is only supported for testing environments. 1 = **Enable** DSW 3.3 V-to-1.05 V Integrated DeepSx Well (DSW) On-Die Voltage Regulator. This must always be pulled high on production boards. ***Notes:*** 1. This signal is always sampled. 2. This signal is in the RTC well.
SPKR	No Reboot	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = **Disable** "No Reboot" mode. 1 = **Enable** "No Reboot" mode (integrated PCH will disable the TCO Timer system reboot feature). This function is useful when running Intel® In-Target Probe (Intel® ITP)/XDP. ***Notes:*** 1. The internal pull-down is disabled after PLTRST_N de-asserts. 2. The status of this strap is readable using the NO REBOOT bit (Chipset Config Registers: RCBA + Offset 3410h:Bit 5). 3. This signal is in the core well.
SATA2GP/GPIO36	SoC RX Termination	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. This signal only takes effect if SoC is configured in AC coupled mode. 0 = SoC RX is terminated to VSS. Intel® Xeon® Processor D-1500 NS Product Family-based platform only supports SoC Rx terminated to VSS. 1 = SoC RX is terminated to VCC/2. ***Notes:*** 1. The internal pull-down is disabled after PLTRST_N de-asserts. 2. If SoC is operating in DC-coupled mode, then SoC RX is terminated to VSS and the value of this strap is ignored and does not take effect. 3. This signal is in the core well

Table 2-23. SoC Integrated PCH Functional Strap Definitions (Sheet 3 of 3)

Signal	Usage	When Sampled	Comment
GPIO33	SoC Tx Termination	Rising edge of PCH_PWROK	This signal has a weak internal pull-down. 0 = SoC TX is terminated to VSS. Intel® Xeon® Processor D-1500 NS Product Family-based platform only supports SoC Tx terminated to VSS 1 = SoC TX is terminated to VCC/2. ***Notes:*** 1. The internal pull-down is disabled after PLTRST_N de-asserts. 2. This signal is in the core well.
GPIO53	SoC AC-Coupling or DC-Coupling Mode	Rising edge of PCH_PWROK	This signal has a weak internal pull-up. 0 = SoC is in AC-coupling mode. Intel® Xeon® Processor D-1500 Product Family-based platform only supports AC-coupling mode. 1 = SoC is in DC-coupling mode. ***Notes:*** 1. The internal pull-up is disabled after PLTRST_N de-asserts. 2. This signal is in the core well.
GPIO55	Top Swap Override	Rising edge of PCH_PWROK	The signal has a weak internal pull-up. 0 = **Enable** "Top Swap" mode. This inverts an address on access to SPI flash, so the processor fetches the alternate boot block instead of the original boot-block. PCH will invert A16 (default) for cycles going to the upper two 64 KB blocks in the SPI flash or the appropriate address lines (A16, A17, A18, A19, or A20) as selected in Top-Swap Block size soft strap (handled through FITc. 1 = **Disable** "Top Swap" mode. ***Notes:*** 1. The internal pull-up is disabled after PLTRST_N de-asserts. 2. Software will not be able to clear the Top Swap mode bit until the system is rebooted. 3. The status of this strap is readable using the Top Swap bit (Chipset Config Registers: RCBA + Offset 3414h:Bit 0). 4. This signal is in the core well.
GPIO72	Boot Inhibit	Rising edge of RSMRST_N	Need 1K-10K pull up to VCCSUS3_3. Signal must be sampled high at rising edge of RSMRST_N.
ME_RCVR_N	Forces ME into Recovery Mode.	This signal is checked whenever the ME resets. It should not be shared with other functions if configured for ME Recovery.	This signal can be configured via the FITc tool to be on MGPIO[8:1] or disabled. The default is pin GPIO57_MGPIO5. This signal does not have an internal pull-up or pull-down. It should have an external 10K pull-up to VCCSUS3_3 with a jumper option to a 1K pull down resistor. 0=Recovery mode 1=Normal operating mode for Intel ME. The default for production systems must be normal operating mode.

2.23 SoC Integrated Processor Straps

Table 2-24. SoC Integrated Processor Straps Definitions (Sheet 1 of 3)

Signal	Usage	When Sampled	Description
BIST_ENABLE	BIST Enable Strap	RESET_CPU_N De-assertion	5K-15K ohm internal pull up to VCCIOIN power rail. Build-in Self Test (BIST) enable strap: 0 = BIST Disable 1 = BIST Enable
BMCINIT	BMC Initialization Strap	PWRGOOD_CPU assertion	5K-15K ohm internal pull down to GND. Integrated Service Processor Boot Mode Selection: 0 = Integrated Service Processor Boot Mode Disabled 1 = Integrated Service Processor Boot Mode Enabled

Table 2-24. SoC Integrated Processor Straps Definitions (Sheet 2 of 3)

Signal	Usage	When Sampled	Description
TXT_PLTEN	Platform Enable Strap	PWRGOOD_CPU assertion	5K-15K ohm internal pull up to VCCIOIN power rail. 0 = The platform is not Intel enabled. 1 = Default. The platform is Intel enabled.
TXT_AGENT	Agent Strap	PWRGOOD_CPU assertion	5K-15K ohm internal pull down to GND. 0 = Default. The SoC is not the Intel Agent. 1 = The SoC is the Intel Agent.
SAFE_MODE_BOOT	Safe Mode Boot Strap	PWRGOOD_CPU assertion	5K-15K ohm internal pull down to GND. 0 = Safe Mode Boot Disabled 1 = Safe Mode Boot Enabled
DEBUG_EN_N	Force Debug Enable Strap	PWRGOOD_CPU assertion	5K-15K ohm internal pull up to VCCIOIN power rail. 0 = Debug Mode 1 = Normal Mode
DDR3_4_STRAP	DDR3 or DDR4 Selection Strap	Rising edge of LAN_PWRGOOD	It has internal pull up. Select between DDR4 and DDR3. 0 = DDR3, it requires <1K ohm pull down in order to out drive the internal pull up. 1= DDR4 (Default)
LAN1_MDC0_LED0_1_PECI_ID0; LAN_NCSI_TRI_EN_PECI_ID1; THROTTLE_PECI_ID2	PECI ID[2:0]	Rising edge of LAN_PWRGOOD	In micro-server design space, there will be multiple sockets that share a PECI bus. However these sockets are effectively independent agents. The PECI IDs are used as straps to identify which socket is which in order for PECI bus to work. For example: Node 0 - 3'b000, Node 1- 3'b001, Node 2- 3'b010... and so on. Recommend 5.1 kohm pull up to VCCIOIN or 5.1 kohm pull down to GND. There is no internal pull up or pull down.
LAN0_MDIO_DIR_CTL_0; LAN0_MDIO_DIR_CTL_1	LAN_SEL[1:0]	Rising edge of LAN_PWRGOOD	00 = Both LAN ports are disabled. ***Note:*** In this mode manageability is not functional and must not be enabled in NVM control word 1. 01 = LAN_KR_{TX/RX}1 is disabled. Port 0 is enabled. 10 = Reserved 11 = LAN_KR_{TX/RX}{0/1} are enabled. Recommend 5.1 kohm pull up to VCCIOIN or 5.1 kohm pull down to GND. There is no internal pull up or pull down.
LAN1_MDIO_DIR_CTL_0; LAN1_MDIO_DIR_CTL_1	LAN1_SEL[1:0]	Rising edge of LAN_PWRGOOD	00 = Both LAN1 ports are disabled. Note: In this mode manageability is not functional and must not be enabled in NVM control word 1. 01 = LAN1_KR_{TX/RX}1 is disabled. Port 0 is enabled. 10 = Reserved 11 = LAN1_KR_{TX/RX}{0/1} are enabled. Recommend 5.1 kohm pull up to VCCIOIN or 5.1 kohm pull down to GND. There is no internal pull up or pull down.
LAN1_FLASH_DI	Reserved	Rising edge of LAN_PWRGOOD	This pin should have a 5.1 kohm pull down to GND.
LAN1_MDC1_LED1_1	Reserved	Rising edge of LAN_PWRGOOD	This pin should have a 1.0 kohm pull down to GND. There is no internal pull up or pull down.
SERIRQ_DIR	Reserved	Rising edge of LAN_PWRGOOD	Recommend 5.1 kohm pull up to VCCIOIN. There is no internal pull up or pull down.
UART_TXD[0]	Reserved	Rising edge of LAN_PWRGOOD	Recommend 5.1 kohm pull down to GND. There is no internal pull up or pull down.

Table 2-24. SoC Integrated Processor Straps Definitions (Sheet 3 of 3)

Signal	Usage	When Sampled	Description
UART_TXD[1]	NVM Security Attributes Control	Rising edge of LAN_PWRGOOD	Controls the security attributes on the NVM - for pre-production usage only. 0 = Disable NVM Security (Default) 1 = Security Enabled Recommend 5.1 kohm pull down to GND. There is weak internal pull up.
LAN_NCSI_RXD0	Manageability Traffic Control for LAN1	Rising edge of LAN_PWRGOOD	Enable/Disable manageability traffic: 0 = LAN1 available in S5 for WoL (Default) 1 = Reserved. Mandatory 5.1 kohm pull down to GND. There is no internal pull up or pull down.
LAN_NCSI_RXD1	Manageability Traffic Control	Rising edge of LAN_PWRGOOD	Enable/Disable manageability traffic: 0 = LAN available in S5 for WoL (Default) 1 = Reserved. Mandatory 5.1 kohm pull down to GND. There is no internal pull up or pull down.
LAN_NCSI_ARB_OUT	SVID VR Configuration	Rising edge of LAN_PWRGOOD	Selects SVID VR Operating Mode Must have 10K pull-up to VCCGBE supply. 1 - P1V05_PCH, VCCGBE, VCCIOIN are combined into one SVID controlled supply. 0 - Reserved.

2.24 Reserved/Test Signals

Reserved and NCTF/TP can generally be left unconnected except for the following signals which require special termination. A range is specified where the exact value is not critical.

Table 2-25. Reserved Signals

Signal Name	Pin	Connection
RSVD84	AA66	49.9 Ω 1% to GND
RSVD93	A73	1k - 5.1 kΩ to GND
RSVD94	A74	1k - 5.1 kΩ to GND
RSVD00	BL14	1k - 10kΩ to VCC3_3
RSVD18	E55	1k - 5.1 kΩ to GND
RSVD16	F54	1k - 5.1 kΩ to GND
RSVD17	J54	1k - 5.1 kΩ to GND
NCTF/TP	BA27	1k - 10kΩ to VCC3_3
NCTF/TP	P11	8.2k to GND

2.25 Power Groups

Table 2-26. Power Signals (Sheet 1 of 2)

Signal Name	Description
VCCD	Power supply for the SoC memory interface.
VCCIN	Input to the Integrated Voltage Regulator (IVR) for the SoC. It is provided by a VRM/EVRD 12.5 compliant regulator. The output voltage of this supply is selected by the SoC, using the serial voltage ID (SVID) bus.
VCCIOIN	1.05 voltage supply input for SoC TAP port, Intel ITP connector and PECI interface, Intel ME and South Complex.
VCCGBE	Power supply to SoC Integrated 10 GbE controller interface.
VCCSCSUS	SoC South Complex digital supply. The output voltage of this supply is selected by the SoC, using the serial voltage ID (SVID) bus.
VCCKRHV	High Voltage KR supply.
VCCKRLCPLL	Power supply to KR PLL. Filter version of VCCGBE, tie to VCCGBE on motherboard.
VCCKX4PLL	Power supply to PCIe Gen 3 PLL. Tie to VCCKRHV on motherboard.
VCCSCFUSESUS	1.7V SC Fuse LVR always ON supply.
VCCSCPLL	Supplies SC PLLs. Filtered version of VCCGBE, tied to VCCGBE on motherboard.
VCCSCSUS_SENSE, VSS_VCCSCSUS_SENSE	Remote sense signals for VCCSCSUS and are used by the voltage regulator to ensure accurate voltage regulation. These signals must be connected to the voltage regulator feedback circuit, which insures the output voltage remains within specification.
VCCGBE_SENSE VSS_VCCGBE_SENSE	Remote sense signals for VCCGBE and are used by the voltage regulator to ensure accurate voltage regulation. These signals must be connected to the voltage regulator feedback circuit, which insures the output voltage remains within specification
VCCIN_SENSE VSS_VCCIN_SENSE	VCCIN_SENSE and VSS_VCCIN_SENSE are remote sense signals for VCCIN MBVR12.5 and are used by the voltage regulator to ensure accurate voltage regulation. These signals must be connected to the voltage regulator feedback circuit, which insures the output voltage remains within specification.
DCPRTC	**Decoupling:** This signal is for RTC decoupling.
DCPSST	**Decoupling:** Internally generated 1.5V powered from Suspend Well. This signal requires decoupling. Decoupling is required even if this feature is not used
DCPSUS1	1.05V Suspend well power. If INTVRMEN is strapped high, power to this well is supplied internally and this pin should be left as no connect. If INTVRMEN is strapped low, power to this well must be supplied by an external 1.05 V suspend rail.
DCPSUS2	1.05V Suspend well power for USB 2.0. If INTVRMEN is strapped high, power to this well is supplied internally and this pin should be left as no connect. If INTVRMEN is strapped low, power to this well must be supplied by an external 1.05V suspend rail.
DCPSUS3	1.05V Suspend well power for USB 3.0. If INTVRMEN is strapped high, power to this well is supplied internally and these pins should be left as no connect. If INTVRMEN is strapped low, power to this well must be supplied by an external 1.05V suspend rail.
DCPSUSBYP	**Decoupling:** This signal is for decoupling internally generated 1.05V DeepSx only.
P1V05_PROC_IO	1.05V supply for SoC integrated processor interface signals. This power may be shut off in S3, S4, S5, or G3 states.
VCC	1.05V supply for PCH core well logic. This power may be shut off in S3, S4, S5, or G3 states.
VCC_SENSE	VCC_SENSE is remote sense signals for VCC and is used by voltage regulator to ensure accurate voltage regulation.
VCC3_3	3.3V supply for core well I/O buffers.
VCCADAC1_5	1.5V supply for Display DAC Analog Power. This power may be shut off in S3, S4, S5 or G3 states
VCCADACBG3_3	3.3V supply for Display DAC Band Gap. This power may be shut off in S3, S4, S5 or G3 states.
VCCAXCK1_05	Filter version of VCCCLK.
VCCCLK	1.05V analog power supply for internal clock PLL. This power may be shut off in S3, S4, S5 or G3 states.

Table 2-26. Power Signals (Sheet 2 of 2)

Signal Name	Description
VCCCLK3_3	3.3V Analog power supply for internal clock PLL. This power may be shut off in S3, S4, S5 or G3 states.
VCCRTC	3.3V (can drop to 2.0V min. in G3 state) supply for the RTC well. This power is not expected to be shut off unless the RTC battery is removed or completely drained. ***Note:*** Implementations should not attempt to clear CMOS by using a jumper to pull VccRTC low. Clearing CMOS can be done by using a jumper on RTCRST_N or GPI.
VCCIO	1.05V supply for SoC integrated PCH I/O buffers. This power may be shut off in S3, S4, S5, or G3 states.
VCCSUS3_3	3.3V supply for suspend well I/O buffers.
VCCUSBPLL	1.05V Analog power supply for USB PLL. This power may be shut off in S3, S4, S5, or G3 states.
VCCVRM	1.5V supply for internal VRMs. This power may be shut off in S3, S4, S5, or G3 states.
VSS	Ground

2.26 Integrated 10 GbE Controller Signals

High speed signals:

Group Name	Signal Name	Type	Name and Function
(n = 0 through 1 for port#)			
High Speed TX I/O and RX I/O	LAN0_KR_TX<**n**>_P LAN0_KR_TX<**n**>_N LAN1_KR_TX<**n**>_P LAN1_KR_TX<**n**>_N	OUT	KR PHY Tx Differential Output
	LAN0_KR_RX<**n**>_P LAN0_KR_RX<**n**>_N LAN1_KR_RX<**n**>_P LAN1_KR_RX<**n**>_N	IN	KR PHY Rx Differential Input

Group Name	Signal Name	Type	Name and Function
(n = 0 through 1 for port#)			
Management Interface for Physical-Layer (PHY) Components and LED Indicators. **Note:** MDIO and LED functions share the same interface pins, so only one can be operational at a time. These interfaces can be configured using NVM.	LAN0_I2C_SCL[**n**] LAN1_I2C_SCL[**n**]	I/O - OD	I2C Clock, of the two-wire management interface used to access the management registers of an external optical module of port n. One clock pulse is generated for each data bit transferred.
	LAN0_I2C_SDA[**n**] LAN1_I2C_SDA[**n**]	I/O - OD	I2C Data, of the two-wire management interface used to access the management registers of an external optical module of port n. Stable during the high period of the clock (unless it is a start or stop condition).
	LAN0_MDIO<**n**>_ LED<**n**>_[1:0] LAN1_MDIO<**n**>_ LED<**n**>_[1:0]	I/O - LVCMOS	Management Data. Bi-directional signal for serial data transfers between the MAC and the external PHY. Tristate buffer requires an external pull- up device. Programmable LEDs that can be used for Link Up indication.
	LAN0_MDC<**n**>_ LED<**n**>_[1:0] LAN1_MDC<**n**>_ LED<**n**>_[1:0] LAN1_MDC0_LED0_1_PECI_ID0	O - LVCMOS	Management Clock. Clock output for accessing the external PHY management registers. MDC clock frequency is proportional to link speed. At 10 Gb/s Link speed, MDC frequency can be set up to 2.4 MHz. Programmable LEDs that can be used for Link Up indication.
	LAN0_MDIO_DIR_ CTL_<**n**> LAN1_MDIO_DIR_ CTL_<**n**>	O - LVCMOS	MDIO Direction Control Pin. Used to control the direction of the level shifters.
Software Defined Pins (SDPs) For example, an external PHY topology (10 GbE SFP+ and 10GBASE-T) can detect an interrupt only on the rising edge of the signal from the PHY. Some discrete PHYs (like the X577-AT2 and Inphi CS4227) are designed for active-low signaling so adding a trigger inverter between the PHY and the level shifter on each pin is required to ensure proper functionality.	LAN0_SDP<**n**>_ [1:0] LAN1_SDP<**n**>_ [1:0]	I/O - LVCMOS	2 general purpose SDP Pins per port. Can be used to support IEEE 1588 auxiliary devices or input for external interrupts, etc.
System Management Interface - SMBus Shared by all four MACs.	LAN_SMBALRT_N	I/O - OD	SMBus Alert. Acts as an interrupt pin of a slave device on the SMBus.
	LAN_SMBCLK	I/O - OD	SMBus Clock. One clock pulse is generated for each data bit transferred.
	LAN_SMBDATA	I/O - OD	SMBus Data. Stable during the high period of the clock (unless it is a start or stop condition).

Group Name	Signal Name	Type	Name and Function
(n = 0 through 1 for port#)			
LAN NC-SI Management Interface	LAN_NCSI_CLK_IN	I - LVCMOS	The NC-SI clock input (LAN_NCSI_CLK_IN) should be connected to a NCSI specification-compliant 50 MHz clock generated on the platform (50 ppm).
	LAN_NCSI_RXD[1:0]	O - LVCMOS	The NC-SI receive data output signals (LAN_NCSI_RXD1 and LAN_NCSI_RXD0) should be connected to the NC-SI data inputs of the external Manageability Controller (MC).
	LAN_NCSI_TXD[1:0]	I - LVCMOS	The NC-SI transmit data input signals (LAN_NCSI_TXD1 and LAN_NCSI_TXD0) should be connected to the NC-SI data outputs of the external Manageability Controller (MC).
	LAN_NCSI_CRS_DV	O - LVCMOS	The NC-SI carrier sense/receive data valid signal output (LAN_NCSI_CRS_DV) should be connected to the CRS/DV input port on the external Manageability Controller (MC).
	LAN_NCSI_TX_EN	I - LVCMOS	The NC-SI transmit enable input signal (LAN_NCSI_TX_EN) should be connected to the transmit enable output of the external Manageability Controller (MC).
	LAN_NCSI_TRI_EN	O - LVCMOS	Connect the LAN_NCSI_TRI_EN pin to the enable pin of voltage translators for the NCSI output pins LAN_NCSI_RXD0/1 and LAN_NCSI_CRS_DV.
	LAN_NCSI_ARB_IN	I - LVCMOS	In a multi drop NC-SI topology, the NC-SI hardware arbitration input on the X552 (LAN_NCSI_ARB_IN) should be connected to the external Management Controller ARB_OUT pin.
	LAN_NCSI_ARB_OUT	O - LVCMOS	In multi-drop NC-SI topology, the NC-SI hardware arbitration output on the X552 (LAN_NCSI_ARB_OUT) should be connected to the external Management Controller ARB_IN pin.
Dedicated Flash Interface for LAN0	LAN0_FLSH_CLK	O - LVCMOS	Flash serial clock. Operates at the maximum frequency of 25 MHz.
	LAN0_FLSH_CS_N	O - LVCMOS	Flash chip select output.
	LAN0_FLSH_DI	O - LVCMOS	Serial data output to the Flash.
	LAN0_FLSH_DO	I - LVCMOS	Serial data input from the Flash.
Dedicated Flash Interface for LAN1	LAN1_FLSH_CLK	O - LVCMOS	Flash serial clock. Operates at the maximum frequency of 25 MHz.
	LAN1_FLSH_CS_N	O - LVCMOS	Flash chip select output.
	LAN1_FLSH_DI	O - LVCMOS	Serial data output to the Flash.
	LAN1_FLSH_DO	I - LVCMOS	Serial data input from the Flash.
Analog BIAS	LAN1_RBIAS	Analog	BIAS Control for LAN1_KR interface.
	LAN0_RBIAS	Analog	BIAS Control for LAN0_KR interface.

Group Name	Signal Name	Type	Name and Function
(n = 0 through 1 for port#)			
Crystal Pins.	LAN_XTAL_IN	Input	25 MHz Crystal Input for LAN and other SC units. Crystal is required even if LAN interface isn't used.
	LAN_XTAL_OUT	Output	Output of crystal oscillator circuit.

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3 Signal Pin States and Termination

This chapter describes the states of each SoC signal during reset sequencing and the S5 (Soft-Off) power state. It also documents what signals have internal pull-up/pull-down/series termination resistors and their values.

3.1 PCH Integrated Pull-Ups and Pull-Downs

Table 3-1. PCH Integrated Pull-Up and Pull-Down Resistors (Sheet 1 of 2)

Signal	Resistor Type	Nominal	Notes
USB2p/n[3:0]	Pull-down	15K	4
SATA1GP/GPIO19, SUSCLK/GPIO62, GPIO55, GPIO53, GPIO51,	Pull-up	20K	3, 7
SATA2GP/GPIO36, SATA3GP/GPIO37, SPKR	Pull-down	20K	3, 7
MFG_MODE_STRAP	Pull-down	15K	2, 7, 12
SATA4GP/GPIO16, SATA5GP/GPIO49	Pull-up	20K	3, 5
GPIO44, GPIO46, GPIO8	Pull-up	20K	3, 11
NMI#	Pull-up	20K	3, 6
USB3[T/R] [p/n] [2:1], USB3[T/R] [p/n] [6:5]	Pull-down	15K	4
SPI_CLK, SPI_CS[2:0]#	Pull-up	20K	3, 23
SPI_MOSI	Pull-up or Pull-down	20K	3, 22
SPI_MISO, SPI_IO3, SPI_IO2	Pull-up	20K	3, 8
PECI_PCH	Pull-down	350	17
LAD[3:0], LDRQ0#, LDRQ1#	Pull-up	20K	3
TACH[7:0]	Pull-up	20K	3, 19
PWRBTN#	Pull-up	20K	3
WAKE#	Pull-down	20K	3, 9, 19
GPIO31	Pull-down	20K	3, 9
SUSACK#	Pull-up	20K	2
GPIO27	Pull-down	20K	3, 9, 20
PME_N	Pull-up	20K	3
CLKOUT_PCI[4:0], CLKOUTFLEX3/GPIO67, CLKOUTFLEX1/GPIO65	Pull-down	20K	1, 10

Table 3-1. PCH Integrated Pull-Up and Pull-Down Resistors (Sheet 2 of 2)

Signal	Resistor Type	Nominal	Notes
SMI#	Pull-up	20K	3, 9
JTAG_TDI_PCH, JTAG_TMS_PCH	Pull-up	20K	3
JTAG_TCK_PCH	Pull-down	20K	3
PCIE_Tx/Rx_DP/DN[8:1], USB3[T/R] [p/n] [2:1], USB3[T/R] [p/n] [6:5] SATA_TX/RX p/n [6:1]	Pull-up or Pull-down	50	14

Notes:
1. Simulation data shows that these resistor values can range from 10 kΩ to 45 kΩ.
2. Simulation data shows that these resistor values can range from 9 kΩ to 50 kΩ.
3. Simulation data shows that these resistor values can range from 15 kΩ to 40 kΩ.
4. Simulation data shows that these resistor values can range from 14.25 kΩ to 24.8 kΩ.
5. GPIO16 has two native functions – The first native function (SATAP4_PCIEP1_SELECT) is selected if the Flex IO soft strap SATAP4_PCIEP1_MODE = 11b and takes precedence over any other assignments to this pin (that is, if this is selected, writes to GPIO_USE_SEL are ignored). If SATAP4_PCIEP1_MODE is not set to 11b, the GPIO_USE_SEL register can be used to select the second native function (SATA4GP) or GPIO functionality. Setting SATAP4_PCIEP1_MODE = 11b also enables an internal pull up resistor in this pin to allow Flexible I/O selection of SATA Port 4 or PCIe Port 1 to be done based on the type of card installed (If sampled value = 1, select SATA; if sampled value = 0, select PCIe). The same behavior is true of pin SATA5GP/GPIO49 when the soft strap SATAP5_PCIEP2_MODE = 11b. Soft straps are handled through FITc.
6. When operating as NMI# event indication pin function, the pin is open drain but the PCH provides an internal pull up to ensure the pin does not float.
7. This signal is a PCH functional strap; the pull-up or pull-down on this signal is disabled after it is sampled as a PCH functional strap.
8. This signal has a weak internal pull-up that always on.
9. When operating as SMI# event indication pin function, the pin is open drain but the PCH provides an internal pull up to ensure the pin does not float.
10. The pull down is disabled after the pins are driven strongly to logic 0 when PWROK is asserted.
11. The pull-up or pull-down on this signal is disabled after RSMRST# de-asserts. Pin must not be driven low until after RSMRST_N de-asserts.
12. The internal pull-down on MFG_MODE_STRAP is enabled during reset. However, the pin is strongly driven low after reset.
13. The controller link clock and data buffers use internal pull-up or pull-down resistors to drive a logical 1 or 0.
14. Termination resistors may be present if signal is enabled (that is, related Port is not disabled). These resistors appear to be strong pull downs or pull ups on the signals.
15. Internal pull down resistor may be enabled in Deep Sx mode based on DSX_CFG configuration bit, as follows: '1' (pin will be driven by platform in Deep Sx) -> Z; - '0' (pin will NOT be driven by platform in Deep Sx) -> Internal pull-down. Refer to DSX_CFG register (RCBA+3334h) for more details.
16. N/A
17. This is a 350-Ω normal pull-down, signal will be overridden to logic 1 with pull-up resistor (31 Ω) to VCC 1.05 V.
18. N/A
19. Regardless of internal pull up or pull down, an external pull up resistor is still required.
20. External pull-up if Intel wired LAN is present (pull up to SUS/DSW based on deepest wake on LAN support desired).
21. N/A
22. Weak internal pull-up resistor is enabled when APWROK is de-asserted and is switched to a weak internal pull-down resistor when APWROK and PLTRST# are both asserted.
23. Signals are tri-stated with weak pull-up resistors when APWROK is de-asserted. SPI_CS1# remains tri-stated with a weak pull-up resistor when APWROK and PLTRST# are both asserted.

3.2 Integrated PCH Output Signals Planes and States

Table 3-2 shows the power plane associated with the output and I/O signals, as well as the state at various times. Within the table, the following terms are used:

"DL"	SoC drives low.
"DH"	SoC drives high.
"IPU"	Internal pull-up
"IPD"	Internal pull-down
"T"	Toggling or signal is transitioning because function not stopping.

"High-Z"	Tri-state. SoC not driving the signal high or low.
"Defined"	Driven to a level that is defined by the function or external pull-up/pull-down resistor (will be high or low).
"Off"	The power plane is off; SoC is not driving when configured as an output or sampling when configured as an input.

Note: Pin state within table assumes interfaces are idle and default pin configuration for different power states.

Signal levels are the same in S3, S4 and S5, except as noted.

In general, integrated PCH suspend well signal states are indeterminate and undefined and may glitch prior to RSMRST# de-assertion.

PCH core well signal states are indeterminate and undefined and may glitch prior to PCH_PWROK assertion. However, this does not apply to THRMTRIP# as this signal is determinate and defined prior to PCH_PWROK assertion.

DSW indicates PCH Deep Sx Well. This state provides a few wake events and critical context to allow system to draw minimal power in S3, S4 or S5 states. In general, PCH DSW signal states are indeterminate, undefined and may glitch prior to DPWROK assertion. The signals that are determinate and defined prior to DPWROK assertion will have a note added as a reference.

Note: The Intel® Xeon® Processor D-1500 Product Family-based platform does not support DSW state. The DSW power well has been merged with VccSUS3_3.

Table 3-2. PCH Logic Output Signals - Power Plane and States (Sheet 1 of 3)

Signal Name	Power Plane	During Reset[5]	Immediately after Reset[5]	S3/S4/S5
USB Interface				
USB2p/n[3:0]	Suspend	IPD	IPD	IPD
USB3Tp/n[6:5, 2:1]	Suspend	IPD[1]	IPD[1]	S4 and S5 Off
PCI Express				
PCIE_Tx_DP/DN[8:1]	Core	IPD[1]	IPD[1]	Off
SATA Interface				
SATA_TXp/n[5:0]	Core	IPU[1]	IPU[1]	Off
SATALED#	Core	High-Z	High-Z	Off
SCLOCK	Core	High-Z	High-Z	Off
SLOAD	Core	High-Z	High-Z	Off
SDATAOUT[1:0]	Core	High-Z	High-Z	Off
Clocking Signals				
CLKOUT_ITPXDP_P/N	Core	T (platform dependent)	T (platform dependent)	Off
XTAL25_OUT	Core	High-Z	High-Z	Off
CLKOUT_PEG_P/N	Core	T	T	Off
CLKOUT_PCIE_P/N[7:0]	Core	T	T	Off
CLKOUT_PCI[4:0]	Core	T	T	Off
CLKOUTFLEX3, CLKOUTFLEX1	Core	T (platform dependent)	T (platform dependent)	Off
DIFFCLK_BIASREF	Core	High-Z	High-Z	Off
ICLK_IREF	Core	High-Z	High-Z	Off

Table 3-2. PCH Logic Output Signals - Power Plane and States (Sheet 2 of 3)

Signal Name	Power Plane	During Reset[5]	Immediately after Reset[5]	S3/S4/S5
Interrupt Interface				
SERIRQ	Core	High-Z	High-Z	Off
PIRQ[D:A]#	Core	High-Z	High-Z	Off
PIRQ[H:E]#	Core	High-Z	High-Z	Off
NMI#[4]	Core	IPU	IPU	Off
Processor Interface				
PROCPWRGD_PCH	Core	DL	DH	Off
PMSYNCH_PCH	Core	DL	DL	Off
MFG_MODE_STRAP	Suspend	IPD	DL	IPD
GPIO33	Core	IPD	IPD	Off
LPC Interface				
LAD[3:0]	Core	IPU	IPU	Off
LFRAME#	Core	DH	DH	Off
Non-Multiplexed GPIO Signals				
GPIO8	Suspend	IPU	DH	DH
GPIO15[4]	Suspend	DL	DL	DL
GPIO24[4]	Suspend	DL	DL	DL
GPIO28[4]	Suspend	DL	DL	DL
GPIO[53, 51]	Core	IPU	DH	Off
GPIO55	Core	IPU	DL	DL
SMBus Interface				
SMBCLK, SMBDATA	Suspend	High-Z	High-Z	High-Z
System Management Interface				
SML0DATA	Suspend	High-Z	High-Z	High-Z
SML0CLK	Suspend	High-Z	High-Z	High-Z
SML0ALERT#	Suspend	High-Z	High-Z[7]	High-Z
SML1ALERT#	Suspend	High-Z	High-Z	High-Z
SML1CLK	Suspend	High-Z	High-Z	High-Z
SML1DATA	Suspend	High-Z	High-Z	High-Z
SPI Interface				
SPI_CLK	Suspend	DL	DL	DL
SPI_CS0#	Suspend	DH	DH	DH
SPI_CS1#	Suspend	IPU	DH	DH
SPI_CS2#	Suspend	DH	DH	DH
SPI_MOSI	Suspend	IPD	DL	DL
SPI_MISO	Suspend	IPU	IPU	IPU
SPI_IO2	Suspend	IPU	IPU	IPU
SPI_IO3	Suspend	IPU	IPU	IPU
Power Management				
DRAMPWROK_PCH	Suspend	DL	High-Z	S3 High-Z, S4 and S5 DL
LAN_PHY_PWR_CTRL	DSW	DL	DL	DL
PLTRST#	Suspend	DL	DH	DL
PLTRST_PROC#	Core	DL	DH	DL

Table 3-2. PCH Logic Output Signals - Power Plane and States (Sheet 3 of 3)

Signal Name	Power Plane	During Reset[5]	Immediately after Reset[5]	S3/S4/S5
SLP_A#[2, 3]	DSW	DL	DH	DH
SLP_S3#[2]	DSW	DL	DH	DL
SLP_S4#[2]	DSW	DL	DH	S3 DH, S4 and S5 DL
SLP_SUS#[2]	DSW	DL	DH	DH
SUS_STAT#	Suspend	DL	DH	DL
SUSCLK	Suspend	IPU	T	
SUSWARN#/ SUSPWRDNACK[2, 4]	Suspend	DL	DL	DL
Thermal Signals				
PWM0	Core	DL	DL	Off
PECI_PCH	Core	DL	DL	Off
Miscellaneous Signals				
SPKR	Core	IPD	DL	Off
PCH_HOT#	Suspend	High-Z	High-Z	High-Z
JTAG_TDO	Suspend	High-Z	High-Z	High-Z

Notes:
1. This is a strong pull down (or pull up, as applicable).
2. The pin output shall not glitch during power up sequence.
3. The state of signals in S3-S5 will be defined by Intel ME Policies.
4. Based on wake events and ME state. SUSPWRDNACK is always '0' while in M0 or M3, but can be driven to 0 or 1 during the Moff state. SUSPWRDNACK is the default mode of operation. If the system supports DeepSx, then subsequent boots will default to SUSWARN# mode.
5. The states of signals on Core and processor power planes are evaluated at the times during PLTRST# and immediately after PLTRST#. The states of the Suspend signals are evaluated at the times during RSMRST# and Immediately after RSMRST#, with an exception to GPIO signals; refer to the EDS for more details on GPIO state after reset.

3.3 Integrated PCH Input and I/O Signals Planes and States

Table 3-3 shows the power plane associated with the input and I/O signals, as well as the state at various times. Within the table, the following terms are used:

"IPU"	Internal pull-up
"IPD"	Internal pull-down
"T"	Toggling or signal is transitioning because function not stopping.
"High-Z"	Tri-state. SoC not driving the signal high or low.
"Defined"	Driven to a level that is defined by the function or external pull-up/pull-down resistor (will be high or low).
"Off"	The power plane is off; SoC is not driving when configured as an output or sampling when configured as an input.

Note: Pin state within table assumes interfaces are idle and default pin configuration for different power states.

Signal levels are the same in S3, S4, and S5, except as noted.

In general, integrated PCH suspend well signal states are indeterminate and undefined and may glitch prior to RSMRST# de-assertion.

Integrated PCH core well signal states are indeterminate and undefined and may glitch prior to PCH_PWROK assertion. However, this does not apply to THRMTRIP# as this signal is determinate and defined prior to PCH_PWROK assertion.

DSW indicates integrated PCH Deep Sx Well. This state provides a few wake events and critical context to allow system to draw minimal power in S3, S4, or S5 states. In general, PCH DSW signal states are indeterminate, undefined and may glitch prior to DPWROK assertion. The signals that are determinate and defined prior to DPWROK assertion will have a note added as a reference.

Note that Intel® Xeon® Processor D-1500 Product Family-based platform does not support DSW state. The DSW power well has been merged with VccSUS3_3.

Table 3-3. Integrated PCH Input Signals - Power Plane and States (Sheet 1 of 3)

Signal Name	Power Plane	During Reset	Immediately after Reset	S3/S4/S5
USB Interface				
USB2p/n[3:0]	Suspend	IPD	IPD	IPD
USB3Rp/n[6:5, 2:1]	Suspend	IPD[1, 2]	IPD[1, 2]	S4 and S5 Off
OC0#[3], OC1#[3], OC2#[3], OC3#[3], OC4#[3], OC5#[3], OC6#[3], OC7#[3]	Suspend	High-Z	High-Z	High-Z
PCI Express*				
PERp/n[8:1]	Core	IPD[4]	IPD[4]	Off
SATA Interface				
SATA_RXp/n[5:0]	Core	IPD[2]	IPD[2]	Off
SATA0GP, SATA4GP, SATA5G	Core	High-Z	High-Z	Off
SATA1GP	Core	IPU	High-Z	Off
SATA2GP, SATA3GP	Core	IPD	High-Z	Off
Clocking Signals				
XTAL25_IN	Core	High-Z	High-Z	Off
CLKIN_33MHZLOOPBACK	Core	High-Z	High-Z	Off
DIFFCLK_BIASREF	Core	High-Z	High-Z	Off
ICLK_IREF	Core	High-Z	High-Z	Off
Processor Interface				
THRMTRIP#	Core	High-Z	High-Z	Off
Interrupt Interface				
SERIRQ	Core	High-Z	High-Z	Off
PIRQ[D:A]#	Core	High-Z	High-Z	Off
PIRQ[H:E]#	Core	High-Z	High-Z	Off
LPC Interface				
LAD[3:0]	Core	IPU	IPU	Off
LDRQ0# LDRQ1#	Core	IPU	IPU	Off

Table 3-3. Integrated PCH Input Signals - Power Plane and States (Sheet 2 of 3)

Signal Name	Power Plane	During Reset	Immediately after Reset	S3/S4/S5
Non-Multiplexed GPIO Signals				
GPIO8	Suspend	IPU	DH	DH
GPIO15	Suspend	DL	DL	DL
GPIO24	Suspend	DL	DL	DL
GPIO27	DSW	High-Z	High-Z	High-Z
GPIO28	Suspend	DL	DL	DL
GPIO50	Core	High-Z	High-Z	Off
GPIO51	Core	IPU	DH	Off
GPIO52	Core	High-Z	High-Z	Off
GPIO53	Core	IPU	DH	Off
GPIO54	Core	High-Z	High-Z	Off
GPIO55	Core	IPU	DL	DL
GPIO57	Suspend	DL	High-Z	High-Z
SMBus Interface				
SMBCLK, SMBDATA	Suspend	High-Z	High-Z	High-Z
SMBALERT#	Suspend	High-Z	High-Z	High-Z
System Management Interface				
INTRUDER#	RTC	High-Z	High-Z	High-Z
SML0DATA	Suspend	High-Z	High-Z	High-Z
SML0CLK	Suspend	High-Z	High-Z	High-Z
SML1CLK	Suspend	High-Z	High-Z	High-Z
SML1DATA	Suspend	High-Z	High-Z	High-Z
SPI Interface				
SPI_MOSI	Suspend	IPD	DL	DL
SPI_MISO	Suspend	IPU	IPU	IPU
SPI_IO2	Suspend	IPU	IPU	IPU
SPI_IO3	Suspend	IPU	IPU	IPU

Table 3-3. Integrated PCH Input Signals - Power Plane and States (Sheet 3 of 3)

Signal Name	Power Plane	During Reset	Immediately after Reset	S3/S4/S5
Power Management				
APWROK	Suspend	High-Z	High-Z	High-Z
BMBUSY#	Core	High-Z	High-Z	Off
DPWROK	RTC	High-Z	High-Z	High-Z
PWRBTN#	DSW	IPU	IPU	IPU
PCH_PWROK	RTC	High-Z	High-Z	High-Z
RI#	Suspend	High-Z	High-Z	High-Z
RSMRST#	RTC	High-Z	High-Z	High-Z
SUSACK#	Suspend	IPU	IPU	IPU
SYS_PWROK	Suspend	High-Z	High-Z	High-Z
SYS_RESET#	Core	High-Z	High-Z	Off
WAKE#	DSW	High-Z	High-Z	High-Z
Thermal Signals				
TACH0, TACH1, TACH2, TACH3, TACH4, TACH5, TACH6, TACH7	Core	IPU (TACH)	IPU(TACH)	Off
PECI_PCH	Core	DL[5]	DL[5]	Off
Miscellaneous Signals				
INTVRMEN	RTC	High-Z	High-Z	High-Z
DSWVRMEN	RTC	High-Z	High-Z	High-Z
RTCRST#	RTC	High-Z	High-Z	High-Z
SRTCRST#	RTC	High-Z	High-Z	High-Z
PME_N	Suspend	IPU	IPU	IPU
JTAG_TCK_PCH	Suspend	IPD	IPD	IPD
JTAG_TMS_PCH	Suspend	IPU	IPU	IPU
JTAG_TDI_PCH	Suspend	IPU	IPU	IPU

Notes:
1. USB3 Rx pins transition from High-Z to IPD after Reset.
2. This is a strong pull down (or pull up, as applicable).
3. Signals could be shared between ports.
4. PCIe Rx pins transition from High-Z to IPD after reset.
5. This is a 350 ohm normal pull-down, the signal will be overridden to logic 1 with pull-up resistor (31 ohms) to 1.05V.

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4 Signal DC and Timing Characteristics

This section documents the DC characteristics of the following signal groups or interfaces. All data in this chapter are pre-silicon estimates.

4.1 General DC Characteristics

4.1.1 General DC Input Characteristics

DC specifications are defined at the SoC pads, unless otherwise noted. DC specifications are only valid while meeting specifications for case temperature T_{CASE}, clock frequency, and input voltages. Care should be taken to read all notes associated with each specification.

4.1.2 SoC Integrated Processor Voltage and Current Specifications

Table 4-1. Voltage Specification (Sheet 1 of 2)

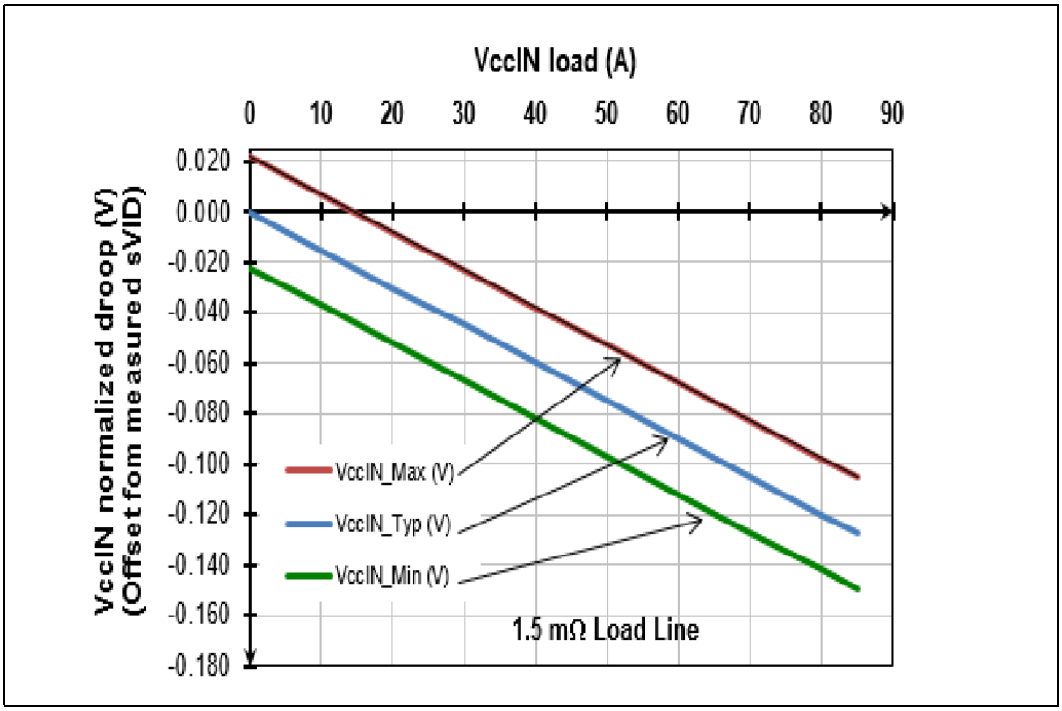
Voltage Rail	Description	Min	Nom	Max	Unit	Notes[1]
VCCIN	Input to Integrated Voltage Regulator (SVID address 00h) Vboot = 1.7V	1.6	1.82	1.95	V	2, 3, 4, 5, 8, 12
V_{VID_STEP}	VID step size during a transition		10.0		mV	6
VCCD	I/O Voltage for DDR4 (SVID address 02h)	0.95*VCCD_NOM	1.2	1.05*VCCD_NOM	V	2, 7, 9, 10, 11
	I/O Voltage for DDR3L (SVID address 02h)	0.95*VCCD_NOM	1.35	1.05*VCCD_NOM	V	2, 7, 9, 10, 11
VCCIOIN	CPU I/O Voltage	VCCIOIN_NOM - 5%	1.05	VCCIOIN_NOM + 5%	V	
VCCGBE	10GbE Controller (SVID address 03h)	VCCGBE_NOM - 0.018	1.05	VCCGBE_NOM +0.018	V	2, 13
VCCKRHV	Supply for KR/KX PHY	1.248	1.3	1.352	V	13
VCCSCSUS	South complex digital logic supply. (SVID address 01h) Vboot = 1.05V	NOM -5%	1.05	NOM + 5%	V	2, 13
VCCSCFUSESUS		1.615	1.7	1.785	V	13
VCC, VCCIO, VCCLK	PCH Logic supplies (SVID Address 03H)	NOM - 5%	1.05	NOM + 5%	V	2, 14
P1V05_PROC_IO	PCH Logic I/O Supply for CPU interface.	NOM - 5%	1.05	NOM + 5%	V	14

Table 4-1. Voltage Specification (Sheet 2 of 2)

Voltage Rail	Description	Min	Nom	Max	Unit	Notes[1]
VCCVRM, VCCADAC1_5	PCH Logic Internal VR supply.	1.43	1.50	1.58	V	14
VCCADACBG3_3, VCCCLK3_3, VCC3_3, VCCSUS3_3	Misc 3.3V supplies	3.14	3.30	3.47	V	14
VCCRTC	PCH RTC Supply	2.0	3.3	3.47	V	14

Notes:
1. Unless otherwise noted, all specifications in this table apply to all SKUs. These specifications are based on pre-silicon characterization and will be updated as further data becomes available.
2. These voltages are targets only. A SVID controlled variable voltage source should exist on systems in the event that a different voltage is required.
3. The V_{CCIN} voltage specification requirements are measured across the remote sense pin pairs (V_{CCIN_SENSE} and $V_{SS\_VCCIN\_SENSE}$) on the SoC package. Voltage measurement should be taken with a DC to 100 MHz bandwidth oscilloscope limit (or DC to 20 MHz for older model oscilloscopes), using a 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of the ground wire on the probe should be less than 5 mm to ensure external noise from the system is not coupled in the scope probe.VCCIN is a function of sVID setting and the load. The required voltage droop is depicted in Figure 4-1.
4. Refer to Table 4-5, "VCCIN Overshoot Specifications" and corresponding figure that the SoC should not be subjected to any static V_{CCIN} level that exceeds the V_{CCIN_MAX} associated with any particular current. Failure to adhere to this specification can shorten SoC lifetime.
5. Minimum V_{CCIN} and maximum I_{CCIN} are specified at the maximum SoC case temperature T_{CASE}. shown in the TMSDG document. I_{CCIN_MAX} is specified at the relative V_{CC_MAX} point on the V_{CCIN} load line. The SoC is capable of drawing I_{CCIN_MAX} for up to 4 ms.
6. This specification represents the V_{CCIN} reduction or V_{CCIN} increase due to each VID transition.
7. Baseboard bandwidth is limited to 20 MHz.
8. FMB is the flexible motherboard guidelines.
9. DC + AC + Ripple = Total Tolerance
10. V_{CCD} tolerance at SoC pins. Tolerance for VR at remote sense is ±3.3%*V_{CCD}.
11. The V_{CCD} voltage specification requirements are measured across vias on the platform. Choose V_{CCD} vias close to the package and measure with a DC to 100 MHz bandwidth oscilloscope limit (or DC to 20 MHz for older model oscilloscopes), using 1.5 pF maximum probe capacitance, and 1M ohm minimum impedance. The maximum length of the ground wire on the probe should be less than 5 mm to ensure external noise from the system is not coupled in the scope probe.
12. V_{CCIN} has a V_{boot} setting of 1.7V and is not included in the PWRGOOD_CPU indication.
13. The supply voltage is measured at the package pins. The tolerances shown in Table 4-1 are inclusive of all noise from DC up to 20 MHz. In testing, the voltage rails should be measured with a bandwidth limited oscilloscope that has a rolloff of 3 dB/decade above 20 MHz.

Figure 4-1. V_{CCIN} Static and Transient Tolerance Loadlines



Notes:
1. The VCCIN_MIN and VCCIN_MAX loadlines represent static and transient limits. Please see VCCIN Overshoot specifications.
2. The loadlines specify voltage limits at the die measured at the VCCIN_SENSE and VSS_VCCIN_SENSE lands. Voltage regulation feedback for voltage regulator circuits must also be taken from SoC VCCIN_SENSE and VSS_VCCIN_SENSE lands.
3. The Adaptive Voltage Positioning slope is 1.5 mΩ (mohm) with ±22 mV Tolerance of Band (TOB).
4. VCCIN_Vmax = VID(V) - 1.5 mΩ * ICCIN +22 mV
5. VCCIN_Vtyp = VID(V) - 1.5 mΩ * ICCIN
6. VCCIN_Vmin = VID(V) - 1.5 mΩ * ICCIN - 22 mV

Table 4-2. VCCIN Supply Current (I_{CCIN_MAX} and I_{CCIN_TDC}) Specification

SKU	TDP	ICC_MAX @ VCCIN	ICCIN_TDC @VCCIN	Pmax[2] (SoC)	Notes[1]
D-1553N	65W	75A	38A	130W	
D-1543N, D-1523N, D-1533N	45W	55A	26A	90W	
D-1513N	35W	43A	21A	70W	
D-1653N	65W	75A	39A	130W	3
D-1637	55W	66A	33A	110W	3
D-1649N, D-1633N, D-1627	45W	55A	27A	90W	3
D-1622	40W	48A	24A	80W	3
D-1623N	35W	43A	21A	70W	3
D-1602	27W	31A	16A	54W	3

1. Unless otherwise noted, all specifications in this table apply to all SKUs.
2.
3. For these SKUs, the workload assumed for maintaining P1 frequency at TDP is an average of the SPECint_rate benchmark. Marked frequency may not be maintained on more compute intensive workloads even if there is thermal margin as TDP is enforced by throttling. See Chapter 1, "Changes to Thermal Design Power (TDP) Workload" for more information.

Table 4-3. SoC CPU Section Current Specifications

Voltage Rail	Nominal Voltage (V)	TDC	Max ICC	Notes
VCCD - DDR4	1.2V	2.2A	2.45A	SoC only. During Memory training only. May last up to 5 seconds during boot.
	1.2V	0.81A	1.44	SoC only. Normal Operation.
VCCD - DDR3L	1.35V	5.7A	6.1A	SoC only. During Memory training only. May last up to 5 seconds during boot.
	1.35V	1.5A	2.7A	SoC only. Normal Operation.
VCCIOIN	1.05V	1.75A	2.1A	
VCCGBE	1.05V	2.5A	3.5A	
VCCKRHV + VCCKX4PLL	1.3V	0.25A	0.50A	Pins are tied together and sourced from the same supply.
VCCSCSUS	1.05V	14A	15.2A	
VCCSCFUSESUS	1.7V	0.30A	0.45A	
VCCKRLCPLL	1.05V	0.08A	0.15A	
VCCSCPLL	1.05V	0.08A	0.15A	

Table 4-4. SoC PCH Section Current Specifications

Voltage Rail	Voltage (V)	S0 Iccmax Current[3] (A)	S0 Idle Current[3] (A)	Sx Iccmax Current[3] (A)	Sx Idle Current[3] (A)	G3
VCC	1.05	1.312	0.130	0	0	0
VCCIO	1.05	3.491	0.199	0	0	0
VCCADAC1_5	1.5	0.004	0.002	0	0	0
VCCADACBG3_3	3.3	<1 mA	<1 mA	0	0	0
VCCCLK	1.05	0.306	0.089	0	0	0
VCCCLK3_3	3.3	0.055	0.011	0	0	0
VCCVRM	1.5	0.158	0.043	0	0	0
VCC3_3	3.3	0.133	0.003	0	0	0
VCCSUS3_3[4]	3.3	0.298	0.008	0.055	0.021	0
VCCRTC	3.3	N/A	N/A	N/A	N/A	6 uA See notes 1, 2.
P1V05_PROC_IO	1.05	0.004	0.002	0	0	0

1. Icc (RTC) data is taken with VccRTC at 3.0V while the system in a mechanical off (G3) state at room temperature.
2. S0 Iccmax Measurements taken at 110 °C (PCH die junction temperature) and S0 Idle/Sx Iccmax/Sx Idle measurements taken at 50 °C (PCH die junction temperature).
3. The VccSUS3_3 voltage regulator and associated power delivery circuitry should be capable of handling temporary inrush currents up to 2.5 A until the internally generated 1.05V rail (DcpSusByp) ramps. This inrush only occurs when coming from the G3 mechanical off (with missing/dead RTC battery) state.

4.1.3 SoC Integrated Processor Die Voltage Validation

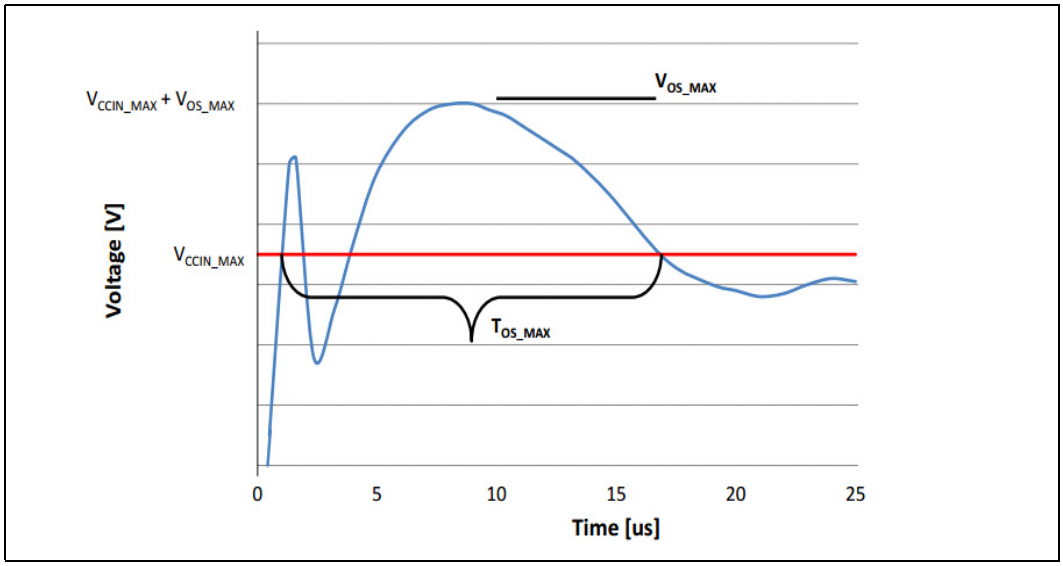
Core voltage (VCCIN) overshoot events at the SoC must meet the specifications in below table when measured across the VCCIN_SENSE and VSS_VCCIN_SENSE lands. Overshoot events that are < 10 ns in duration may be ignored. These measurements of SoC die level overshoot should be taken with a 100 MHz bandwidth limited oscilloscope.

The SoC can tolerate short transient overshoot events where VCCIN exceeds the VID voltage when transitioning from a high-to-low current load condition. This overshoot can't exceed VID + VOS_MAX (VOS_MAX is the maximum allowable overshoot above VID). These specifications apply to the SoC die voltage as measured across the VCCIN_SENSE and VSS_VCCIN_SENSE lands.

Table 4-5. V_{CCIN} Overshoot Specifications

Symbol	Parameter	Min	Max	Units	Figure	Notes
V_{OS_MAX}	Magnitude of V_{CCIN} overshoot above Vccin-max		50	mV	4-2	
T_{OS_MAX}	Time duration of V_{CCIN} overshoot above Vccin_max value at the new lighter load		25	us	4-2	

Figure 4-2. V_{CC} Overshoot Example Waveform



Notes:
1. V_{OS_MAX} is the measured overshoot voltage.
2. T_{OS_MAX} is the measured time duration above VccMAX.
3. VccinMAX = VID + 22 mV

4.1.4 Signal DC Specifications

4.1.4.1 DDR4 Signal

Table 4-6. DDR4 Signal DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes[1]
I_{IL}	Input Leakage Current	-1.4		1.4	mA	9
Data Signals: DDR{0/1}_DQ[63:0], DDR{0/1}_ECC[7:0], DDR{0/1}_DQS_D{P/N}[17:0]						
V_{OL}	Output Low Voltage		Varies			10
V_{OH}	Output High Voltage		VCCD		V	
R_{ON}	DDR4 Data Buffer On Resistance	27		33	ohm	6
Data ODT	On-Die Termination for Data Signals	45		55	ohm	8
Reference Clock Signals, Command Signals: DDR{0/1}_MA[13:0], DDR{0/1}_MA14_WE_N, DDR{0/1}_MA15_CAS_N, DDR{0/1}_MA16_RAS_N, DDR{0/1}_BA[1:0], DDR{0/1}_BG[0]_BA[2], DDR{0/1}_BG[1]_MA[14], DDR{0/1}_ACT_N_MA[15], DDR{0/1}_PAR, DDR{0/1}_CLK_D{P/N}[3:0]						
V_{OL}	Output Low Voltage		(V_{CCD} / 2)* (R_{ON} / (R_{ON}+R_{VTT_TERM}))		V	2, 7
V_{OH}	Output High Voltage		V_{CCD} - ((V_{CCD} / 2)* (R_{ON}/ (R_{ON}+R_{VTT_TERM}))		V	2, 5, 7
Reference Clock Signal: DDR{0/1}_CLK_D{P/N}[3:0]						
R_{ON}	DDR4 Clock Buffer On Resistance	27		33	ohm	6
Command Signals: DDR{0/1}_MA[13:0], DDR{0/1}_MA14_WE_N, DDR{0/1}_MA15_CAS_N, DDR{0/1}_MA16_RAS_N, DDR{0/1}_BA[1:0], DDR{0/1}_BG[0]_BA[2], DDR{0/1}_BG[1]_MA[14], DDR{0/1}_ACT_N_MA[15], DDR{0/1}_PAR						
R_{ON}	DDR4 Command Buffer On Resistance	16		20	ohm	6
R_{ON}	DDR4 Reset Buffer On Resistance		78		ohm	6
$V_{OL\_CMOS1.2v}$	Output Low Voltage, Signals DDR_RESET_N			0.2*V_{CCD}	V	1,2
$V_{OH\_CMOS1.2v}$	Output High Voltage, Signals DDR_RESET_N	0.9*V_{CCD}			V	1,2
Control Signals: DDR{0/1}_CS_N[1:0], DDR{0/1}_CS_N_[5:4], DDR{0/1}_CKE[3:0], DDR{0/1}_ODT[3:0]						
R_{ON}	DDR4 Control Buffer On Resistance	27		33	ohm	6
DDR4 Miscellaneous Signals						
ALERT_N	On-Die Termination for Parity Error Signals	81	90	99	ohm	
V_{IL}	Input Low Voltage DRAM_PWR_OK			304	mV	2, 3
V_{IH}	Input High Voltage DRAM_PWR_OK	800			mV	2, 4, 5

Notes:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The voltage rail VCCD which will be set to 1.2V nominal depending on the voltage of all DIMMs connected to the processor.

3. V_{IL} is the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
4. V_{IH} is the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
5. V_{IH} and V_{OH} may experience excursions above V_{CCD}. However, input signal drivers must comply with the signal quality specifications.
6. This is the pull down driver resistance. Refer to processor signal integrity models for I/V characteristics. Reset drive does not have a termination.
7. R_{VTT_TERM} is the termination on the DIMM and not controlled by the processor. Please refer to the applicable DIMM datasheet.
8. The minimum and maximum values for these signals are programmable by BIOS to one of the pairs.
9. Input leakage current is specified for all DDR4 signals.
10. Vol = Ron * [VCCD/(Ron + Rtt_Eff)], where Rtt_Eff is the effective pull-up resistance of all DIMMs in the system, including ODTs and series resistors on the DIMMs.

4.1.4.2 PECI_CPU DC Specification

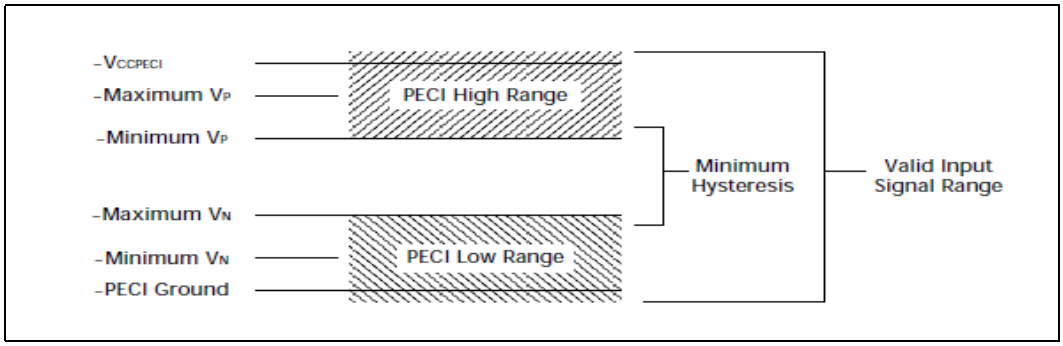
This section details the DC specifications for the PECI_CPU pin.

Table 4-7. PECI_CPU DC Specifications

Symbol	Definition and Conditions	Min	Max	Units	Notes[1]
V_{In}	Input Voltage Range	-0.150	VCCIOIN + 0.150	V	
$V_{Hysteresis}$	Hysteresis	0.100 * VCCIOIN		V	
V_N	Negative-edge threshold voltage	0.275 *VCCIOIN	0.500 * VCCIOIN	V	2
V_P	Positive-edge threshold voltage	0.550 * VCCIOIN	0.725 * VCCIOIN	V	2
I_{SOURCE}	High level output source V_{OH} = 0.75 * V_{CCIOIN}	-6.0		mA	
I_{Leak+}	High impedance state leakage to V_{CCIOIN} (V_{leak} = V_{OL})	50	200	µA	3
R_{ON}	High impedance leakage to GND (Vleak = Voh)	20	36	ohm	
C_{Bus}	Bus capacitance per node	N/A	10	pF	4,5
V_{Noise}	Signal noise immunity above 300 MHz	0.100 * V_{CCIOIN}	N/A	V_{p-p}	
	Output Edge Rate (50 ohm to VSS, between V_{IL} and V_{IH})	1.5	4	V/ns	

Notes:
1. VCCIOIN supplies the PECI interface. PECI behavior does not affect VCCIOIN min/max specification.
2. It is expected that the PECI driver will take into account, the variance in the receiver input thresholds and consequently, be able to drive its output within safe limits (-0.150V to 0.275*VCCIOIN for the low level and 0.725*VCCIOIN to VCCIOIN+0.150V for the high level).
3. The leakage specification applies to powered devices on the PECI bus.
4. One node is counted for each client and one node for the system host. Extended trace lengths might appear as additional nodes.
5. Excessive capacitive loading on the PECI line may slow down the signal rise/fall times and consequently limit the maximum bit rate at which the interface can operate.

Figure 4-3. PECI_CPU Input Device Hysteresis



4.1.4.3 Memory and LAN SMBus and LAN I2C DC Specifications

This section details the DC specifications for the DDR_SCL, DDR_SDA, LAN_SMBALRT_N, LAN_SMBCLK, LAN_SMBDATA, LAN_I2C_SCL[1:0] and LAN_I2C_SDA[1:0] pins.

Table 4-8. SMBus DC Specifications

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage		0.3*VCCIOIN	V	
V_{IH}	Input High Voltage	0.7*VCCIOIN		V	
$V_{Hysteresis}$	Hysteresis	0.1*VCCIOIN		V	
V_{OL}	Output Low Voltage		0.2*VCCIOIN	V	
R_{ON}	Buffer On Resistance	4	14	ohm	
I_L	Leakage Current	50	200	µA	
	Output Edge Rate (50 ohm to V_{TT}, between V_{IL} and V_{IH})	0.05	0.6	V/ns	

Note: Value obtained through test bench with 50 Ω pull up to VCCIOIN.

4.1.4.4 Integrated Processor JTAG and TAP Signals DC Specifications

This section details the DC specifications for the CPU side JTAG and TAP signals.

Table 4-9. JTAG and TAP Signals DC Specifications

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage		0.4*VCCIOIN	V	
V_{IH}	Input High Voltage	0.8*VCCIOIN		V	
V_{IL}	Input Low Voltage: JTAG_TCK_CPU		0.4*VCCIOIN	V	
V_{IH}	Input High Voltage: JTAG_TCK_CPU	0.6*VCCIOIN		V	
V_{OL}	Output Low Voltage: BPM_N[7:0], JTAG_TDO_CPU		0.2*VCCIOIN	V	
$V_{Hysteresis}$	Hysteresis	0.1*VCCIOIN		V	
R_{ON}	Buffer On Resistance BPM_N[7:0], JTAG_TDO_CPU	4	14	ohm	
I_{IL}	Input Leakage Current	50	200	µA	
	Output Edge Rate (50 ohm to V_{CCIOIN}) Signal: BPM_N[7:0], PRDY_N, TDO	0.2	1.5	V/ns	

Note:
1. These signals are measured between VIL and VIH.
2. The signal edge rate must be met or the signal must transition monotonically to the asserted state.

4.1.4.5 Serial VID Interface (SVID) DC Specifications

Table 4-10. Serial VID Interface (SVID) DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes
VCCIOIN	CPU I/O Voltage	VCCIOIN - 5%	1.05	VCCIOIN + 5%	V	1
V_{IL}	Input Low Voltage Signals SVID_DATA, SVIDALERT_N			0.4*VCCIOIN	V	1
V_{IH}	Input High Voltage Signals SVID_DATA, SVIDALERT_N	0.7*VCCIOIN			V	1
V_{OL}	Output Low Voltage Signals SVID_CLK, SVID_DATA			0.2*VCCIOIN	V	1,5
$V_{Hysteresis}$	Hysteresis	0.05*VCCIOIN			V	1
R_{ON}	Buffer On Resistance Signals SVID_CLK, SVID_DATA	4		14	ohm	2
I_{IL}	Input Leakage Current	50		200	µA	3
	Input Edge Rate Signal: SVIDALERT_N	0.05			V/ns	4
	Output Edge Rate (50 Ω to VCCIOIN)	0.20		1.5		4

Notes:
1. V_{CCIOIN} refers to instantaneous V_{CCIOIN}.
2. Measured at $0.31*V_{CCIOIN}$
3. Vin between 0V and V_{CCIOIN} (applies to SVIDDATA and SVIDALERT_N only).
4. These are measured between V_{IL} and V_{IH}.
5. Value is obtained through test bench with 50 Ω pull up to VCCIOIN.

4.1.4.6 SoC Integrated Processor Asynchronous Signal DC Specification

Table 4-11. SoC Misc Signal DC Specifications (Sheet 1 of 2)

Symbol	Parameter	Min	Max	Units	Notes
CMOS 1.05V Signal: BIST_ENABLE, BMCINIT, DEBUG_EN_N, PWRGOOD_CPU, PMSYNC_CPU, RESET_CPU_N, SAFE_MODE_BOOT, TXT_AGENT, TXT_PLTEN, LAN_PWRGOOD, RSMRST_CPU_N, SERIRQ_DATA, SERIRQ_CLK,DDR_PWRGOOD, THROTTLE_PECI_ID2					
$V_{IL\_CMOS1.05V}$	Input Low Voltage		0.4*VCCIOIN	V	1
$V_{IH\_CMOS1.05V}$	Input High Voltage	0.6*VCCIOIN		V	1
$I_{IL\_CMOS1.05V}$	Input Leakage Current	50	200	µA	1
Open Drain CMOS (ODCMOS) Signals: CATERR_N, ERROR_N[2:0], MEM_HOT_N, PROCHOT_N, THERMTRIP					
V_{IL_ODCMOS}	Input Low Voltage Signals: CATERR_N		0.4*VCCIOIN	V	
V_{IL_ODCMOS}	Input Low Voltage Signals: MEM_HOT_N, PROCHOT_N		0.3*VCCIOIN	V	
V_{IH_ODCMOS}	Input High Voltage Signals: CATERR_N, MEM_HOT_N, PROCHOT_N	0.7*VCCIOIN			
V_{OL_ODCMOS}	Output Low Voltage		0.2*VCCIOIN		1
$V_{Hysteresis}$	Hysteresis Signals: MEM_HOT_N, PROCHOT_N	0.1*VCCIOIN			
$V_{Hysteresis}$	Hysteresis Signal: CATERR_N	0.05*VCCIOIN			
I_L	Input Leakage Current		200	µA	1

Table 4-11. SoC Misc Signal DC Specifications (Sheet 2 of 2)

Symbol	Parameter	Min	Max	Units	Notes
R_{ON}	Buffer On Resistance	4	14	ohm	1
	Output Edge Rate Signal: MEM_HOT_ N, ERROR_N[2:0], THERMTRIP, PROCHOT_N	0.05	0.60	V/ns	2
	Output Edge Rate Signal: CATERR_N	0.20	1.5	V/ns	2
CMOS 1.05V Signal: LAN_XTAL_IN					
V_{IL}	Input Low Voltage	0	0.2	V	
V_{IH}	Input High Voltage	0.7	VCCGBE	V	3

Notes:
1. Row applies to all signals within group.
2. These are measured between V_{IL} and V_{IH}.
3. VCCGBE must be stable before driving LAN_XTAL_IN.

4.1.4.7 SoC Integrated PCH General DC Characteristics

Table 4-12. Single-Ended Signal DC Characteristics as Inputs or Outputs (Sheet 1 of 4)

Type	Symbol	Parameter	Min	Max	Units	Condition	Notes
Associated Signals: CLKIN_PCILOOPBACK, GPIO15, GPIO27, GPIO28, GPIO32, GPIO72, GPIO33, LDRQ1#/ GPIO23, LDRQ0#, LAD[3:0], LFRAME#, SERIRQ, GPIO8, GPIO44, GPIO45, GPIO46, LAN_PHY_PWR_CTRL/GPIO12, SATA0GP/GPIO21, SATA1GP/GPIO19, SATA2GP/GPIO36, SATA3GP/GPIO37, SATA4GP/GPIO16, SATA5GP/GPIO49, GPIO35/NMI#, GPIO18, GPIO20/SMI#, GPIO25, GPIO26, BMBUSY#/GPIO0, OC0#/GPIO59, OC1#/GPIO40, OC2#/ GPIO41, OC3#/GPIO42, OC4#/GPIO43, OC5#/GPIO9, OC6#/GPIO10, OC7#/GPIO14, PLTRST#, SPKR, PME_N, SPI_CLK, SPI_CS0#, SPI_CS1#, SPI_CS2#, SPI_MISO, SPI_MOSI, SPI_IO2, SPI_IO3							2
	V_{CC}	Supply Voltage Reference	3.14	3.47	V		
Input	V_{IH}	Input High Voltage	0.5 x V_{CC}	V_{CC} + 0.5	V		
	V_{IL}	Input Low Voltage	-0.5	0.3 x V_{CC}	V		
	I_{IL}	Input Leakage Current	-10	10	uA		3
	C_{IN}	Pin Input Capacitance	—	10	pF		4
Output	V_{OH}	Output High Voltage	0.9 x V_{CC}	—	V	I_{out}=-0.5 mA	1
	V_{OL}	Output Low Voltage	—	0.1 x V_{CC}	V	I_{out}=1.5 mA	
Associated Signals: SATALED#, SYS_RESET#, DRAMPWROK_PCH, GPIO24, GPIO57, GPIO51, GPIO54, GPIO52, GPIO53, GPIO50, RI#, SUS_STAT#/GPIO61, SUSACK#, SUSCLK/GPIO62, SUSWARN#/SUSPWRNACK/GPIO30, WAKE#, GPIO31, SLP_A#, SLP_LAN#, SLP_S3#, SLP_S4#, SLP_SUS#, SLP_WLAN#/GPIO29, PWRBTN#, TACH1/ GPIO1, TACH0/GPIO17, TACH2/GPIO6, TACH3/GPIO7, TACH4/GPIO68, TACH5/GPIO69, TACH6/GPIO70, TACH7/ GPIO71, PIRQE#/GPIO2, PIRQF#/GPIO3, PIRQG#/GPIO4, PIRQH#/GPIO5, PIRQA#, PIRQB#, PIRQC#, PIRQD#							2
	V_{CC}	Supply Voltage Reference	3.14	3.47	V		
Input	V_{HYS}	Schmitt Trigger Hysteresis	250	—	mVpp		
	V_{IH}	Input High Voltage	2	V_{CC} + 0.5	V		
	V_{IL}	Input Low Voltage	-0.5	0.8	V		
	I_{IL}	Input Leakage Current	-10	10	uA		
	C_{IN}	Pin Input Capacitance	—	10	pF		
Output	V_{OH}	Output High Voltage	V_{CC} — 0.5	V_{CC}	V	I_{out}=-2.0 mA	1
	V_{OL}	Output Low Voltage	—	0.4	V	I_{out}= 4.5 mA	

Table 4-12. Single-Ended Signal DC Characteristics as Inputs or Outputs (Sheet 2 of 4)

Type	Symbol	Parameter	Min	Max	Units	Condition	Notes
Associated Signals: SCLOCK/GPIO22, SDATAOUT0/GPIO39, SDATAOUT1/GPIO48, SLOAD/GPIO38, GPIO55							2
	V_{CC}	Supply Voltage Reference	3.14	3.47	V		
Input	V_{HYS}	Schmitt Trigger Hysteresis	250	—	mVpp		
	V_{IH}	Input High Voltage	2	V_{CC} + 0.5	V		
	V_{IL}	Input Low Voltage	-0.5	0.8	V		
	I_{IL}	Input Leakage Current	-10	10	uA		
	C_{IN}	Pin Input Capacitance	—	10	pF		
Output	V_{OH}	Output High Voltage	2.4	V_{CC}	V	I_{out}=-2.0 mA	1
	V_{OL}	Output Low Voltage	—	0.4	V	I_{out}=12 mA	
Associated Signals: SMBALERT#/GPIO11, SMBCLK, SMBDATA, SML0ALERT#/GPIO60, SML0CLK, SML0DATA, SML1ALERT#/TEMP_ALERT#/GPIO74, SML1CLK/GPIO58, SML1DATA/GPIO75, PWM0							2
	V_{CC}	Supply Voltage Reference	3.14	3.47	V		
Input							
	V_{IH}	Input High Voltage	2	V_{CC} + 0.5	V		
	V_{IL}	Input Low Voltage	-0.5	0.8	V		
	I_{IL}	Input Leakage Current	-10	10	uA		
	C_{IN}	Pin Input Capacitance	—	10	pF		
Output							
	V_{OH}	Output High Voltage	2.4	V_{CC}	V	I_{out}=-4.0 mA	1
	V_{OL}	Output Low Voltage	—	0.4	V	I_{out}=4 mA	
Associated Signals: SYS_PWROK, APWROK							2
Input	V_{CC}	Supply Voltage Reference	3.14	3.47	V		
	V_{HYS}	Schmitt Trigger Hysteresis	250	—	mVpp		
	V_{IH}	Input High Voltage	2.1	3.3	V		
	V_{IL}	Input Low Voltage	—	0.8	V		
	I_{IL}	Input Leakage Current	-10	10	uA		
	C_{IN}	Pin Input Capacitance	—	50	pF		
Associated Signals: JTAG_TCK_PCH, JTAG_TDI_PCH, JTAG_TDO_PCH, JTAG_TMS_PCH							2
Input	V_{CC}	Supply Voltage Reference	0.94	1.13	V		
	V_{HYS}	Schmitt Trigger Hysteresis	250	—	mVpp		
	V_{IH}	Input High Voltage	0.75	V_{CC} + 0.5	V		
	V_{IL}	Input Low Voltage	-0.5	0.3	V		
	I_{IL}	Input Leakage Current	-10	10	uA		
	C_{IN}	Pin Input Capacitance	—	10	pF		

Table 4-12. Single-Ended Signal DC Characteristics as Inputs or Outputs (Sheet 3 of 4)

Type	Symbol	Parameter	Min	Max	Units	Condition	Notes
Output	V_{OH}	Output High Voltage	0.75	—	V	I_{out}=-0.5 mA	1
	V_{OL}	Output Low Voltage	—	0.3	V	I_{out}=0.5mA	
Associated Signals: PECI_PCH							2
Input	V_{CC}	Supply Voltage Reference	0.9	1.15	V		
	V_{HYS}	Schmitt Trigger Hysteresis	0.1 x V_{CC}	—	mVpp		
	V_n	Negative edge threshold voltage	0.275 x V_{CC}	0.500 x V_{CC}	V		
	V_p	Positive edge threshold voltage	0.550 x V_{CC}	0.725 x V_{CC}	V		
	V_{IN}	Input Voltage Range	-0.15	V_{CC} + 0.15	V		
Output	V_{OH}	Output High Voltage	0.75 * VCC	—	V	IOH=-6 mA	1
	V_{OL}	Output Low Voltage	-	0.25 * VCC	V	IOL= 1 mA	
Associated Signals: PROCPWRGD_PCH, PLTRST_PROC#, PM_SYNC_PCH, THRMTRIP_PCH#							2
Input	V_{CC}	Supply Voltage Reference	0.9	1.15	V		
	V_{HYS}	Schmitt Trigger Hysteresis	0.1 x V_{CC}	—	mVpp		
	V_{IH}	Input High Voltage	0.81 x V_{CC}	—	V		
	V_{IL}	Input Low Voltage	—	0.51 x V_{CC}	V		
	I_{IL}	Input Leakage Current	-10	10	uA		
	C_{IN}	Pin Input Capacitance	—	10	pF		
Output	V_{OH}	Output High Voltage	V_{CC} - 0.3	—	V	IOH = -3 mA	1
	V_{OL}	Output Low Voltage	—	0.255	V	IOL = 3 mA	
Associated Signals: RSMRST#, INTVRMEN, RTCRST_N, SRTCRST#, INTRUDER#, PCH_PWROK, DPWROK, DSWVRMEN							2
VIL_RTC1		Input Low Voltage	-0.5	0.78	V		
VIH_RTC1		Input High Voltage	2.0	V_{CCRTC}+0.5	V		6
Associated Signals: RTCX1							
VIL_RTC3		Input Low Voltage	-0.5	0.1	V		
VIH_RTC3		Input High Voltage	0.8	1.2	V		
Associated Signals: XTAL25_IN, XTAL25_OUT							
V_{IL}		Maximum Input Low Voltage	-0.25	0.15	V		
V_{IH}		Minimum Input High Voltage	0.7	1.2	V		

Table 4-12. Single-Ended Signal DC Characteristics as Inputs or Outputs (Sheet 4 of 4)

Type	Symbol	Parameter	Min	Max	Units	Condition	Notes
Associated Signals: CLKOUT_PCI[4:0], CLKOUTFLEX1, CLKOUTFLEX3							
Output	V_{OH}	Output High Voltage	2.4		V		
	V_{OL}	Output Low Voltage		0.4	V		
	I_{OH}	Output High Current		-1	mA		
	I_{OL}	Output Low Current		1	mA		

Notes:
1. The V_{OH} specification does not apply to open-collector or open-drain drivers. Signals of this type must have an external pull-up resistor, and that is what determines the high-output voltage level. Refer to Chapter 2 for details on signal types.
2. Input characteristics apply when a signal is configured as Input or to signals that are only Inputs. Output characteristics apply when a signal is configured as an Output or to signals that are only Outputs. Refer to Chapter 2 for details on signal types.
3. PME_N Input Current Leakage is 1 uA max.
4. CLKIN_33MHZLOOPBACK has a pin capacitance in the range of 1 pF to 12 pF.
5. Only applies to FAST MODE (400 kbits/s).
6. VCCRTC is the voltage applied to the VCCRTC well of the PCH. When the system is in a G3 state, this is generally supplied by the coin cell battery, but for S5 and greater, this is generally VCCSUS3_3.

Table 4-13. Differential Signal DC Characteristics (Sheet 1 of 3)

Symbol	Parameter	Min	Max	Units	Notes
Associated Signals: PCIE_TX_DP[7:1], PCIE_TX_DN[7:1], PCIE_RX_DP[7:1], PCIE_RX_DN[7:1]					
Generation 1					
VTX-DIFF P-P	Differential Peak to Peak Output Voltage	0.8	1.2	V	1
VTX-DIFF P-P - Low	Low power differential Peak to Peak Output Voltage	0.4	1.2	V	
VTX_CM-ACp	TX AC Common Mode Output Voltage (2.5 GT/s)	-	20	mV	
ZTX-DIFF-DC	DC Differential TX Impedance	80	120	ohm	
VRX-DIFF p-p	Differential Input Peak to Peak Voltage	0.175	1.2	V	1
VRX_CM-ACp	AC peak Common Mode Input Voltage	-	150	mV	
Generation 2					
VTX-DIFF P-P	Differential Peak to Peak Output Voltage	0.8	1.2	V	1
VTX-DIFF P-P - Low	Low power differential Peak to Peak Output Voltage	0.8	1.2	V	
VTX_CM-ACp	TX AC Common Mode Output Voltage (2.5 GT/s)	-	100	mV	
ZTX-DIFF-DC	DC Differential TX Impedance		120	ohm	
VRX-DIFF p-p	Differential Input Peak to Peak Voltage	0.1	1.2	V	1
VRX_CM-ACp	AC peak Common Mode Input Voltage	-	150	mV	
Associated Signals: USB3R[N/P][6:5;2:1], USB3T[N/P][6:5; 2:1]					
VTX-DIFF P-P	Differential Peak to Peak Output Voltage	0.8	1.2	V	1
VTX-DIFF P-P - Low	Low power differential Peak to Peak Output Voltage	0.4	1.2	V	
Associated Signals: SATA_RXN[5:0], SATA_RXP[5:0], SATA_TXN[5:0], SATA_TXP[5:0]					
VIMIN10- Gen1i	Minimum Input Voltage - 1.5 Gb/s internal SATA	325	-	mVdiff p-p	2

Table 4-13. Differential Signal DC Characteristics (Sheet 2 of 3)

Symbol	Parameter	Min	Max	Units	Notes
VIMAX10-Gen1i	Maximum Input Voltage - 1.5 Gb/s internal SATA	-	600	mVdiff p-p	2
VIMIN10-Gen1m	Minimum Input Voltage - 1.5 Gb/s eSATA	240	-	mVdiff p-p	2
VIMAX10-Gen1m	Maximum Input Voltage - 1.5 Gb/s eSATA	-	600	mVdiff p-p	2
VIMIN10-Gen2i	Minimum Input Voltage - 3.0 Gb/s internal SATA	275	-	mVdiff p-p	2
VIMAX10-Gen2i	Maximum Input Voltage - 3.0 Gb/s internal SATA	-	750	mVdiff p-p	2
VIMIN10-Gen2m	Minimum Input Voltage - 3.0 Gb/s eSATA	240	-	mVdiff p-p	2
VIMAX10-Gen2m	Maximum Input Voltage - 3.0 Gb/s eSATA	-	750	mVdiff p-p	2
VIMIN10-Gen3i	Minimum Input Voltage - 6.0 Gb/s internal SATA	240	-	mVdiff p-p	2
VIMAX10-Gen3i	Maximum Input Voltage - 6.0 Gb/s internal SATA	-	1000	mVdiff p-p	2
VOMIN7-Gen1i,m	Minimum Output Voltage 1.5 Gb/s eSATA	400		mVdiff p-p	3
VOMAX7-Gen1i,m	Maximum Output Voltage 1.5 Gb/s eSATA	—	600	mVdiff p-p	3
VOMIN7-Gen2i,m	Minimum Output Voltage 3.0 Gb/s internal SATA	400	—	mVdiff p-p	3
VOMAX7-Gen2i,m	Maximum Output Voltage 3.0 Gb/s internal SATA	—	700	mVdiff p-p	3
VOMIN7-Gen3i	Minimum Output Voltage 6.0 Gb/s internal SATA	200	—	mVdiff p-p	3
VOMAX7-Gen3i	Maximum Output Voltage 6.0 Gb/s internal SATA	-	900	mVdiff p-p	3
Associated Signals: USB2_DN[3:0], USB2_DP[3:0]					
VDI	Differential Input Sensitivity - classic mode	0.2	-	V	4,6
VCM	Differential Common Mode Range - classic mode	0.8	2.5	V	5,6
VSE	Single-Ended Receiver Threshold - classic mode	0.8	2	V	6
VCRS	Output Signal Crossover Voltage - classic mode	1.3	2	V	6
VHSSQ	HS Squelch Detection Threshold - HS mode	100	150	mV	7
VHSDSC	HS Disconnect Detection Threshold - HS mode	525	625	mV	7
VHSCM	HS Data Signaling Common Mode Voltage Range - HS mode	-50	500	mV	7
VHSOI	HS Idle Level -HS mode	-10	10	mV	7
VHSOH	HS Data Signaling High -HS mode	360	440	mV	7
VHSOL	HS Data Signaling Low -HS mode	-10	10	mV	7
VCHIRPJ	Chirp J Level -HS mode	700	1100	mV	7

Table 4-13. Differential Signal DC Characteristics (Sheet 3 of 3)

Symbol	Parameter	Min	Max	Units	Notes
VCHIRPK	Chirp K Level -HS mode	-900	-500	mV	7
VOL	Output Low Voltage	—	0.4	V	6
VOH	Output High Voltage	3.3 V – 0.5	—	V	6

Notes:
1. PCI Express* mVdiff p-p = 2*|PETp[x] – PETn[x]|; PCI Express mVdiff p-p = 2*|PERp[x] – PERn[x]|
2. SATA Vdiff, RX (V_{IMAX}/V_{IMIN}) is measured at the SATA connector on the receiver side (generally, the motherboard connector), where SATA mVdiff p-p = 2*|SATA[x]RXP – SATA[x]RXN|.
3. SATA Vdiff, tx (V_{OMIN}/V_{OMAX}) is measured at the SATA connector on the transmit side (generally, the motherboard connector), where SATA mVdiff p-p = 2*|SATA[x]TXP – SATA[x]TXN|
4. V_{DI} = | USBPx[P] – USBPx[N] |
5. Includes VDI range.
6. Applies to Low-Speed/Full-Speed USB.
7. Applies to High-Speed USB 2.0.
8. USB 3.0 mVdiff p-p = 2*|USB3Rp[x] – USB3Rn[x]|; USB 3.0 mVdiff p-p = 2*|USB3Tp[x] – USB3Tn[x]|
9. Max PCIe* DC voltage is 3.6V, as specified in *PCIe Specification*, and maximum spike should not exceed 5.4V as specified in JEDEC specification JESD78.

4.1.4.8 KR Interface AC/DC Specifications

The KR interface supports the 10GBASE-KR electrical specification defined in IEEE802.3ap clause 72.

4.1.4.9 KX Interface AC/DC Specifications

The KX interface supports the 1000BASE-KX electrical specification defined in IEEE802.3ap clause 70.

4.1.4.10 Network Controller Sideband Interface (NC-SI) AC/DC Specifications

The NC-SI interface supports the NC-SI electrical specification as defined by the Distributed Management Task Force.

4.1.4.11 LAN_SPI, LAN_MDIO and LAN_SPD DC Specifications

This section details the DC specifications for the LAN[1:0]_MDIO[1:0], LAN[1:0]_MDIO_DIR_CTL, LAN[1:0]_SDP[1:0]_[1:0], LAN[1:0]_FLASH_CLK, LAN[1:0]_FLSH_CS_N, LAN[1:0]_FLSH_DI and LAN[1:0]_FLSH_DO pins.

Table 4-14. LAN SPI, MDIO and SDP DC Specifications

Symbol	Parameter	Min	Max	Units	Notes
V_{IL}	Input Low Voltage	-0.150	0.3*VCCIOIN	V	
V_{IH}	Input High Voltage	0.7*VCCIOIN	VCCIOIN +0.15	V	
$V_{Hysteresis}$	Hysteresis	0.1*VCCIOIN		V	
V_{OL}	Output Low Voltage		0.1*VCCIOIN	V	
V_{OH}	Output High Voltage	0.9 *VCCIOIN		V	
R_{ON}	Output Buffer On Resistance	20	50		
I_L	Leakage Current	-10	10	µA	

1. It is permissible to violate this specification if the SoC starts driving the strap before the hold time ends. The SoC will not drive an output which is also a strap until after it has latched the strap value.

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5 Operating Conditions and Power Requirements

Note: The information provided in this chapter is preliminary and subject to change. It is based on both pre-silicon engineering estimates and some post-silicon measurements. As they arise, notable changes to the operational characteristics and parameters will be updated in future revisions of this document.

5.1 Absolute Maximum and Minimum Ratings

Below table specifies absolute maximum and minimum ratings. At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

Although the processor contains protective circuitry to resist damage from Electro-Static Discharge (ESD), precautions should always be taken to avoid high static voltages or electric fields.

Table 5-1. SoC Integrated Processor Absolute Minimum and Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{CCIN}	Processor voltage with respect to Vss	-0.3	1.98	V
V_{CCD}	Processor I/O supply voltage for DDR4 (standard voltage) with respect to V_{SS}	-0.3	1.35	V
V_{CCD}	Processor I/O supply voltage for DDR3L (standard voltage) with respect to V_{SS}	-0.4	1.6	V
V_{CCIOIN}	Processor system agent voltage with respect to Vss	-0.3	1.35	V

Notes:
1. For functional operation, all processor electrical, signal quality, mechanical, and thermal specifications must be satisfied.
2. Overshoot and undershoot voltage guidelines for input, output, and I/O signals are outlined in Overshoot/ Undershoot Tolerance. Excessive overshoot or undershoot on any signal will likely result in permanent damage to the processor.

Table 5-2. SoC Integrated PCH Absolute Maximum Ratings

Parameter	Maximum Limits
Voltage on any integrated PCH 3.3V pin with respect to ground	-0.5 to Vcc3_3 + 0.4V
Voltage on any integrated PCH 1.5V pin with respect to ground	-0.5 to VccVRM + 0.5V
Voltage on any integrated PCH 1.05V (VCC, VCCIO) tolerant pin with respect to ground	-0.5 to Vcc + 0.5V
1.05V (VCC, VCCIO) Supply Voltage with respect to VSS	-0.5 to 1.3V
3.3V Supply Voltage with respect to VSS	-0.5 to 3.7V
P1V05_PROC_IO Supply Voltage with respect to VSS	-0.5 to 1.3V
1.5V Supply Voltage for the analog PLL with respect to VSS	-0.5 to 1.65V

The table above specifies absolute maximum and minimum ratings. At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits (but within the absolute maximum and minimum ratings) the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, instantaneous device damage can occur. If a device is subjected to these conditions for any length of time, it will either not function or its reliability will be severely degraded when returned to conditions within the functional operating condition limits.

Although the SoC contains protective circuitry to resist damage from Electrostatic Discharge (ESD), precautions should always be taken to avoid high static voltages or electric fields.

5.2 Storage Conditions Specifications

Environmental storage condition limits define the temperature and relative humidity limits to which the device is exposed to while being stored in a moisture barrier bag. The specified storage conditions are for component level prior to board attach (see notes in the table for post board attach limits).

The table below specifies absolute maximum and minimum storage temperature limits which represent the maximum or minimum device condition beyond which damage, latent or otherwise, may occur. The table also specifies sustained storage temperature, relative humidity, and time-duration limits. These limits specify the maximum or minimum device storage conditions for a sustained period of time. At conditions outside sustained limits, but within absolute maximum and minimum ratings, quality and reliability may be affected.

Table 5-3. Storage Condition Ratings

Symbol	Parameter	Min	Max	Unit
$T_{absolute\ storage}$	The non-operating device storage temperature. Damage (latent or otherwise) may occur when subjected to this temperature for any length of time in Intel Original sealed moisture barrier bag and / or box	-25	125 °C	1,2,3
$T_{sustained\ storage}$	The ambient storage temperature limit (in shipping media) for the sustained period of time as specified below in Intel Original sealed moisture barrier bag and / or box	-5	40 °C	1,2,3
$RH_{sustained\ storage}$	The maximum device storage relative humidity for the sustained period of time as specified below in Intel Original sealed moisture barrier bag and / or box	60% @ 24 °C		1,2,3
$Time_{sustained\ storage}$	Maximum time: associated with customer shelf life in Intel Original sealed moisture barrier bag and / or box	Moisture Sensitive Devices: 60 months from bag seal date; Non-moisture sensitive devices: 60 months from lot date		1,2,3

Notes:
1. TABSOLUTE STORAGE applies to the un-assembled component only and does not apply to the shipping media, moisture barrier bags or desiccant. Refers to a component device that is not assembled in a board or socket that is not to be electrically connected to a voltage reference or I/O signals.

2. Specified temperatures are based on data collected. Exceptions for surface mount re-flow are specified by applicable JEDEC J-STD-020 and MAS documents. The JEDEC, J-STD-020 moisture level rating and associated handling practices apply to all moisture sensitive devices removed from the moisture barrier bag.
3. Post board attach storage temperature limits are not specified for non-Intel branded boards. Consult your board manufacturer for storage specifications

5.2.1 Overshoot/Undershoot Tolerance

Overshoot (or undershoot) is the absolute value of the maximum voltage above or below $V_{SS,}$ see below figure. The overshoot/undershoot specifications limit transitions beyond V_{CCD} or V_{SS} due to the fast signal edge rates. The processor can be damaged by single and/or repeated overshoot or undershoot events on any input, output, or I/O buffer if the charge is large enough (that is, if the over/undershoot is great enough). Determining the impact of an overshoot/undershoot condition requires knowledge of the magnitude, the pulse direction, and the Activity Factor (AF). Permanent damage to the processor is the likely result of excessive overshoot/undershoot.

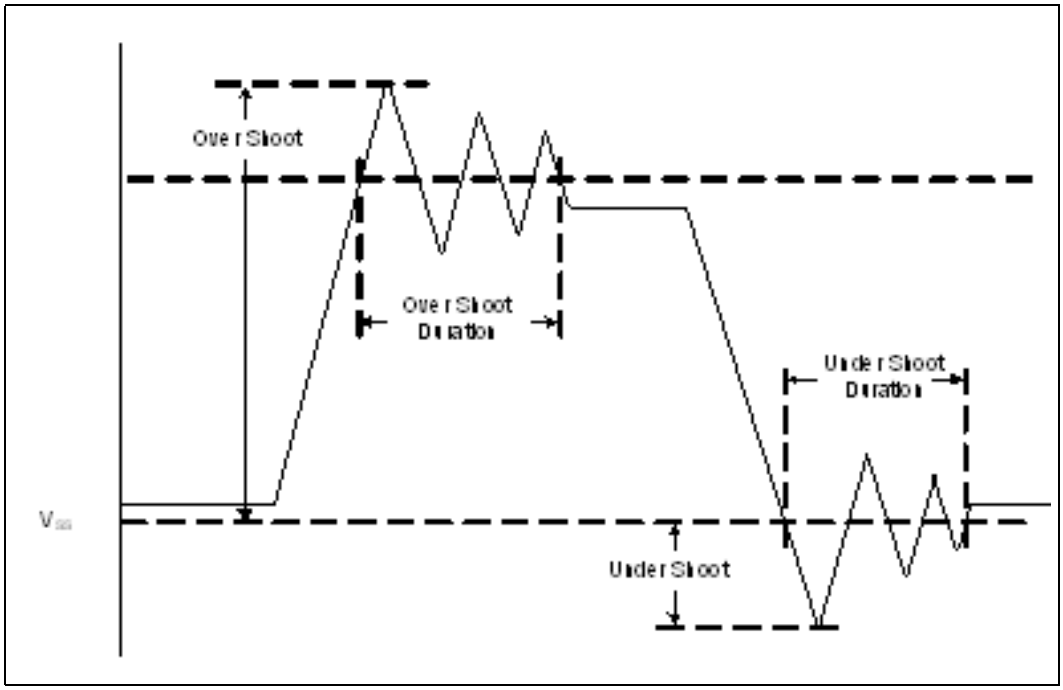
Baseboard designs which meet signal integrity and timing requirements and which do not exceed the maximum overshoot or undershoot limits listed in below table will insure reliable IO performance for the lifetime of the processor.

Table 5-4. Processor I/O Overshoot/Undershoot Specifications

Signal Group	Minimum Undershoot	Maximum Overshoot	Overshoot Duration	Undershoot Duration	Notes
DDR4	-0.22*V_{CCD}	1.22*V_{CCD}	0.25*T_{CH}	0.1*T_{CH}	1, 2, 3
Processor Asynchronous Sideband Signals	-0.35*V_{CCIOIN}	1.35*V_{CCIOIN}	1.25ns	0.5ns	1, 2
PWRGOOD_CPU Signal	-0.420V	V_{CCIOIN}+ 0.28	1.25ns	0.5ns	

Notes:
1. These specifications are measured at the processor pad.
2. Refer to Figure 5-1 for description of allowable overshoot/undershoot magnitude and duration.
3. Tch is the minimum high pulse width duration. It is nominally ½ of the DDR clock period.

Figure 5-1. Maximum Acceptable Overshoot/Undershoot Waveform



5.2.1.1 Overshoot/Undershoot Magnitude

Overshoot/Undershoot magnitude describes the maximum potential difference between a signal and its voltage reference level. For the processor, both overshoot and undershoot magnitude are referenced to V_{SS}. It is important to note that the overshoot and undershoot conditions are separate and their impact must be determined independently.

The pulse magnitude and duration, and activity factor must be used to determine if the overshoot/undershoot pulse is within specifications.

5.2.1.2 Overshoot/Undershoot Pulse Duration

Overshoot/undershoot pulse duration describes the total amount of time that an overshoot/undershoot event exceeds the overshoot/undershoot reference voltage. The total time could encompass several oscillations above the reference voltage. Multiple overshoot/undershoot pulses within a single overshoot/undershoot event may need to be measured to determine the total pulse duration.

Note: Oscillations below the reference voltage cannot be subtracted from the total overshoot/undershoot pulse duration.

5.2.1.3 Activity Factor

Activity Factor (AF) describes the frequency of overshoot (or undershoot) occurrence relative to a clock. Since the highest frequency of assertion of any common clock signal is every other clock, an AF = 0.1 indicates that the specific overshoot (or undershoot) waveform occurs every other clock cycle.

The specification provided in the table shows the maximum pulse duration allowed for a given overshoot/undershoot magnitude at a specific activity factor. Each table entry is independent of all others, meaning that the pulse duration reflects the existence of overshoot/undershoot events of that magnitude ONLY. A platform with an overshoot/undershoot that just meets the pulse duration for a specific magnitude where the AF < 0.1, means that there can be no other overshoot/undershoot events, even of lesser magnitude (note that if AF = 0.1, then the event occurs at all times and no other events can occur).

5.2.1.4 Reading Overshoot/Undershoot Specification Tables

The overshoot/undershoot specification for the processor is not a simple single value. Instead, many factors are needed to determine the over/undershoot specification. In addition to the magnitude of the overshoot, the following parameters must also be known: the width of the overshoot and the Activity Factor (AF). To determine the allowed overshoot for a particular overshoot event, the following must be done:

1. Determine the signal group a particular signal falls into.
2. Determine the magnitude of the overshoot or the undershoot (relative to VSS).
3. Determine the activity factor (How often does this overshoot occur?).
4. Next, from the appropriate specification table, determine the maximum pulse duration (in nanoseconds) allowed.
5. Compare the specified maximum pulse duration to the signal being measured. If the pulse duration measured is less than the pulse duration shown in the table, then the signal meets the specifications.

Undershoot events must be analyzed separately from overshoot events as they are mutually exclusive.

5.2.1.5 Determining if a System Meets the Overshoot/Undershoot Specifications

The overshoot/undershoot specifications listed in Table 4-5 specify the allowable overshoot/undershoot for a single overshoot/undershoot event. However most systems will have multiple overshoot and/or undershoot events that each have their own set of parameters (duration, AF and magnitude). While each overshoot on its own may meet the overshoot specification, when you add the total impact of all overshoot events, the system may fail. A guideline to ensure a system passes the overshoot and undershoot specifications is shown below.

1. If only one overshoot/undershoot event magnitude occurs, ensure it meets the over/undershoot specifications, OR
2. If multiple overshoots and/or multiple undershoots occur, measure the worst case pulse duration for each magnitude and compare the results against the AF = 0.1 specifications. If all of these worst case overshoot or undershoot events meet the specifications (measured time < specifications) in the table (where AF= 0.1), then the system passes.

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6 Intel® QuickData Technology Configuration Registers

The Intel® Xeon® Processor D-1500 NS product family implements the Intel® QuickData Technology 3.2 DMA engine. This is different from the Intel QuickData Technology 3.3 DMA present in the Intel Xeon Processor D-1500 product family.

The DMA is mapped to CPUBUSNO(0), Device 4, Functions 0-7. CPUBUSNO(0) is programmable by BIOS.

This section describes the standard PCI configuration registers and device specific Configuration Registers related to below:

- Intel QuickData Technology 3.2 DMA Registers - Device 4, Function 0 -7
- Intel QuickData Technology 3.2 MMIO Registers

6.1 Device 4 Function 0-7

Intel QuickData Technology PCI Configuration Registers.

Register Name	Offset	Size	Function
vid	0x0	16	0-7
did	0x2	16	0-7
pcicmd	0x4	16	0-7
pcists	0x6	16	0-7
rid	0x8	8	0-7
ccr	0x9	24	0-7
clsr	0xc	8	0-7
hdr	0xe	8	0-7
cb_bar	0x10	64	0-7
svid	0x2c	16	0-7
sdid	0x2e	16	0-7
capptr	0x34	8	0-7
intl	0x3c	8	0-7
intpin	0x3d	8	0-7
devcfg	0x60	16	0
msixcapid	0x80	8	0-7
msixnxtptr	0x81	8	0-7
msixmsgctl	0x82	16	0-7
tableoff_bir	0x84	32	0-7
pbaoff_bir	0x88	32	0-7
capid	0x90	8	0-7
nextptr	0x91	8	0-7
expcap	0x92	16	0-7

Register Name	Offset	Size	Function
devcap	0x94	32	0-7
devcon	0x98	16	0-7
devsts	0x9a	16	0-7
devcap2	0xb4	32	0-7
devcon2	0xb8	16	0-7
pmcap	0xe0	32	0-7
pmcsr	0xe4	32	0-7
dmauncerrsts	0x148	32	0
dmauncerrmsk	0x14c	32	0
dmauncerrsev	0x150	32	0
dmauncerrptr	0x154	8	0
dmaglberrptr	0x160	8	0
chanerr_int	0x180	32	0-7
chanerrmsk_int	0x184	32	0-7
chanerrsev_int	0x188	32	0-7
chanerrptr	0x18c	8	0-7

6.1.1 vid

Type: CFG **PortID:** N/A
Bus: 0 **Device:** 4 **Function:** 0-7
Offset: 0x0

Bit	Attr	Default	Description
15:0	RO	0x8086	vendor_identification_number: The value is assigned by PCI-SIG to Intel.

6.1.2 did

Type: CFG **PortID:** N/A
Bus: 0 **Device:** 4 **Function:** 0-7
Offset: 0x2

Bit	Attr	Default	Description
15:0	RO	0x2f20 (Function 0) 0x2f21 (Function 1) 0x2f22 (Function 2) 0x2f23 (Function 3) 0x2f24 (Function 4) 0x2f25 (Function 5) 0x2f26 (Function 6) 0x2f27 (Function 7)	device_identification_number: Device ID values vary from function to function.

6.1.3 pcicmd

Type: CFG Bus: 0 Offset: 0x4		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
10:10	RW	0x0	intx_interrupt_disable:
9:9	RO	0x0	fast_back_to_back_enable: Not applicable to PCI Express* and is hardwired to 0
8:8	RO	0x0	serre:
7:7	RO	0x0	idsel_stepping_wait_cycle_control: Not applicable to internal devices. Hardwired to 0.
6:6	RO	0x0	perre:
5:5	RO	0x0	vga_palette_snoop_enable: Not applicable to internal devices. Hardwired to 0.
4:4	RO	0x0	mwie:
3:3	RO	0x0	sce:
2:2	RW	0x0	bme:
1:1	RW	0x0	mse:
0:0	RO	0x0	iose:

6.1.4 pcists

Type: CFG Bus: 0 Offset: 0x6		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
15:15	RW1C	0x0	dpe:
14:14	RO	0x0	sse:
13:13	RO	0x0	rma:
12:12	RO	0x0	rta:
11:11	RW1C	0x0	sta:
10:9	RO	0x0	devsel_timing: Not applicable to PCI Express. Hardwired to 0.
8:8	RW1C	0x0	mdpe:
7:7	RO	0x0	fast_back_to_back: Not applicable to PCI Express. Hardwired to 0.
5:5	RO	0x0	pci66mhz_capable: Not applicable to PCI Express. Hardwired to 0.
4:4	RO	0x1	capabilities_list: This bit indicates the presence of a capabilities list structure
3:3	RO_V	0x0	intxsts:

6.1.5 rid

Type: CFG Bus: 0 Offset: 0x8		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
7:0	RO_V	0x0	revision_id: Reflects the Uncore Revision ID after reset. Reflects the Compatibility Revision ID after BIOS writes 0x69 to any RID register.

6.1.6 ccr

Type: CFG Bus: 0 Offset: 0x9		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
23:16	RO_V	0x8	base_class: Generic Device
15:8	RO_V	0x80	sub_class: Generic Device
7:0	RO_V	0x0	register_level_programming_interface: Set to 00h for all non-APIC devices.

6.1.7 clsr

Type: CFG Bus: 0 Offset: 0xc		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
7:0	RW	0x0	cacheline_size: This register is set as RW for compatibility reasons only. Cacheline size is always 64B.

6.1.8 hdr

Type: CFG Bus: 0 Offset: 0xe		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
7:7	RO	0x1	multi_function_device: This bit defaults to 1b since all these devices are multi-function
6:0	RO	0x0	configuration_layout: This field identifies the format of the configuration header layout. It is Type 0 for all these devices. The default is 00h, indicating a endpoint device.

6.1.9 cb_bar

Intel QuickData Technology Base Address Register

Type: CFG Bus: 0 Offset: 0x10			PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**	
63:14	RW	0x0	bar: This marks the 16 KB aligned 64-bit base address for memory-mapped registers of Intel QuickData Technology-DMA. The BAR register in the 8 functions will be referenced with a logical name of CB_BAR[0:7].	
3:3	RO	0x0	prefetchable: The DMA registers are not prefetchable.	
2:1	RO	0x2	type: The DMA registers is 64-bit address space and can be placed anywhere within the addressable region of the system.	
0:0	RO	0x0	memory_space: This Base Address Register indicates memory space.	

6.1.10 svid

Type: CFG Bus: 0 Offset: 0x2c			PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**	
15:0	RW_O	0x8086	vendor_identification_number:	

6.1.11 sdid

Type: CFG Bus: 0 Offset: 0x2e			PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**	
15:0	RW_O	0x0	subsystem_identification_number:	

6.1.12 capptr

Type: CFG Bus: 0 Offset: 0x34			PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**	
7:0	RO	0x80	capability_pointer: Points to the first capability structure for the device which is the PCIe capability.	

6.1.13 intl

Type: CFG	PortID: N/A	
Bus: 0	Device: 4	Function: 0-7
Offset: 0x3c		

Bit	Attr	Default	Description
7:0	RW	0x0	interrupt_line: NA for these devices

6.1.14 intpin

Type: CFG	PortID: N/A	
Bus: 0	Device: 4	Function: 0-7
Offset: 0x3d		

Bit	Attr	Default	Description
7:0	RW_O	0x1 (Function 0) 0x2 (Function 1) 0x3 (Function 2) 0x4 (Function 3) 0x1 (Function 4) 0x2 (Function 5) 0x3 (Function 6) 0x4 (Function 7)	cb_intpin0: (Function 0) cb_intpin1: (Function 1) cb_intpin2: (Function 2) cb_intpin3: (Function 3) cb_intpin4: (Function 4) cb_intpin5: (Function 5) cb_intpin6: (Function 6) cb_intpin7: (Function 7)

6.1.15 devcfg

This DEVCFG is for Function 0 only.

Type: CFG	PortID: N/A	
Bus: 0	Device: 4	Function: 0
Offset: 0x60		

Bit	Attr	Default	Description
11:11	RW_O	0x0	f1extop_diden: When set, this bit switches in the Function 1 Device ID that are typically used in storage applications. When clear, the function 1 DID remains at the default value associated with applications (for example, networking). This bit should be written by the BIOS prior to enumeration.
10:10	RW_O	0x0	f0extop_diden: When set, this bit switches in the Function 0 Device ID that are typically used in storage applications. When clear, the function 0 DID remains at the default value associated with applications (e.g.,networking). This bit should be written by the BIOS prior to enumeration.
9:9	RWS	0x0	enable_no_snoop: This bit is akin to the NoSnoop enable bit in the PCI Express capability register, only that this bit is controlled by bios rather than OS. When set, the no snoop optimization is enabled (provided the equivalent bit in the PCI Express DEVCON register is set) on behalf of Intel QuickData Technology DMA otherwise it is not. Notes: Due to severe performance degradation, it is not recommended that this bit be set except in debug mode.

6.1.16 msixcapid

MSI-X Capability ID

Type: CFG	PortID: N/A	
Bus: 0	Device: 4	Function: 0-7
Offset: 0x80		

Bit	Attr	Default	Description
7:0	RO	0x11	cb_msixcapid: Assigned by PCI-SIG for MSI-X (Intel QuickData Technology DMA).

6.1.17 msixnxtptr

MSI-X Next Pointer

Type: CFG	PortID: N/A	
Bus: 0	Device: 4	Function: 0-7
Offset: 0x81		

Bit	Attr	Default	Description
7:0	RO	0x90	cb_msixnxtptr: This field is set to 90h for the next capability list (PCI Express capability structure) in the chain.

6.1.18 msixmsgctl

MSI-X Message Control

Type: CFG	PortID: N/A	
Bus: 0	Device: 4	Function: 0-7
Offset: 0x82		

Bit	Attr	Default	Description
15:15	RW	0x0	msi_x_enable: Software uses this bit to select between MSI-X or INTx method for signaling interrupts from the DMA. 0: INTx method is chosen for DMA interrupts 1: MSI-X method is chosen for DMA interrupts
14:14	RW	0x0	function_mask: If 1, the 1 vector associated with the dma is masked, regardless of the per-vector mask bit state. If 0, the vector's mask bit determines whether the vector is masked or not. Setting or clearing the MSI-X function mask bit has no effect on the state of the per-vector Mask bit.
10:0	RO	0x0	table_size: Indicates the MSI-X table size which for IIO is 1, encoded as a value of 0h.

6.1.19 tableoff_bir

MSI-X Table Offset and BAR Indicator

Type: CFG **Bus:** 0 **Offset:** 0x84			**PortID:** N/A **Device:** 4 **Function:** 0-7
Bit	**Attr**	**Default**	**Description**
31:3	RO	0x400	table_offset: MSI-X Table Structure is at offset 8K from the Intel QuickData Technology BAR address. See "MSI-X Lower Address Registers (MSGADDR)" for the start of details relating to MSI-X registers.
2:0	RO	0x0	table_bir: Intel QuickData Technology DMA BAR is at offset 10h in the DMA config space and hence this register is 0.

6.1.20 pbaoff_bir

Type: CFG **Bus:** 0 **Offset:** 0x88			**PortID:** N/A **Device:** 4 **Function:** 0-7
Bit	**Attr**	**Default**	**Description**
31:3	RO	0x600	table_offset: MSI-X PBA Structure is at offset 12K from the Intel QuickData Technology BAR address.
2:0	RO	0x0	table_bir: Intel QuickData Technology DMA BAR is at offset 10h in the DMA config space and hence this register is 0.

6.1.21 capid

The PCI Express Capability List register enumerates the PCI Express Capability structure in the PCI 3.0 configuration space.

Type: CFG **Bus:** 0 **Offset:** 0x90			**PortID:** N/A **Device:** 4 **Function:** 0-7
Bit	**Attr**	**Default**	**Description**
7:0	RO	0x10	capability_id: Provides the PCI Express capability ID assigned by PCI-SIG.

6.1.22 nextptr

The PCI Express Capability List register enumerates the PCI Express Capability structure in the PCI 3.0 configuration space.

Type: CFG			**PortID:** N/A
Bus: 0			**Device:** 4 **Function:** 0-7
Offset: 0x91			
Bit	**Attr**	**Default**	**Description**
7:0	RO	0xe0	next_ptr: This field is set to the PCI Power Management capability.

6.1.23 expcap

The PCI Express Capabilities register identifies the PCI Express device type and associated capabilities.

Type: CFG			**PortID:** N/A
Bus: 0			**Device:** 4 **Function:** 0-7
Offset: 0x92			
Bit	**Attr**	**Default**	**Description**
13:9	RO	0x0	interrupt_message_number: N/A
8:8	RO	0x0	slot_implemented: N/A
7:4	RO	0x9	device_port_type: This field identifies the type of device. It is set to for the DMA to indicate root complex integrated endpoint device.
3:0	RO	0x2	capability_version: This field identifies the version of the PCI Express capability structure. Set to 2h for PCI Express and DMA devices for compliance with the extended base registers.

6.1.24 devcap

The PCI Express Device Capabilities register identifies device specific information for the device.

Type: CFG			**PortID:** N/A
Bus: 0			**Device:** 4 **Function:** 0-7
Offset: 0x94			
Bit	**Attr**	**Default**	**Description**
28:28	RWS_O	0x0	flr_supported:
27:26	RO	0x0	captured_slot_power_limit_scale: Does not apply to Intel QuickData Technology DMA.
25:18	RO	0x0	captured_slot_power_limit_value: Does not apply to Intel QuickData Technology DMA.
15:15	RO	0x1	role_based_error_reporting: IIO is 1.1 compliant and so supports this feature.
14:14	RO	0x0	power_indicator_present_on_device: Does not apply to Intel QuickData Technology DMA.

Type: CFG Bus: 0 Offset: 0x94		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
13:13	RO	0x0	attention_indicator_present: Does not apply to Intel QuickData Technology DMA.
12:12	RO	0x0	attention_button_present: Does not apply to Intel QuickData Technology DMA.
11:9	RO	0x0	endpoint_l1_acceptable_latency: N/A
8:6	RO	0x0	endpoint_l0s_acceptable_latency: N/A
5:5	RO	0x0	extended_tag_field_supported:
4:3	RO	0x0	phantom_functions_supported: Intel QuickData Technology DMA does not support phantom functions.
2:0	RO	0x0	max_payload_size: Intel QuickData Technology DMA supports max 128B on writes to PCI Express

6.1.25 devcon

The PCI Express Device Control register controls PCI Express specific capabilities parameters associated with the device.

Type: CFG Bus: 0 Offset: 0x98		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
15:15	RW	0x0	initiate_flr: Intel QuickData Technology DMA does a reset of that function only per the FLR ECN. This bit always returns 0 when read and a write of 0 has no impact.
14:12	RO	0x0	max_read_request_size: N/A to Intel QuickData Technology DMA since it does not issue tx on PCIe.
11:11	RW	0x1	enable_no_snoop: For Intel QuickData Technology DMA, when this bit is clear, all DMA transactions must be snooped. When set, DMA transactions to main memory can utilize No Snoop optimization under the guidance of the device driver.
10:10	RO	0x0	auxiliary_power_management_enable: Not applicable to Intel QuickData Technology DMA.
9:9	RO	0x0	phantom_functions_enable: Not applicable to Intel QuickData Technology DMA since it never uses phantom functions as a requester.
8:8	RO	0x0	extended_tag_field_enable:
7:5	RO	0x0	max_payload_size: N/A for Intel QuickData Technology DMA
4:4	RW	0x0	enable_relaxed_ordering: For most parts, writes from Intel QuickData Technology DMA are relaxed ordered, except for DMA completion writes. But the fact that Intel QuickData Technology DMA writes are relaxed ordered is not very useful except when the writes are also non-snooped. If the writes are snooped, relaxed ordering does not provide any particular advantage based on IIO uArch. But when writes are non-snooped, relaxed ordering is required to get good BW and this bit is expected to be set. If this bit is clear, NS writes will get terrible performance.

Type: CFG Bus: 0 Offset: 0x98		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
3:3	RO	0x0	unsupported_request_reporting_enable: N/A for Intel QuickData Technology DMA
2:2	RO	0x0	fatal_error_reporting_enable: N/A for Intel QuickData Technology DMA
1:1	RO	0x0	non_fatal_error_reporting_enable: N/A for Intel QuickData Technology DMA
0:0	RO	0x0	correctable_error_reporting_enable: N/A for Intel QuickData Technology DMA

6.1.26 devsts

The PCI Express Device Status register provides information about PCI Express device specific parameters associated with the device.

Type: CFG Bus: 0 Offset: 0x9a		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
5:5	RO	0x0	transactions_pending: 1: Indicates that the Intel QuickData Technology DMA device has outstanding Non-Posted Request which it has issued either towards main memory, which have not been completed. 0: Intel QuickData Technology DMA reports this bit cleared only when all Completions for any outstanding Non-Posted Requests it owns have been received.
4:4	RO	0x0	aux_power_detected: Does not apply to IIO
3:3	RO	0x0	unsupported_request_detected: N/A for Intel QuickData Technology DMA
2:2	RO	0x0	fatal_error_detected: N/A for Intel QuickData Technology DMA
1:1	RO	0x0	non_fatal_error_detected: N/A for Intel QuickData Technology DMA
0:0	RO	0x0	correctable_error_detected: N/A for Intel QuickData Technology DMA

6.1.27 devcap2

Type: CFG Bus: 0 Offset: 0xb4		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
4:4	RO	0x1	completion_timeout_disable_supported:
3:0	RO	0x0	completion_timeout_values_supported: Not Supported

6.1.28 devcon2

Type: CFG Bus: 0 Offset: 0xb8		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
4:4	RW	0x0	completion_timeout_disable:
3:0	RO	0x0	completion_timeout_value:

6.1.29 pmcap

Power Management Capability

The Power Management Capabilities Register defines the capability ID, next pointer and other power management related support. The following power management registers/ capabilities are added for software compliance.

Type: CFG Bus: 0 Offset: 0xe0		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
26:26	RO	0x0	d2_support: Does not support power management state D2.
25:25	RO	0x0	d1_support: Does not support power management state D1.
24:22	RO	0x0	aux_current:
21:21	RO	0x0	device_specific_initialization:
19:19	RO	0x0	pme_clock: This field is hardwired to 0h as it does not apply to PCI Express.
18:16	RWS_O	0x3	version: This field is set to 3h (Power Management 1.2 compliant) as version number. Bit is RW-O to make the version 2h in case legacy operating systems have any issues.
15:8	RO	0x0	next_capability_pointer: This is the last capability in the chain and hence set to 0.
7:0	RO	0x1	capability_id: Provides the Power Management capability ID assigned by PCI-SIG.

6.1.30 pmcsr

Power Management Control and Status

This register provides status and control information for Power Management events in the PCI Express port of the IIO.

Type: CFG **Bus:** 0 **Offset:** 0xe4			**PortID:** N/A **Device:** 4 **Function:** 0-7
Bit	**Attr**	**Default**	**Description**
31:24	RO	0x0	data: N/A
23:23	RO	0x0	bus_power_clock_control_enable: N/A
22:22	RO	0x0	b2_b3_support: N/A
15:15	RO	0x0	pme_status: N/A
14:13	RO	0x0	data_scale: N/A
12:9	RO	0x0	data_select: N/A
8:8	RO	0x0	pme_enable: N/A
3:3	RO	0x1	no_soft_reset: Indicates does not reset its registers when transitioning from D3hot to D0.
1:0	RW_V	0x0	power_state: This 2-bit field is used to determine the current power state of the function and to set a new power state as well. 00: D0 01: D1 (not supported) 10: D2 (not supported) 11: D3_hot If Software tries to write 01 or 10 to this field, the power state does not change from the existing power state which is either (D0 or D3_hot) and nor do these bits[1:0] change value. When in D3_hot state, the DMA will: a) Respond to only Type 0 configuration transactions targeted at the device's configuration space, when in D3_hot state. c) Will not respond to memory i.e., $D3_{HOT}$ state is equivalent to MSE, accesses to MBAR region note: ABAR region access still go through in D3_hot state, if it enabled. d) Will not generate any MSI writes.

6.1.31 dmauncerrsts

DMA Cluster Uncorrectable Error Status

Type: CFG **Bus:** 0 **Offset:** 0x148		**PortID:** N/A **Device:** 4	**Function:** 0
Bit	**Attr**	**Default**	**Description**
12:12	RW1CS	0x0	syndrome: Multiple errors
10:10	RW1CS	0x0	read_address_decode_error_status:
7:7	RW1CS	0x0	rd_cmpl_header_error_status:
3:3	RW1CS	0x0	dma_internal_hw_parity_error_status:
2:2	RW1CS	0x0	received_poisoned_data_from_dp_status:

6.1.32 dmauncerrmsk

DMA Cluster Uncorrectable Error Mask

Type: CFG **Bus:** 0 **Offset:** 0x14c		**PortID:** N/A **Device:** 4	**Function:** 0
Bit	**Attr**	**Default**	**Description**
12:12	RWS	0x0	syndrome: Multiple errors
10:10	RWS	0x0	read_address_decode_error_mask:
7:7	RWS	0x0	rd_cmpl_header_error_mask:
4:4	RWS	0x0	cfg_reg_parity_error_mask:
3:3	RWS	0x0	dma_internal_hw_parity_error_mask:
2:2	RWS	0x0	received_poisoned_data_from_dp_mask:

6.1.33 dmauncerrsev

DMA Cluster Uncorrectable Error Severity

This register controls severity of uncorrectable DMA unit errors between fatal and non-fatal.

Type: CFG **Bus:** 0 **Offset:** 0x150		**PortID:** N/A **Device:** 4	**Function:** 0
Bit	**Attr**	**Default**	**Description**
12:12	RWS	0x0	syndrome: Multiple errors
10:10	RWS	0x0	read_address_decode_error_severity:
7:7	RWS	0x1	rd_cmpl_header_error_severity:

Type: CFG	PortID: N/A		
Bus: 0	Device: 4	Function: 0	
Offset: 0x150			
Bit	**Attr**	**Default**	**Description**
4:4	RWS	0x1	cfg_reg_parity_error_severity:
3:3	RWS	0x1	dma_internal_hw_parity_error_severity:
2:2	RWS	0x0	received_poisoned_data_from_dp_severity:

6.1.34 dmauncerrptr

DMA Cluster Uncorrectable Error Pointer

Type: CFG	PortID: N/A		
Bus: 0	Device: 4	Function: 0	
Offset: 0x154			
Bit	**Attr**	**Default**	**Description**
4:0	ROS_V	0x0	uncerrptr: Points to the first unmasked uncorrectable error logged in the DMAUNCERRSTS register. This field is only valid when the corresponding error is unmasked and the status bit is set and this register is rearmed to load again once the error pointed by this field in the uncorrectable error status register is cleared.Value of 0x0 corresponds to bit 0 in DMAUNCERRSTS register, value of 0x1 corresponds to bit 1, etc.

6.1.35 dmaglberrptr

DMA Cluster Global Error Pointer

Type: CFG	PortID: N/A		
Bus: 0	Device: 4	Function: 0	
Offset: 0x160			
Bit	**Attr**	**Default**	**Description**
3:0	ROS_V	0x0	global_error_pointer: Points to one of 8 possible sources of uncorrectable errors – DMA channels 0-7. The DMA channel errors are logged in CHANERRx_INT registers. This register is only valid when the register group pointed to by this register has at least one unmasked error status bit set and this register is rearmed to load again once all the unmasked uncorrectable errors in the source pointed to by this field are cleared. Value of 0x0 corresponds to channel#0, value of 0x1 corresponds to channel#1, and value of 0x7 corresponds to channel#7.

6.1.36 chanerr_int

Internal DMA Channel Error Status Registers

Type: CFG Bus: 0 Offset: 0x180		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
18:18	RW1CS (Function 0-1) RO (Function 2-7)	0x0	desccnterr: (Function 0-1) The hardware sets this bit when it encounters a base descriptor that requires an extended descriptor (such as an XOR with 8 sources), but DMACount indicates that the Base descriptor is the last descriptor that can be processed. Reserved. (Function 2-7)
17:17	RW1CS (Function 0-1) RO (Function 2-7)	0x0	xorqerr: The hardware sets this bit when the Q validation part of the XOR with Galois Field Multiply Validate operation fails. Reserved. (Function 2-7)
16:16	RW1CS	0x0	crc_xorp_err: The hardware sets this bit when a CRC Test operation or XOR Validity operation fails or when the P validation part of the XOR with Galois Field Multiply Validate operation fails.
15:15	RO	0x0	unaffil_err: Unaffiliated Error. IIO never sets this bit
14:14	RO	0x0	unused:
13:13	RW1CS	0x0	int_cfg_err: Interrupt Configuration Error. The DMA channel sets this bit indicating that the interrupt registers were not configured properly when the DMA channel attempted to generate an interrupt e.g., interrupt address is not 0xFEE.
12:12	RW1CS	0x0	cmp_addr_err: Completion Address Error. The DMA channel sets this bit indicating that the completion address register was configured to an illegal address or has not been configured.
11:11	RW1CS	0x0	desc_len_err: Descriptor Length Error. The DMA channel sets this bit indicating that the current transfer has an illegal length field value. When this bit has been set, the address of the failed descriptor is in the Channel Status register.
10:10	RW1CS	0x0	desc_ctrl_err: Descriptor Control Error. The DMA channel sets this bit indicating that the current transfer has an illegal control field value. When this bit has been set, the address of the failed descriptor is in the Channel Status register.
9:9	RW1CS	0x0	wr_data_err: Write Data Error. The DMA channel sets this bit indicating that the current transfer has encountered an error while writing the destination data. This error could be because of an internal ram error in the write queue that stores the write data before being written to main memory. When this bit has been set, the address of the failed descriptor is in the Channel Status register.
8:8	RW1CS	0x0	rd_data_err: Read Data Error. The DMA channel sets this bit indicating that the current transfer has encountered an error while accessing the source data. This error could be a read data that is received poisoned. When this bit has been set, the address of the failed descriptor is in the Channel Status register.
7:7	RW1CS	0x0	dma_data_parerr: DMA Data Parity Error. The DMA channel sets this bit indicating that the current transfer has encountered an uncorrectable ECC/parity error reported by the DMA engine.

Type: CFG	PortID: N/A	
Bus: 0	Device: 4	Function: 0-7
Offset: 0x180		

Bit	Attr	Default	Description
6:6	RW1CS	0x0	cdata_parerr: Data Parity Error. The DMA channel sets this bit indicating that the current transfer has encountered a parity error. When this bit has been set, the address of the failed descriptor is in the Channel Status register.
5:5	RW1CS	0x0	chancmd_err: CHANCMD Error. The DMA channel sets this bit indicating that a write to the CHANCMD register contained an invalid value (e.g., more than one command bit set).
4:4	RW1CS	0x0	chn_addr_valerr: Chain Address Value Error. The DMA channel sets this bit indicating that the CHAINADDR register has an illegal address including an alignment error (not on a 64-byte boundary).
3:3	RW1CS	0x0	descriptor_error: The DMA channel sets this bit indicating that the current transfer has encountered an error (not otherwise covered under other error bits) when reading or executing a DMA descriptor. When this bit has been set and the channel returns to the Halted state, the address of the failed descriptor is in the Channel Status register.
2:2	RW1CS	0x0	nxt_desc_addr_err: Next Descriptor Address Error. The DMA channel sets this bit indicating that the current descriptor has an illegal next descriptor address including an alignment error (not on a 64-byte boundary). When this bit has been set and the channel returns to the Halted state, the address of the failed descriptor is in the Channel Status register.
1:1	RW1CS	0x0	dma_xfrer_daddr_err: DMA Transfer Destination Address Error. The DMA channel sets this bit indicating that the current descriptor has an illegal destination address. When this bit has been set, the address of the failure descriptor has been stored in the Channel Status register.
0:0	RW1CS	0x0	dma_trans_saddr_err: DMA Transfer Source Address Error. The DMA channel sets this bit indicating that the current descriptor has an illegal source address. When this bit has been set, the address of the failure descriptor has been stored in the Channel Status register.

6.1.37 chanerrmsk_int

Internal DMA Channel Error Mask Registers

Type: CFG Bus: 0 Offset: 0x184		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
18:18	RWS (Function 0-1) RO (Function 2-7)	0x0	mask18: This register is a bit for bit mask for the CHANERR_INT register. 0: Enable 1: Disable
17:17	RWS (Function 0-1) RO (Function 2-7)	0x0	mask17: This register is a bit for bit mask for the CHANERR_INT register. 0: Enable 1: Disable
16:16	RWS	0x0	mask16: This register is a bit for bit mask for the CHANERR_INT register. 0: Enable 1: Disable
15:15	RO	0x0	chanerrintmskro:
13:0	RWS	0x0	mask13_0: This register is a bit for bit mask for the CHANERR_INT register. 0: Enable 1: Disable

6.1.38 chanerrsev_int

Internal DMA Channel Error Severity Registers

Type: CFG Bus: 0 Offset: 0x188		PortID: N/A Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
18:18	RWS (Function 0-1) RO (Function 2-7)	0x0	severity18: (Function 0-1) 1: Corresponding error logged in the CHANERR_INT register is escalated as fatal error to the IIO internal core error logic. 0: That error is escalated as non-fatal to the IIO internal core error logic. Reserved. (Function 2-7)
17:17	RWS (Function 0-1) RO (Function 2-7)	0x0	severity17: (Function 0-1) 1: Corresponding error logged in the CHANERR_INT register is escalated as fatal error to the IIO internal core error logic. 0: That error is escalated as non-fatal to the IIO internal core error logic. Reserved. (Function 2-7)

Type: CFG	PortID: N/A	
Bus: 0	Device: 4	Function: 0-7
Offset: 0x188		

Bit	Attr	Default	Description
16:16	RWS	0x0	severity16: 1: Corresponding error logged in the CHANERR_INT register is escalated as fatal error to the IIO internal core error logic. 0: That error is escalated as non-fatal to the IIO internal core error logic.
15:14	RO	0x0	chanerrsevro1_0:
13:0	RWS	0x0	severity13_0: 1: Corresponding error logged in the CHANERR_INT register is escalated as fatal error to the IIO internal core error logic. 0: That error is escalated as non-fatal to the IIO internal core error logic.

6.1.39 chanerrptr

DMA Channel Error Pointer

Type: CFG	PortID: N/A	
Bus: 0	Device: 4	Function: 0-7
Offset: 0x18c		

Bit	Attr	Default	Description
4:0	ROS_V	0x0	dma_chan_err_pointer: Points to the first uncorrectable, unmasked error logged in the CHANERR_INT register. This register is only valid when the corresponding error is unmasked and its status bit is set and this register is rearmed to load again once the error pointed to by this register, in the CHANERR_INT status register, is cleared.

6.2 Device 4 Function 0 - 7 MMIO Region Intel QuickData Technology BARs

Intel QuickData Technology MMIO Register used to control the DMA functionality. The Intel QuickData Technology BAR register points to the based address to these registers.

All of these registers are accessible from only the processor. The IIO supports accessing the Intel QuickData Technology device memory-mapped registers via QWORD reads and writes. The offsets indicated in the following table are from the Intel QuickData Technology BAR value.

Register Name	Offset	Size
chancnt	0x0	8
xfercap	0x1	8
genctrl	0x2	8
intrctrl	0x3	8
attnstatus	0x4	32
cbver	0x8	8
intrdelay	0xc	16
cs_status	0xe	16
dmacapability	0x10	32
dcaoffset	0x14	16
cbprio	0x40	8
chanctrl	0x80	16
dma_comp	0x82	16
chancmd	0x84	8
dmacount	0x86	16
chansts_0	0x88	32
chansts_1	0x8c	32
chainaddr_0	0x90	32
chainaddr_1	0x94	32
chancmp_0	0x98	32
chancmp_1	0x9c	32
chanerr	0xa8	32
chanerrmsk	0xac	32
dcactrl	0xb0	32
dca_ver	0x100	8
dca_reqid_offset	0x102	16
csi_capability	0x108	16
pcie_capability	0x10a	16
csi_cap_enable	0x10c	16
pcie_cap_enable	0x10e	16
apicid_tag_map	0x110	64
dca_reqid0	0x180	32
dca_reqid1	0x184	32
msgaddr	0x2000	32

Register Name	Offset	Size
msgupaddr	0x2004	32
msgdata	0x2008	32
vecctrl	0x200c	32
pendingbits	0x3000	32

6.2.1 chancnt

Channel Count

The Channel Count register specifies the number of channels that are implemented.

Type: MEM	**PortID:** 8'h7e	
Bus: 0	**Device:** 4	**Function:** 0-7
Offset: 0x0		

Bit	Attr	Default	Description
4:0	RO	0x1	num_chan: Number of channels. Specifies the number of DMA channels. The IIO supports 1 DMA Channel per function so this register will always read 1.

6.2.2 xfercap

Transfer Capacity

The Transfer Capacity specifies the minimum of the maximum DMA transfer size supported on all channels.

Type: MEM	**PortID:** 8'h7e	
Bus: 0	**Device:** 4	**Function:** 0-7
Offset: 0x1		

Bit	Attr	Default	Description
4:0	RO	0x14	trans_size: Transfer size. This field specifies the number of bytes that may be specified in a DMA descriptor's Transfer Size field. This defines the maximum transfer size supported by IIO as a power of 2. CPU will support 1M max.

6.2.3 genctrl

DMA General Control

The DMA Control register provides for general control operations.

Type: MEM	**PortID:** 8'h7e	
Bus: 0	**Device:** 4	**Function:** 0-7
Offset: 0x2		

Bit	Attr	Default	Description
0:0	RW	0x0	dbgen: Debug Enable

6.2.4 intrctrl

The Interrupt Control register provides for control of DMA interrupts.

Type: MEM **Bus:** 0 **Offset:** 0x3			**PortID:** 8'h7e **Device:** 4 **Function:** 0-7
Bit	**Attr**	**Default**	**Description**
3:3	RW	0x0	msix_vecctrl: Intel QuickData Technology DMA ignores this bit.
2:2	RO	0x0	intp: Interrupt. This bit is set whenever the channel status bit in the Attention Status register is set and the Master Interrupt Enable bit is set. That is, it is the logical AND of Interrupt Status and Master Interrupt Enable bits of this register. This bit represents the legacy interrupt drive signal (when in legacy interrupt mode). In MSI-X mode, this bit is not used by software and is a don't care.
1:1	RO	0x0	intp_sts: Interrupt Status. This bit is set whenever the bit in the Attention Status register is set. This bit is not used by software in MSI-X mode and is a don't care.
0:0	RW	0x0	mstr_intp_en: Master Interrupt Enable. Setting this bit enables the generation of an interrupt in legacy interrupt mode. This bit is automatically reset each time this register is read. When this bit is clear ed, the IIO will not generate a legacy interrupt under otherwise valid conditions. This bit is not used when DMA is in MSI-X mode.

6.2.5 attnstatus

Attention Status

Type: MEM **Bus:** 0 **Offset:** 0x4			**PortID:** 8'h7e **Device:** 4 **Function:** 0-7
Bit	**Attr**	**Default**	**Description**
0:0	RO_V	0x0	chanattn: Channel Attention. Represents the interrupt status of the channel. This bit clears when read. Writes have no impact on this bit.

6.2.6 cbver

The Intel QuickData Technology version register field indicates the version of the Intel QuickData Technology specification that the IIO implements. The most significant 4-bits (range 7:4) are the major version number and the least significant 4-bits (range 3:0) are the minor version number. The IIO implementation for this Intel QuickData Technology version is 3.2 encoded as 0b0011 0010.

Type: MEM	**PortID:** 8'h7e	
Bus: 0	**Device:** 4	**Function:** 0-7
Offset: 0x8		

Bit	Attr	Default	Description
7:4	RO	0x3	mjrver: Major Version. Specifies Major version of the Intel QuickData Technology implementation. Current value is 2h.
3:0	RO	0x2	mnrver: Minor Version. Specifies Minor version of the Intel QuickData Technology implementation. Current value is 0h.

6.2.7 intrdelay

Interrupt Delay

Type: MEM	**PortID:** 8'h7e	
Bus: 0	**Device:** 4	**Function:** 0-7
Offset: 0xc		

Bit	Attr	Default	Description
15:15	RO	0x1	interrupt_coalescing_supported: The IIO does support interrupt coalescing by delaying interrupt generation.
13:0	RW	0x0	interrupt_delay_time: Specifies the number of microseconds that the IIO delays generation of an interrupt (legacy or MSI or MSI-X) from the time that interrupts are enabled (that is, Master Interrupt Enable bit in the CSIPINTRCTRL register is set or, for MSI-X when Vector Control bit1, when CHANCTRL:Interrupt Disable for that channel is reset).

6.2.8 cs_status

Chipset Status

Type: MEM	**PortID:** 8'h7e	
Bus: 0	**Device:** 4	**Function:** 0-7
Offset: 0xe		

Bit	Attr	Default	Description
3:3	RO	0x0	address_remapping: This bit reflects the TE bit of the non-VC1 Intel® Virtualization Technology (Intel® VT) for Directed I/O (Intel® VT-d) engine.
2:2	RO	0x0	memory_bypass:
1:1	RO	0x0	mmio_restriction:

6.2.9 dmacapability

Type: MEM	PortID: 8'h7e	Function: 0-7
Bus: 0	Device: 4	
Offset: 0x10		

Bit	Attr	Default	Description
9:9	RO_V (Function 0-1) RO (Function 2-7)	0x0	xor_raid6: If set, specifies XOR with Galios Field Multiply Parity and Quotient opcodes for RAID5 and RAID6 are supported. The opcodes are: 0x89 - XOR with Galios Field Multiply Generation 0x8A - XOR with Galios Field Multiply Validate 0x8B - XOR with Galios Field Multiply Update Generation ***Note:*** When this bit is zero, the DMA engine will halt if it encounters a descriptor with these opcodes.
8:8	RO	0x0	xor_raid5: If set, specifies XOR without Galios Field Multiply parity only opcodes for RAID5 are supported. The opcodes are: 0x87 - XOR Generation 0x88 - XOR Validate ***Note:*** When this bit is zero, the DMA engine will halt if it encounters a descriptor with these opcodes.
7:7	RO	0x1	extended_apic_id: Set if 32b APIC IDs are supported. 1: 32b APIC IDs supported 0: 8b APIC IDs supported
6:6	RO	0x1	block_fill: If set, specifies the Block Fill opcode is supported. The opcode is: 0x01 - Block Fill ***Note:*** When this bit is zero, the DMA engine will abort if it encounters a descriptor with these opcodes.
5:5	RO	0x1	move_crc: If set, specifies Move and CRC opcodes are supported. The opcodes are: 0x41 - Move and Generate CRC-32 0x42 - Move and Test CRC-32 0x43 - Move and Store CRC-32 ***Note:*** When this bit is zero, the DMA engine will abort if it encounters a descriptor with these opcodes.
4:4	RW_O	0x1	dca: If set, specifies DMA DCA operations are supported according to the settings in the descriptors. ***Notes:*** When this bit is zero, the DMA engine ignores the DCA hints in DMA descriptors. This bit is RW-O to give bios the ability to turn off DCA operation from Intel QuickData Technology DMA.
3:3	RO	0x0	xor: If set, specifies XOR opcodes are supported. Opcodes are: 0x85 - original XOR Generation 0x86 - original XOR Validate ***Notes:*** These opcodes have been deprecated in Intel QuickData Technology DMA v3. The DMA engine will abort if it encounters a descriptor with these opcodes.

Type: MEM	PortID: 8'h7e	
Bus: 0	Device: 4	Function: 0-7
Offset: 0x10		

Bit	Attr	Default	Description
2:2	RO	0x1	marker_skipping: If set, specifies the Marker Skipping opcode is supported. The opcode is: 0x84 - Marker Skipping ***Note:*** When this bit is zero, the DMA engine will abort if it encounters a descriptor with this opcode.
1:1	RO	0x1	crc: If set, specifies CRC Generation opcodes are supported. Opcodes are: 0x81 - CRC-32 Generation 0x82 - CRC-32 Generation and Test 0x83 - CRC-32 Generation and Store ***Note:*** When this bit is zero, the DMA engine will abort if it encounters a descriptor with these opcodes.
0:0	RO	0x1	page_break: If set, specifies a transfer crossing physical pages is supported. ***Note:*** When this bit is zero, software must not set SPBrk nor DPBrk bits in the DMA descriptor and the DMA engine generates an error if either of those bits are set.

6.2.10 dcaoffset

Type: MEM	PortID: 8'h7e	
Bus: 0	Device: 4	Function: 0-7
Offset: 0x14		

Bit	Attr	Default	Description
15:0	RO	0x100	dcaregptr:

6.2.11 cbprio

Intel QuickData Technology DMA Priority Register

Type: MEM	PortID: 8'h7e	
Bus: 0	Device: 4	Function: 0-7
Offset: 0x40		

Bit	Attr	Default	Description
7:0	RO	0x0	not_used:

6.2.12 chanctrl

The Channel Control register controls the behavior of the DMA channel when specific events occur such as completion or errors.

Type: MEM **Bus:** 0 **Offset:** 0x80			**PortID:** 8'h7e **Device:** 4 **Function:** 0-7
Bit	**Attr**	**Default**	**Description**
9:9	RW_L	0x0	cmpwr_dca_enable: When this bit is set, and the DMA engine supports DCA, then completion writes will be directed to the CPU indicated in Target CPU.This field is RW if CHANCNT register is 1 otherwise this register is RO.
8:8	RW_LV	0x0	in_use: In Use. This bit indicates whether the DMA channel is in use. The first time this bit is read after it has been cleared, it will return 0 and automatically transition from 0 to 1, reserving the channel for the first consumer that reads this register. All subsequent reads will return 1 indicating that the channel is in use. This bit is cleared by writing a 0 value, thus releasing the channel. A consumer uses this mechanism to atomically claim exclusive ownership of the DMA channel. This should be done before attempting to program any register in the DMA channel register set. This field is RW if CHANCNT register is 1 otherwise this register is RO.
5:5	RW_L	0x0	desc_addr_snp_ctrl: Descriptor address snoop control. 1: When set, this bit indicates that the descriptors are not in coherent space and should not be snooped. 0: When cleared, the descriptors are in coherent space and each descriptor address must be snooped on QPI. This field is RW if CHANCNT register is 1 otherwise this register is RO.
4:4	RW_L	0x0	err_int_en: Error Interrupt Enable. This bit enables the DMA channel to generate an interrupt (MSI or legacy) when an error occurs during the DMA transfer. If Any Error Abort Enable (see below) is not set, then unaffiliated errors do not cause an interrupt.This field is RW if CHANCNT register is 1 otherwise this register is RO.
3:3	RW_L	0x0	anyerr_abrt_en: Any Error Abort Enable. This bit enables an abort operation when any error is encountered during the DMA transfer. When the abort occurs, the DMA channel generates an interrupt and a completion update as per the Error Interrupt Enable and Error Completion Enable bits. When this bit is reset, only affiliated errors cause the DMA channel to abort.This field is RW if CHANCNT register is 1 otherwise this register is RO.
2:2	RW_L	0x0	err_cmp_en: Error Completion Enable. This bit enables a completion write to the address specified in the CHANCMP register upon encountering an error during the DMA transfer. If Any Error Abort is not set, then unaffiliated errors do not cause a completion write.This field is RW if CHANCNT register is 1 otherwise this register is RO.
0:0	RW1C	0x0	intp_dis: Interrupt Disable. Upon completing a descriptor, if an interrupt is specified for that descriptor and this bit is reset, then the DMA channel generates an interrupt and sets this bit. The choice between MSI or legacy interrupt mode is determined with the MSICTRL register. Legacy interrupts are further gated through intxDisable in thePCICMD register of the Intel QuickData Technology DMA PCI configuration space. The controlling process can re-enable this channel's interrupt by writing a one to this bit, which clears the bit. Writing a zero has no effect. Thus, each time this bit is reset, it enables the DMA channel to generate one interrupt.

6.2.13 dma_comp

DMA Compatibility Register

Type: MEM			**PortID:** 8'h7e	
Bus: 0			**Device:** 4	**Function:** 0-7
Offset: 0x82				
Bit	**Attr**	**Default**	**Description**	
2:2	RO	0x1	v3_compatibility: Compatible with version 3 Intel QuickData Technology specification	
1:1	RO	0x1	v2_compatibility: Compatible with version 2 Intel QuickData Technology specification	
0:0	RO	0x0	v1_compatibility: Not compatible with version 1	

6.2.14 chancmd

DMA Channel Command Register

Setting more than one of these bits with the same write operation will result in an fatal error affiliated.

Type: MEM			**PortID:** 8'h7e	
Bus: 0			**Device:** 4	**Function:** 0-7
Offset: 0x84				
Bit	**Attr**	**Default**	**Description**	
5:5	RW_LV	0x0	reset_dma: Set this bit to reset the DMA channel. Setting this bit is a last resort to recover the DMA channel from a programming error or other problem such as dead lock from cache coherency protocol. Execution of this command does not generate an interrupt or generate status. This command causes the DMA channel to return to a known state Halted.This field is RW if CHANCNT register is 1 otherwise this register is RO.	
2:2	RW_LV	0x0	susp_dma: Suspend DMA. Set this bit to suspend the current DMA transfer. This field is RW if CHANCNT register is 1 otherwise this register is RO.	

6.2.15 dmacount

DMA Descriptor Count Register

Type: MEM			**PortID:** 8'h7e	
Bus: 0			**Device:** 4	**Function:** 0-7
Offset: 0x86				
Bit	**Attr**	**Default**	**Description**	
15:0	RW_L	0x0	numdesc: This is the absolute value of the number of valid descriptors in the chain. The hardware sets this register and an internal counter to zero whenever the CHAINADDR register is written. When this register does not equal the value of the internal register, the DMA channel processes descriptors, incrementing the internal counter each time that it completes (or skips) a descriptor. This register is RW if CHANCNT register is 1 otherwise this register is RO.	

6.2.16 chansts_0

Channel Status 0 Register

The Channel Status Register records the address of the last descriptor completed by the DMA channel.

Type: MEM **Bus:** 0 **Offset:** 0x88			**PortID:** 8'h7e **Device:** 4 **Function:** 0-7
Bit	**Attr**	**Default**	**Description**
31:6	RO	0x0	cmpdscaddr: This register stores the upper address bits (64B aligned) of the last descriptor processed. The DMA channel automatically updates this register when an error or successful completion occurs. For each completion, the DMA channel over-writes the previous value regardless of whether that value has been read.
2:0	RO	0x3	dma_trans_state: DMA Transfer Status. The DMA engine sets these bits indicating the state of the current DMA transfer. The cause of an abort can be either error during the DMA transfer or invoked by the controlling process via the CHANCMD register. 000 - Active 001 - Idle, DMA Transfer Done (no hard errors) 010 - Suspended 011 - Halted, operation aborted 100 - Armed

6.2.17 chansts_1

Channel Status 1 Register

The Channel Status Register records the address of the last descriptor completed by the DMA channel.

Type: MEM **Bus:** 0 **Offset:** 0x8c			**PortID:** 8'h7e **Device:** 4 **Function:** 0-7
Bit	**Attr**	**Default**	**Description**
31:0	RO	0x0	cmpdscaddr: This register stores the upper address bits (64B aligned) of the last descriptor processed. The DMA channel automatically updates this register when an error or successful completion occurs. For each completion, the DMA channel over-writes the previous value regardless of whether that value has been read.

6.2.18 chainaddr_0

Descriptor Chain Address 0 Register

This register is written by the processor to specify the first descriptor to be fetched by the DMA channel.

Type: MEM **Bus:** 0 **Offset:** 0x90			**PortID:** 8'h7e **Device:** 4 **Function:** 0-7
Bit	**Attr**	**Default**	**Description**
31:0	RW_L	0x0	dscaddrlo: This 64 bit field marks the address of the first descriptor to be fetched by the DMA channel. The least significant 6 bits must be zero for the address to be valid. This register is RW if CHANCNT register is 1 otherwise this register is RO.

6.2.19 chainaddr_1

Descriptor Chain Address 1 Register

This register is written by the processor to specify the first descriptor to be fetched by the DMA channel.

Type: MEM **Bus:** 0 **Offset:** 0x94			**PortID:** 8'h7e **Device:** 4 **Function:** 0-7
Bit	**Attr**	**Default**	**Description**
31:0	RW_L	0x0	dscaddrhi: This 64 bit field marks the address of the first descriptor to be fetched by the DMA channel. The least significant 6 bits must be zero for the address to be valid. This register is RW if CHANCNT register is 1 otherwise this register is RO.

6.2.20 chancmp_0

Channel Completion Address 0 Register

This register specifies the address where the DMA channel writes the completion status upon completion or an error condition i.e., it writes the contents of the CHANSTS register to the destination as pointed by the CHANCMP register.

Type: MEM **Bus:** 0 **Offset:** 0x98			**PortID:** 8'h7e **Device:** 4 **Function:** 0-7
Bit	**Attr**	**Default**	**Description**
31:3	RW_L	0x0	chcmpladdr_lo: This 64-bit field specifies the address where the DMA engine writes the completion status (CHANSTS). This address can fall within system memory or memory-mapped I/O space but should be 8-byte aligned.This register is RW if CHANCNT register is 1 otherwise this register is RO.

6.2.21 chancmp_1

Channel Completion Address 1 Register

This register specifies the address where the DMA channel writes the completion status upon completion or an error condition i.e., it writes the contents of the CHANSTS register to the destination as pointed by the CHANCMP register.

Type: MEM **Bus:** 0 **Offset:** 0x9c			**PortID:** 8'h7e **Device:** 4 **Function:** 0-7
Bit	**Attr**	**Default**	**Description**
31:0	RW_L	0x0	chcmpladdr_hi: This 64-bit field specifies the address where the DMA engine writes the completion status (CHANSTS). This address can fall within system memory or memory-mapped I/O space but should be 8-byte aligned.This register is RW if CHANCNT register is 1 otherwise this register is RO.

6.2.22 chanerr

The Channel Error Register records the error conditions occurring within a given DMA channel.

Type: MEM **Bus:** 0 **Offset:** 0xa8			**PortID:** 8'h7e **Device:** 4 **Function:** 0-7
Bit	**Attr**	**Default**	**Description**
18:18	RW1CS (Function 0-1) RO (Function 2-7)	0x0	desccnterr: The hardware sets this bit when it encounters a base descriptor that requires an extended descriptor (such as an XOR with 8 sources), but DMACount indicates that the Base descriptor is the last descriptor that can be processed.
17:17	RW1CS (Function 0-1) RO (Function 2-7)	0x0	xorqerr: The hardware sets this bit when the Q validation part of the XOR with Galois Field Multiply Validate operation fails.
16:16	RW1CS	0x0	crc_xorp_err: The hardware sets this bit when a CRC Test operation or XOR Validity operation fails or when the P validation part of the XOR with Galois Field Multiply Validate operation fails.
15:15	RO	0x0	unaffil_err: Unaffiliated Error. IIO never sets this bit.
13:13	RW1CS	0x0	int_cfg_err: Interrupt Configuration Error. The DMA channel sets this bit indicating that the interrupt registers were not configured properly when the DMA channel attempted to generate an interrupt. For example, interrupt address is not 0xFEE.
12:12	RW1CS	0x0	cmp_addr_err: Completion Address Error. The DMA channel sets this bit indicating that the completion address register was configured to an illegal address or has not been configured.
11:11	RW1CS	0x0	desc_len_err: Descriptor Length Error. The DMA channel sets this bit indicating that the current transfer has an illegal length field value. When this bit has been set, the address of the failed descriptor is in the Channel Status register.

Type: MEM	PortID: 8'h7e		
Bus: 0	Device: 4	Function: 0-7	
Offset: 0xa8			
Bit	**Attr**	**Default**	**Description**
10:10	RW1CS	0x0	desc_ctrl_err: Descriptor Control Error. The DMA channel sets this bit indicating that the current transfer has an illegal control field value. When this bit has been set, the address of the failed descriptor is in the Channel Status register.
9:9	RW1CS	0x0	wr_data_err: Write Data Error. The DMA channel sets this bit indicating that the current transfer has encountered an error while writing the destination data. This error could be because of an internal ram error in the write queue that stores the write data before being written to main memory. When this bit has been set, the address of the failed descriptor is in the Channel Status register.
8:8	RW1CS	0x0	rd_data_err: Read Data Error. The DMA channel sets this bit indicating that the current transfer has encountered an error while accessing the source data. This error could be a read data that is received poisoned. When this bit has been set, the address of the failed descriptor is in the Channel Status register.
7:7	RW1CS	0x0	dma_data_parerr: DMA Data Parity Error. The DMA channel sets this bit indicating that the current transfer has encountered an uncorrectable ECC/parity error reported by the DMA engine.
6:6	RW1CS	0x0	cdata_parerr: Chipset Data Parity Error. The DMA channel sets this bit indicating that the current transfer has encountered a parity error reported by the chipset. When this bit has been set, the address of the failed descriptor is in the Channel Status register.
5:5	RW1CS	0x0	chancmd_err: CHANCMD Error. The DMA channel sets this bit indicating that a write to the CHANCMD register contained an invalid value (for example. more than one command bit set).
4:4	RW1CS	0x0	chn_addr_valerr: Chain Address Value Error. The DMA channel sets this bit indicating that the CHAINADDR register has an illegal address including an alignment error (not on a 64-byte boundary).
3:3	RW1CS	0x0	descriptor_error: The DMA channel sets this bit indicating that the current transfer has encountered an error (not otherwise covered under other error bits) when reading or executing a DMA descriptor. When this bit has been set and the channel returns to the Halted state, the address of the failed descriptor is in the Channel Status register.

Type: MEM Bus: 0 Offset: 0xa8		PortID: 8'h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
2:2	RW1CS	0x0	nxt_desc_addr_err: Next Descriptor Address Error. The DMA channel sets this bit indicating that the current descriptor has an illegal next descriptor address including an alignment error (not on a 64-byte boundary). When this bit has been set and the channel returns to the Halted state, the address of the failed descriptor is in the Channel Status register.
1:1	RW1CS	0x0	dma_xfrer_daddr_err: DMA Transfer Destination Address Error. The DMA channel sets this bit indicating that the current descriptor has an illegal destination address. When this bit has been set, the address of the failure descriptor has been stored in the Channel Status register.
0:0	RW1CS	0x0	dma_trans_saddr_err: DMA Transfer Source Address Error. The DMA channel sets this bit indicating that the current descriptor has an illegal source address. When this bit has been set, the address of the failure descriptor has been stored in the Channel Status register.

6.2.23 chanerrmsk

Channel Error Mask Register

Type: MEM Bus: 0 Offset: 0xac		PortID: 8'h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**
18:18	RWS (Function 0-1) RO (Function 2-7)	0x0	mask18: This register is a bit for bit mask for the CHANERR register. 0: Enable 1: Disable
17:17	RWS (Function 0-1) RO (Function 2-7)	0x0	mask17: This register is a bit for bit mask for the CHANERR register. 0: Enable 1: Disable
16:16	RWS	0x0	mask16: This register is a bit for bit mask for the CHANERR register. 0: Enable 1: Disable
13:0	RWS	0x0	mask13_0: This register is a bit for bit mask for the CHANERR register. 0: Enable 1: Disable

6.2.24 dcactrl

DCA Control

Type: MEM Bus: 0 Offset: 0xb0			PortID: 8'h7e Device: 4 Function: 0-7
Bit	**Attr**	**Default**	**Description**
15:0	RW_L	0x0	target_cpu: Specifies the APIC ID of the target CPU for Completion Writes. This field is RW if CHANCNT register is 1 otherwise this register is RO.

6.2.25 dca_ver

DCA Version Number Register

Type: MEM Bus: 0 Offset: 0x100			PortID: 8'h7e Device: 4 Function: 0-7
Bit	**Attr**	**Default**	**Description**
7:4	RO	0x1	major_revision:
3:0	RO	0x0	minor_revision:

6.2.26 dca_reqid_offset

DCA Requester ID Offset

Type: MEM Bus: 0 Offset: 0x102			PortID: 8'h7e Device: 4 Function: 0-7
Bit	**Attr**	**Default**	**Description**
15:0	RO	0x180	dca_reqid_regs: Registers are at offset 180h.

6.2.27 csi_capability

Intel QPI Compatibility Register

Type: MEM Bus: 0 Offset: 0x108			PortID: 8'h7e Device: 4 Function: 0-7
Bit	**Attr**	**Default**	**Description**
0:0	RO	0x1	prefetch_hint: IIO supports Prefetch Hint only method on the coherent interface.

6.2.28 pcie_capability

PCI Express Capability Register

Type: MEM Bus: 0 Offset: 0x10a			PortID: 8'h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**	
0:0	RO	0x1	memwr: IIO supports only memory write method on PCI Express.	

6.2.29 csi_cap_enable

Intel QPI Capability Enable Register

Type: MEM Bus: 0 Offset: 0x10c			PortID: 8'h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**	
0:0	RW	0x0	enable_prefetch_hint: When set in function 0, DCA on Intel® QuickPath Interconnect (Intel® QPI) is enabled, else disabled. IIO hardware does not use this bit from functions 1-7. In these functions, this bit is provided primarily for BIOS to communicate to driver that DCA is enabled in the IIO.	

6.2.30 pcie_cap_enable

PCI Express Capability Enable Register

Type: MEM Bus: 0 Offset: 0x10e			PortID: 8'h7e Device: 4	Function: 0-7
Bit	**Attr**	**Default**	**Description**	
0:0	RW	0x0	enable_memwr_on_pcie: When set in function 0, DCA on PCIe is enabled, else disabled. IIO hardware does not use this bit from functions 1-7. In these functions, this bit is provided primarily for BIOS to communicate to driver that DCA is enabled in the IIO.	

6.2.31 apicid_tag_map

APICID to Tag Map Register

When DCA is disabled, DMA engine uses all 1s in the tag field of the write.

This register is setup by the BIOS for the Intel QuickData Technology driver to read. The BIOS will map APICID[7:5] to bits Tag[2:0]. The BIOS should set Tag[4] to prevent implicit TPH cache target unless it is intended.

Type: MEM	**PortID:** 8'h7e	
Bus: 0	**Device:** 4	**Function:** 0-7
Offset: 0x110		

Bit	Attr	Default	Description
39:32	RW	0x80	tag_map_4: This field is used by the Intel QuickData Technology DMA engine to populate Tag field bit 4 of the memory write transaction it issues with either 1, 0, or a selected APICID bit. [7:6] 00: Tag[4] = Tag_Map_4[0] 01: Tag[4] = APICID[Tag_Map_4[3:0]] 10: Tag[4] = NOT(APICID [Tag_Map_4[3:0]]) 11: reserved
31:24	RW	0x80	tag_map_3: This field is used by the Intel QuickData Technology DMA engine to populate Tag field bit 3 of the memory write transaction it issues with either 1, 0, or a selected APICID bit. [7:6] 00: Tag[3] = Tag_Map_3[0] 01: Tag[3] = APICID[Tag_Map_3[3:0]] 10: Tag[3] = NOT(APICID[Tag_Map_3[3:0]]) 11: reserved
23:16	RW	0x80	tag_map_2: This field is used by the Intel QuickData Technology DMA engine to populate Tag field bit 2 of the memory write transaction it issues with either 1, 0, or a selected APICID bit. [7:6] 00: Tag[2] = Tag_Map_2[0] 01: Tag[2] = APICID[Tag_Map_2[3:0]] 10: Tag[2] = NOT(APICID[Tag_Map_2[3:0]]) 11: reserved
15:8	RW	0x80	tag_map_1: This field is used by the Intel QuickData Technology DMA engine to populate Tag field bit 1 of the memory write transaction it issues with either 1, 0, or a selected APICID bit. [7:6] 00: Tag[1] = Tag_Map_1[0] 01: Tag[1] = APICID[Tag_Map_1[3:0]] 10: Tag[1] = NOT(APICID[Tag_Map_1[3:0]]) 11: reserved
7:0	RW	0x80	tag_map_0: This field is used by the Intel QuickData Technology DMA engine to populate Tag field bit 0 of the memory write transaction it issues with either 1, 0, or a selected APICID bit. [7:6] 00: Tag[0] = Tag_Map_0[0] 01: Tag[0] = APICID[Tag_Map_0[3:0]] 10: Tag[0] = NOT (APICID[Tag_Map_0[3:0]]) 11: reserved

6.2.32 dca_reqid[0:1]

Global DCA Requester ID Table Registers

Type: MEM			PortID: 8'h7e	
Bus: 0			Device: 4	Function: 0-7
Offset: 0x180, 0x184				
Bit	**Attr**	**Default**	**Description**	
31:31	RO	0x0	last: This bit is set only in the last RequesterID register for this port. Thus, it identifies that this is the last DCA RequesterID register for this port.	
29:29	RW	0x0	valid: when set the requester id programed into bits [15:0] is used by hardware for DCA write identification, otherwise the bits are ignored.	
28:28	RW	0x0	ignore_function_number: When set, the function number field in the RequesterID is ignored when authenticating a DCA write, otherwise the function number is included.	
15:8	RW	0x0	bus_number: PCI bus number of the DCA requester	
7:3	RW	0x0	device_number: Device number of the day requester	
2:0	RW	0x0	function_number: Function number of the day requester	

6.2.33 msgaddr

MSI-X Lower Address Registers

Type: MEM			PortID: 8'h7e	
Bus: 0			Device: 4	Function: 0-7
Offset: 0x2000				
Bit	**Attr**	**Default**	**Description**	
31:2	RW_V	0x0	chmsgaddr: Specifies the local APIC to which this MSI-X interrupt needs to be sent.	
1:0	RO	0x0	chmsgaddr_const:	

6.2.34 msgupaddr

MSI-X Upper Address Registers

Type: MEM			PortID: 8'h7e	
Bus: 0			Device: 4	Function: 0-7
Offset: 0x2004				
Bit	**Attr**	**Default**	**Description**	
31:0	RW_V	0x0	chmsgupaddr_const: Reserved to 0 because does not apply to IA. This field is RW for compatibility reason only.	

6.2.35 msgdata

MSI-X Data Registers

Type: MEM	PortID: 8'h7e	Function: 0-7
Bus: 0	Device: 4	
Offset: 0x2008		

Bit	Attr	Default	Description
31:0	RW_V	0x0	chmsgdata: Specifies the vector that needs to be used for interrupts from the DMA engine. IIO uses the lower 16 bits of this field to form the data portion of the interrupt on the coherent interface. The upper 16 bits are not used by IIO and left as RW only for compatibility reasons.

6.2.36 vecctrl

MSI-X Vector Control Registers

Type: MEM	PortID: 8'h7e	Function: 0-7
Bus: 0	Device: 4	
Offset: 0x200c		

Bit	Attr	Default	Description
31:1	RO	0x0	chvecctrlcnst:
0:0	RW_V	0x1	chmask: When a bit is set, the channel is prohibited from sending a message, even if all other internal conditions for interrupt generation are valid.

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