Product Brief

Broadband Network Gateway (BNG) | Disaggregated Networks

Intel® Broadband Network Gateway Acceleration Kit (Intel® BNG Acceleration Kit)

The Intel® Broadband Network Gateway Acceleration Kit (Intel® BNG Acceleration Kit) provides key building blocks to speed up development of BNG solutions using Intel® Tofino™ Expandable Architecture for faster time to market, scalability and lower cost of ownership

With the rapid growth of internet subscribers and connected devices, cloud service providers and communication service providers find it difficult to meet today's capacity needs for 4k video streaming, work-from-home teleconferencing, IoT (e.g., smart home appliance) propagation and artificial intelligence/machine learning (AI/ML).

The Intel® BNG Acceleration Kit makes it easier for network equipment manufacturers to quickly develop BNG solutions such as OpenBNG. The BNG Acceleration Kit is available for the Intel® Tofino™ Expandable Architecture, which provides massive performance, programmability, intelligence and visibility/control.

The BNG Acceleration Kit takes advantage of the P4 programmability of Intel Tofino Expandable Architecture, enabling vendors to customize and optimize their BNG solutions for customers' unique deployment needs.

This acceleration kit includes the necessary reference implementations to build a fully featured OpenBNG solution using foundational libraries.

OpenBNG solutions that are created using the BNG Acceleration Kit benefit from the power of Intel® Xeon® Scalable processors and the acceleration capabilities of Intel® FPGAs and/or Intel® Infrastructure Processing Units (Intel® IPUs) to extend and augment Intel® Tofino™ Intelligent Fabric Processor (Intel® Tofino™ IFP) functionality (see Figure 1). This hardware acceleration increases the efficiency of the CPU, eliminating heavy networking constraints by partially or completely delegating resource-consuming network functions to the Intel IFP and Intel FPGA, resulting in very low latency. This enables manufacturers to bring new solutions to market quickly and meet their customers' rapidly increasing capacity and flexibility requirements, while reducing development time as well as OpEx and CapEx.

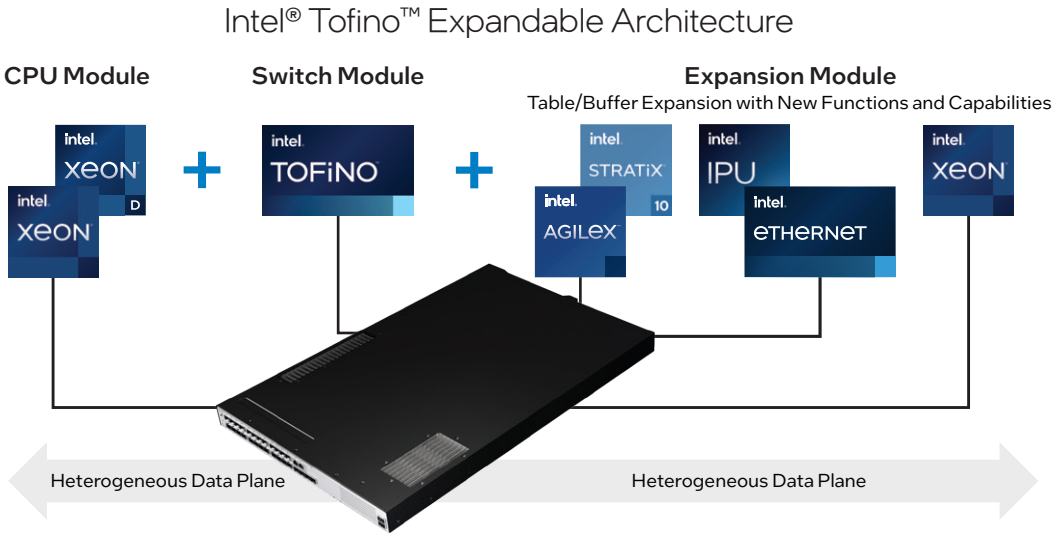

Figure 1. Intel® Tofino™ Expandable Architecture combines Intel® Xeon® CPUs, Intel® Tofino™ IFPs, and Intel® FPGAs/IPUs into a single system.

Features

The Intel® BNG Acceleration Kit, which leverages the Intel® Tofino™ Expandable Architecture, includes:

- **Hardened, yet customizable L2/L3 switching and routing:** The BNG Acceleration Kit includes customizable L2/L3 switching and routing functionality based on a hardened Switch.p4 profile that is secure, reliable and switch abstraction interface (SAI)-controllable.
- **Increased capacity:** Intel Tofino Expandable Architecture achieves two orders of magnitude greater table and buffer capacity[1] compared to a stand-alone data center-focused switch application-specific integrated circuit (ASIC) and supports network transformation through the ability to add new types of network functions.
- **Multiple-pipe programmable packet processing:** Intel Tofino IFP provides multiple pipes, with multiple stages per pipe. It is possible to run the BNG program in some pipes and run counter pool programs on other pipes, as well as focus the programs in each pipe on a specific aspect of the BNG pipeline.
- **BNG-specific functionality:** The reference implementation included in the BNG Acceleration Kit processes the Internet Protocol over Ethernet (IPoE) packets. This functionality is isolated in a separate pipe of the Intel Tofino IFP, allowing for independent development without interfering with the switch profile. Software vendors can focus on developing new features such as Point-to-Point Protocol over Ethernet (PPPoE) while relying on the rest of the user plane to remain unchanged.
- **Software programmability:** The BNG Acceleration Kit offers easy customization to address evolving requirements and deployment scenarios, providing the flexibility to change and grow with customer needs.
- **Time to market:** The BNG Acceleration Kit includes pre-integrated user plane functionality and features for quick development and deployment of new solutions.
- **Open source:** Support for standard and open-source technologies reduces the barriers for use, while increasing flexibility and scalability.
- **Hardware and software disaggregation:** The BNG Acceleration Kit supports multiple hardware platforms from original device manufacturers with the possibility to mix and match solutions from different vendors to meet customers' unique requirements.

Functionality

Overall, a BNG's tasks include packet classification, session termination and collecting statistics for accounting. Once traffic classification occurs, the Intel Tofino IFP marks the packets with additional metadata that tells the Intel FPGA how to treat that traffic. The FPGA extracts that metadata and enqueues the packets accordingly, then the packets are stored in high bandwidth memory (HBM) while they await dequeuing. The scheduling and shaping algorithm propagates the packets through the scheduling hierarchy and, when appropriate, releases the packets back to the Intel Tofino IFP for routing to the rest of the network towards their destinations. The Intel® BNG Acceleration Kit includes four reference implementations that perform all the necessary packet management functions in the BNG (see Figure 2):

- **CPU control plane:** CPU software manages how the user plane operates. It sets up customer sessions, collects statistics from the user plane and handles authentication, authorization and other control functions.
- **BNG.p4:** This handles user plane traffic by performing per-packet operations like classification, session processing, statistics updates, packet updates and rewrites, etc.
- **Switch.p4:** This profile contains L2/L3 switching and routing logic that handles packet forwarding to the correct destinations.
- **FPGA HQoS:** A hierarchical quality of service (HQoS) functionality that is configured and controlled through a standardized Data Plane Development Kit (DPDK)-based API.

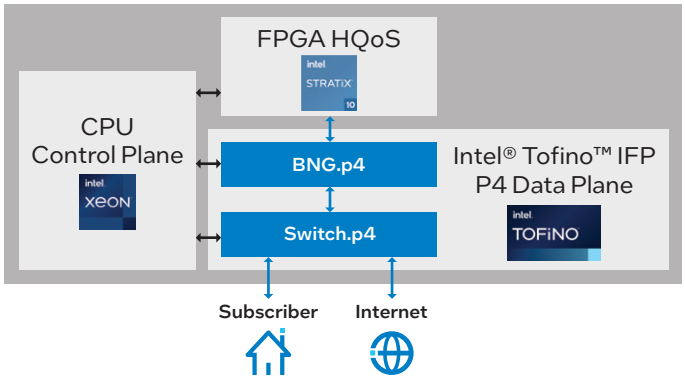

Figure 2. Example functionality of a BNG solution created with the Intel® BNG Acceleration Kit using Intel® Tofino™ Expandable Architecture.

Table 1. Features and Capabilities of the Intel® BNG Acceleration Kit for Intel® Tofino™ Expandable Architecture

Feature	Benefits
Software	▪ Switch abstraction interface (SAI)-compatible for easy integration with SONiC OS and other network operating systems ▪ Standardized APIs for controlling BNG-specific switch functions ▪ Data Plane Development Kit (DPDK)-based API for controlling HQoS functionality
P4 Data Plane	▪ Hardened L2/3 switching and routing functionality ▪ Isolated BNG functionality with reference implementation of IPoE support ▪ Integration with FPGA-based HQoS implementation
Configurable FPGA-based HQoS with HBM2	▪ Scalable per 100 GbE instances ▪ Each 100 GbE instance supports 32,000 queues ▪ 3–7 scheduling layers, with a default configuration of 5 layers ▪ 8 GB or 16 GB of HBM2 memory for traffic buffering, depending on the specific Intel® FPGA ▪ QDR-IV, eSRAM memory for queue management tables ▪ Congestion control ▪ Fine shaping granularity, supporting a combination of low-bandwidth services (e.g., voice) and high-bandwidth broadband services

Learn More

You may find the following resources helpful:

- OpenBNG Solutions from Intel white paper
- OpenBNG webinar
- P4 open source programming language
- SONiC OS
- Vodafone and partners in world first multi-vendor test of new broadband standard press release

Intel Technologies

- Intel® Tofino™ Expandable Architecture
- Intel® Tofino™ IFPs
- Intel® Xeon® Scalable processors
- Intel® FPGAs
- Intel® Silicon Photonics

For more information, contact your Intel representative and visit **intel.com/fabric**.

[1] Intel® Stratix® 10 MX FPGA comes with 8 GBytes or 16 GBytes of HBM2 memory https://cdrdv2.intel.com/v1/dl/getContent/652451 offering 50-100x more memory capacity. A typical data center-focused switch offers hundreds of Mbits of table memory intel.com/content/dam/www/central-libraries/us/en/documents/tofino-product-family-brochure.pdf and hundreds of Mbytes of buffer capacity linleygroup.com/mpr/article.php?id=12304.