BeMicro CV
FPGA Development Board
Hardware Reference Guide

Altera's 28nm Low Cost FPGA Solution

Table of Contents

1. Overview

This document describes the hardware features of the BeMicro CV Cyclone V E FPGA Development Board, including component reference and detailed pin-out information.

General Description

The BeMicro CV Cyclone V E FPGA Development Board features an Altera 28-nm Cyclone V FPGA in the familiar BeMicro form factor.   The Altera 5CEFA2F23C8N Cyclone V FPGA resident on the Be Micro CV features a hardened memory controller (HMC) that supports DDR2, DDR3 and LPDDR3.   On the BeMicro CV the HMC is connected to a single 16-bit wide, 1Gb DDR3 SDRAM device.

The BeMicro CV board also features expansion connectors and sockets.   For a list of products compatible with BeMicro CV board, see the BeMicro CV Partner Pack at http://parts.arrow.com/item/detail/arrow-development-tools/bemicrocv

Board Component Blocks

The BeMicro CV board features the following major component blocks:

- One Cyclone V E FPGA (5CEFA2F23C8N) in a 484-pin FineLine BGA (FPGA)
  - 25,000 LEs
  - 9,434 adaptive logic modules (ALMs)
  - 1,760 Kbit (Kb) M10K and 196 Kb MLAB memory
  - 4 fractional phase locked loops (PLLs)
  - 50 18x18-bit multipliers
  - 1 Hard Memory Controller
  - 224 general purpose input/output (GPIO)
  - 1.1-V core voltage
- FPGA configuration circuitry
  - Active Serial (AS) x1 configuration (EPCS16I8N)
  - Embedded USB-Blaster™ II for use with the Quartus® II Programmer
  - Separate JTAG configuration header
- Clocking circuitry
  - 50 MHz 1.8V oscillator
  - 24 MHz 2.5V oscillator
- Memory

- 1Gbit DDR3 SDRAM (x16)
- 1K (128 x 8) Two-wire Serial EEPROM
- Micro SD card slot
- General user input / output
  - 8 user LEDs
  - 2 User Pushbuttons
  - 3 User DIP switches
- Prototyping
  - 2 Terasic 40 pin prototyping headers
  - BeMicro SDK 80-pin card edge connector
  - Micro SD card slot
- Power via USB or via user-provided 5V supply

Development Board Block Diagram

Figure 1-1 shows a block diagram of the BeMicro CV FPGA development board.
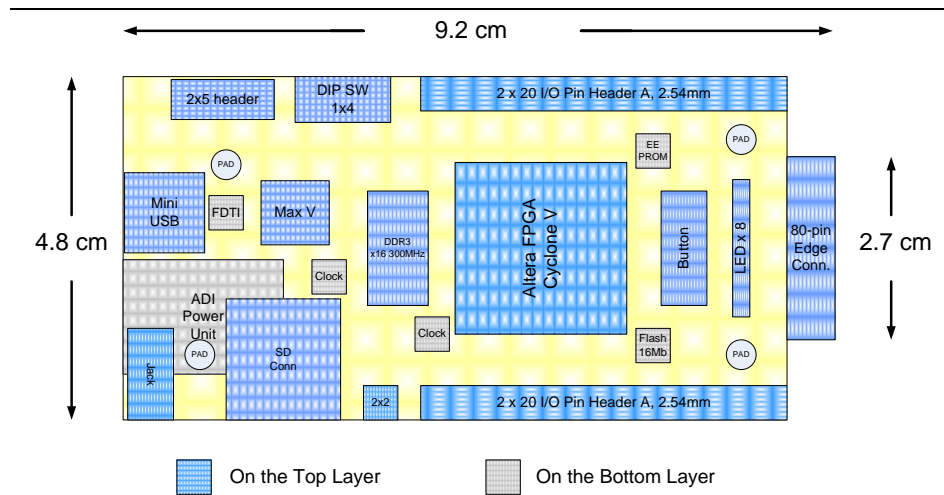

Figure 1-1: BeMicro CV Block Diagram

Figure 1-2 shows a top view of the BeMicro CV FPGA development board.
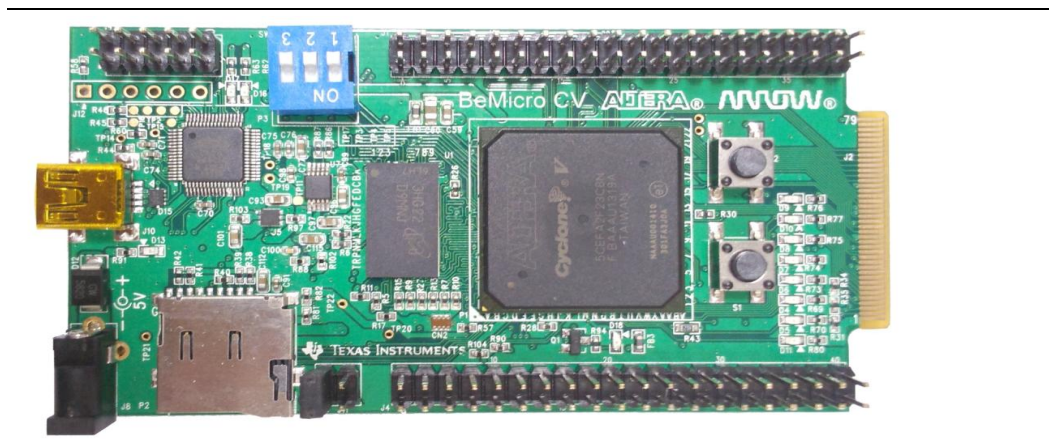

Figure 1-2: Top View of BeMicro CV Development Board.

Figure 1-3 shows a bottom view of the BeMicro CV FPGA development board.
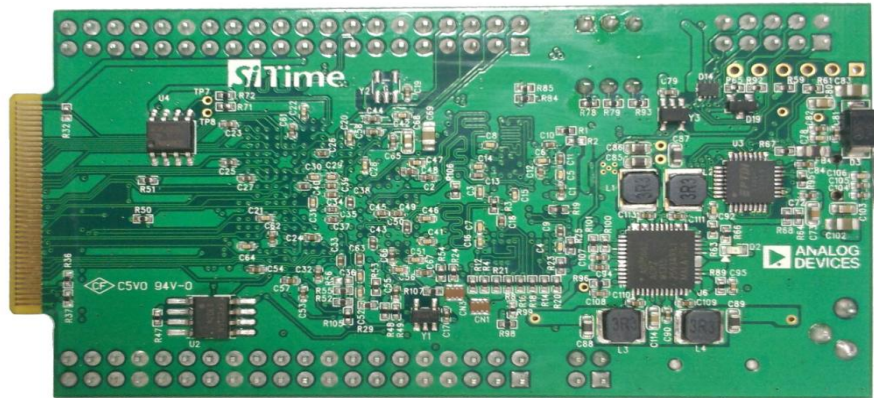
Figure 1-3: Bottom View Be Micro CV Development Board

Handling the Board

When handling the board, it is important to observe the following static discharge precaution:

Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

2. Board Components

This chapter introduces the major components on the Be Micro CV FPGA development board. Figure 2-1 and Figure 2-2 illustrate the component locations.
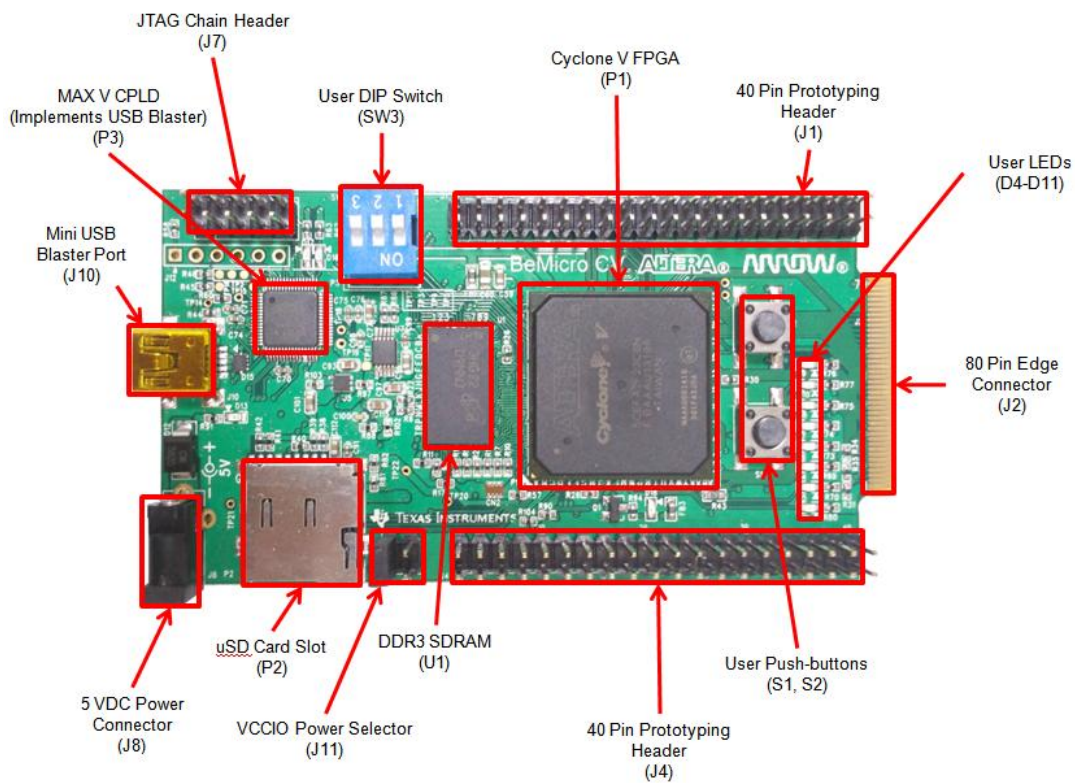
Figure 2-1: Major component locations, Top View

Figure 2-2: Major component locations, Bottom View

This chapter includes the following sections:

- Cyclone V E FPGA
- Configuration Options
- Clock Circuitry
- General User Input / Output
- DDR3 Memory
- EEPROM
- 40 Pin Prototyping Headers
- 80 Pin Edge Connector
- Power Supply

Cyclone V E FPGA

The BeMicro CV E FPGA development board features a Cyclone V E FPGA
5CEFA2F23C8N device (P1) in a 484-pin FBGA package.

Table 2–1 describes the features of the Cyclone V E FPGA 5CEFA2F23C8N device.

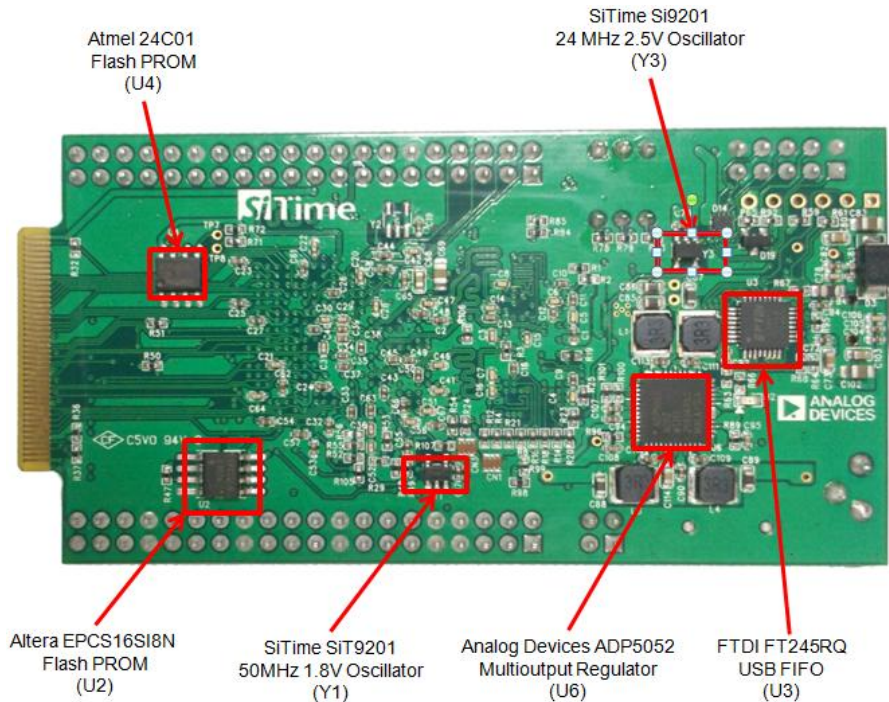| ALMs	Equivalent LE's	M10K RAM (Kbits)	MLAB RAM (Kbits)	18-bit x 18-bit Multipliers	PLLs	Package Type
9,434	25K	1,760	196	50	4	484 pin

Table 2-1: Features of the Cyclone V E 5CEFA2F23C8N

Configuration Options

The Cyclone V E FPGA development board supports the following configuration methods:

- Embedded USB-Blaster is the default method for configuring the FPGA using the Quartus II Programmer in JTAG mode with the supplied USB cable.
- Active Serial Configuration via the on-board EPCS16SI8N configuration device.

FPGA Programming over Embedded USB-Blaster II

This configuration method combines a USB type-B connector (J10), a USB 2.0 PHY device (U3), and an Altera MAX V 5M80ZE64 CPLD (U3) to allow FPGA configuration using a USB cable. This USB cable connects directly between the USB type-B connector on the board and a USB port on a PC running the Quartus II software. The embedded USB-Blaster in the MAX V EPM80ZE64 CPLD normally masters the JTAG chain.

FPGA Programming using EPC Configuration PROM

The low-cost EPC16SI8N non-volatile configuration PROM features a simple six-pin interface and a small form factor. The PROM supports the AS x1 configuration mode. By default, the BeMicro CV E board is set up to configure via AS x 1 configuration mode.   Resistors R55 and R56 allow selection between AS Fast and AS Standard modes.

Figure 2–3 shows the connection between the EPC configuration device and the Cyclone V E FPGA.
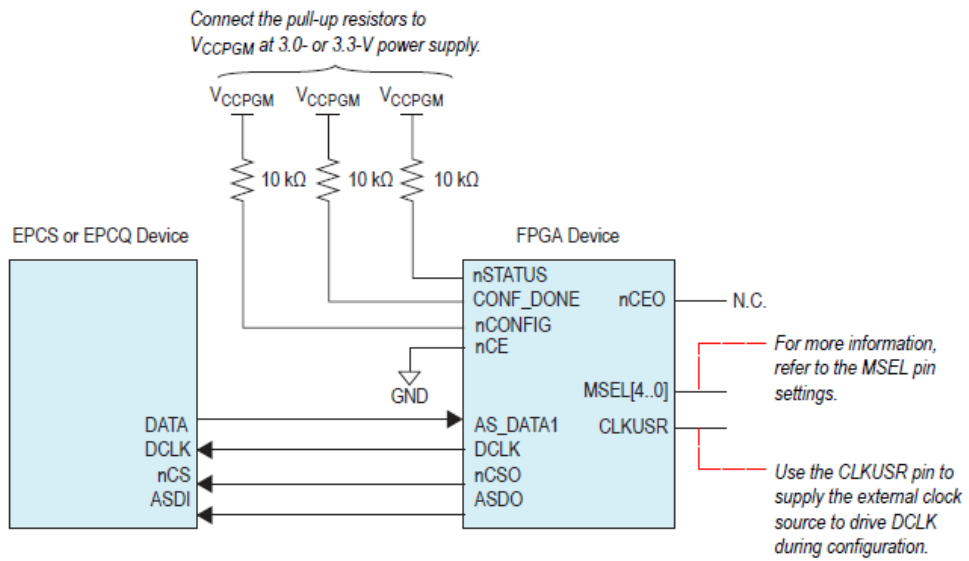
Figure 2-3: Active Serial Configuration Interface

Clock Circuitry

The development board includes oscillators with a frequency of 50-MHz, 100-MHz, and a programmable oscillator

Table 2–2 lists the oscillators, its I/O standard, and voltages required for the development board.

Board Reference	Schematic Signal Name	Frequency	I/O Standard	FPGA Pin Number	Application
Y1	DDR3_CLK_50MHz	50 MHz	1.8V	H13	DDR3 HMC Clock Input
Y2	CLK_50MHz (unpopulated)	50 MHz	2.5V	V16	General Purpose Clock Input
Y3	CLK_24MHz	24 MHz	2.5V	M9	General Purpose Clock Input, also used by on-board USB Blaster II

Table 2-2: BeMico CV On-board oscillators

General User Input / Output

The development board includes switches for user input and LEDs for status output. This section describes these elements.

LED Outputs

Only LED's D4-D11 are available for customer use.   Writing a 0 LED's FPGA output pin will illuminate the LED.   Writing a 1 turns it off.

Table 2–3 lists the LED board references, schematic signal names, and functional descriptions.

Board Reference	Schematic Signal Name	FPGA Pin Number	I/O Standard	Functional Description
D2	NA		NA	ADP5052 Power Good
D4	LED0	U1	3.3-V	Green User LEDs
D5	LED1	N2	3.3-V	Green User LEDs
D6	LED2	U2	3.3-V	Green User LEDs

D7	LED3	W2	3.3-V	Green User LEDs
D8	LED4	AA1	3.3-V	Green User LEDs
D9	LED5	Y3	3.3-V	Green User LEDs
D10	LED6	AA2	3.3-V	Green User LEDs
D11	LED7	N1	3.3-V	Green User LEDs
D13	NA		NA	5V Power Good
D16, D17	NA		NA	Green USB Blaster Status
D18	CONF_DONE		2.5-V	CONF_DONE

Table 2-3: LED Board Reference Information

User-Defined Push Buttons

Board references S1 and S2 are available for user-defined discrete input. When you press and hold down the switch, the device pin is set to logic 0; when you release the switch, the device pin is set to logic 1. There are no board-specific functions for these general user push buttons.

Table 2–4 lists the user-defined push button schematic signal names and their corresponding Cyclone V E FPGA pin numbers.

Board Reference	Schematic Signal Name	FPGA Pin Number	I/O Standard
S1	Tact1	H18	1.5V
S2	Tact2	J18	1.5V

Table 2-4: User-defined Push-button Board Reference Information

User-Defined DIP Switch

Board reference SW3 is a 3-place DIP switch. This switch is user-defined and provides additional FPGA input control. When the switch is in the OFF position, a logic 1 is selected. When the switch is in the ON position, a logic 0 is selected. There are no board-specific functions for this switch.

Table 2–5 lists the user-defined DIP switch schematic signal names and their corresponding Cyclone V E FPGA pin numbers.

Board Reference	Schematic Signal Name	Cyclone V E FPGA Pin Number	I/O Standard
1	DIP_SW1	C16	1.5V
2	DIP_SW2	D17	1.5V
3	DIP_SW3	G17	1.5V

Table 2-5: User-defined DIP Switch Board Reference Information

DDR3 Memory

The development board features a single 1 Gb (8 Meg x 16 x 8 banks) DDR3 device. The device is connected to the Cyclone V E FPGA such that the internal Hard Memory Controller (HMC) can be used. The Cyclone V E FPGA speedgrade will determine the maximum speed at which the DDR3 can be accessed as shown in Table 2-6

Temperature and Speed Grade	Maximum Frequency of Controller (MHz)
C6	400
C7	333
C8	333
I7	400

Table 2-6: Hard Memory Controller Maximum Frequency of Operation

Table 2–7 lists the DDR3 pin assignments, signal names, and functions. The signal names and types are relative to the Cyclone V E FPGA in terms of I/O setting and direction.

Cyclone V E FPGA Pin Number	Schematic Signal Name	I/O Standard	Description
L7	mem_a[0]	1.5V SSTL Class I	Address bus
K7	mem_a[1]	1.5V SSTL Class I	Address bus
H8	mem_a[2]	1.5V SSTL Class I	Address bus
G8	mem_a[3]	1.5V SSTL Class I	Address bus
J7	mem_a[4]	1.5V SSTL Class I	Address bus
J8	mem_a[5]	1.5V SSTL Class I	Address bus
A10	mem_a[6]	1.5V SSTL Class I	Address bus
A9	mem_a[7]	1.5V SSTL Class I	Address bus
A8	mem_a[8]	1.5V SSTL Class I	Address bus
A7	mem_a[9]	1.5V SSTL Class I	Address bus
C6	mem_a[10]	1.5V SSTL Class I	Address bus
D6	mem_a[11]	1.5V SSTL Class I	Address bus
D7	mem_a[12]	1.5V SSTL Class I	Address bus
C8	mem_a[13]	1.5V SSTL Class I	Address bus
A5	mem_ba[0]	1.5V SSTL Class I	Bank address bus
B10	mem_ba[1]	1.5V SSTL Class I	Bank address Bus
C9	mem_ba[2]	1.5V SSTL Class I	Bank address bus
B6	mem_cas_n[0]	1.5V SSTL Class I	Column address strobe
J9	mem_ck[0]	Differential 1.5-V SSTL Class I	Clock
H9	mem_ck_n[0]	Differential 1.5-V SSTL Class I	Clock
F14	mem_cke[0]	1.5V SSTL Class I	Clock Enable
E9	mem_cs_n[0]	1.5V SSTL Class I	Chip Select
G11	mem_dm[0]	1.5V SSTL Class I	Data Mask

J17	mem_dm[1]	1.5V SSTL Class I	Data Mask
E12	mem_dq[0]	1.5V SSTL Class I	Data bus bit 0, byte lane 0
D12	mem_dq[1]	1.5V SSTL Class I	Data bus bit 1, byte lane 0
C11	mem_dq[2]	1.5V SSTL Class I	Data bus bit 2, byte lane 0
K9	mem_dq[3]	1.5V SSTL Class I	Data bus bit 3, byte lane 0
C13	mem_dq[4]	1.5V SSTL Class I	Data bus bit 4, byte lane 0
D13	mem_dq[5]	1.5V SSTL Class I	Data bus bit 5, byte lane 0
B12	mem_dq[6]	1.5V SSTL Class I	Data bus bit 6, byte lane 0
F12	mem_dq[7]	1.5V SSTL Class I	Data bus bit 7, byte lane 0
F13	mem_dq[8]	1.5V SSTL Class I	Data bus bit 8, byte lane 1
E14	mem_dq[9]	1.5V SSTL Class I	Data bus bit 9, byte lane 1
J11	mem_dq[10]	1.5V SSTL Class I	Data bus bit 10, byte lane 1
A13	mem_dq[11]	1.5V SSTL Class I	Data bus bit 11, byte lane 1
B15	mem_dq[12]	1.5V SSTL Class I	Data bus bit 12, byte lane 1
C15	mem_dq[13]	1.5V SSTL Class I	Data bus bit 13, byte lane 1
G15	mem_dq[14]	1.5V SSTL Class I	Data bus bit 14, byte lane 1
K16	mem_dq[15]	1.5V SSTL Class I	Data bus bit 15, byte lane 1
H11	mem_dqs[0]	Differential 1.5-V SSTL	Data Strobe

		Class I	
H14	mem_dqs[1]	Differential 1.5-V SSTL Class I	Data Strobe
G12	mem_dqs_n[0]	Differential 1.5-V SSTL Class I	Data Strobe
J13	mem_dqs_n[1]	Differential 1.5-V SSTL Class I	Data Strobe
L8	mem_odt[0]	1.5V SSTL Class I	On Die Termination Control
B7	mem_ras_n[0]	1.5V SSTL Class I	Row Address Strobe
J19	mem_reset_n	LVCMOS15	Reset in
F7	mem_we_n[0]	1.5V SSTL Class I	Write Enable
B11	oct_rzqin	SSTL-15	Calibration

Table 2-7: DDR3 pin assignments, signal names, and functions

EEPROM

This board includes a 1-Kb EEPROM device. This device has a 2-wire serial interface bus I2C. Table 2-8 lists the EEPROM pin assignments, signal names and functions. The signal names and types are relative to the Cyclone V E FPGA in terms of I/O setting and direction.

Schematic Signal Name	FPGA Pin Numbers	I/O Standard	Description
EEPROM_SDA	P16	2.5-V	Serial Data / Address
EEPROM_SCL	P17	2.5-V	Serial Clock

Table 2-8:   EEPROM Board Reference Information

40 Pin Prototyping Headers

The BeMicro CV Board includes two 2×20 prototyping headers. The FPGA I/Os route directly to the headers for design testing, debugging, verification and prototyping. Table 2–9 and Table 2-10 summarize the debug header pin assignments, signal names, and functions for 40 Pin Prototyping Headers J1 and J4.

Pin Number	Schematic Signal Name	Cyclone V E FPGA Pin Number	I/O Standard
1	GPIO_01	T22	2.5V/3.3V
2	GPIO_02	T15	2.5V/3.3V
3	GPIO_03	R22	2.5V/3.3V
4	GPIO_04	R15	2.5V/3.3V
5	GPIO_05	R21	2.5V/3.3V
6	GPIO_06	R16	2.5V/3.3V
7	GPIO_07	P22	2.5V/3.3V
8	GPIO_08	R17	2.5V/3.3V
9	DIFF_TX_5+	N20	2.5V/3.3V
10	DIFF_TX_5-	N21	2.5V/3.3V
11	VCC5P0	na	5V
12	GND	na	GND
13	DIFF_TX_6+	M22	2.5V/3.3V
14	DIFF_TX_6-	L22	2.5V/3.3V
15	DIFF_TX_7+	M20	2.5V/3.3V
16	DIFF_TX_7-	M21	2.5V/3.3V
17	DIFF_TX_8+	K21	2.5V/3.3V
18	DIFF_TX_8-	K22	2.5V/3.3V
19	DIFF_TX_9+	T19	2.5V/3.3V
20	DIFF_TX_9-	T20	2.5V/3.3V
21	DIFF_RX_9+	T18	2.5V/3.3V
22	DIFF_RX_9-	T17	2.5V/3.3V
23	DIFF_RX_8+	L19	2.5V/3.3V
24	DIFF_RX_8-	L18	2.5V/3.3V
25	DIFF_RX_7+	K17	2.5V/3.3V
26	DIFF_RX_7-	L17	2.5V/3.3V
27	DIFF_RX_6+	N19	2.5V/3.3V

28	DIFF_RX_6-	M18	2.5V/3.3V
29	VCC3P3	na	3.3V
30	GND		
31	DIFF_RX_5+	N16	2.5V/3.3V
32	DIFF_RX_5-	M16	2.5V/3.3V
33	DIFF_RX_4+	U10	2.5V/3.3V
34	DIFF_RX_4-	T9	2.5V/3.3V
35	DIFF_RX_3+	R9	2.5V/3.3V
36	DIFF_RX_3-	T10	2.5V/3.3V
37	DIFF_RX_2+	U12	2.5V/3.3V
38	DIFF_RX_2-	U11	2.5V/3.3V
39	DIFF_RX_1+	R11	2.5V/3.3V
40	DIFF_RX_1-	R10	2.5V/3.3V

Table 2-9: Board Reference Information for 40 Pin Prototyping Header J1

Pin Number	Schematic Signal Name	Cyclone V E FPGA Pin Number	I/O Standard
1	VCC3P3	na	3.3V
2	VCC3P3	Na	3.3V
3	I2C_SDA	G1	2.5V/3.3V
4	I2C_SCL	G2	2.5V/3.3V
5	GPIO_A	V10	2.5V/3.3V
6	GPIO_B	P8	2.5V/3.3V
7	GND		
8	GND		
9	GND		
10	GND		
11	LVDS_TX_E4-	R7	2.5V/3.3V
12	LVDS_TX_E4+	P7	2.5V/3.3V
13	LVDS_TX_E3-	W8	2.5V/3.3V
14	LVDS_TX_E3+	W9	2.5V/3.3V

15	LVDS_TX_ECLK-	U6	2.5V/3.3V
16	LVDS_TX_ECLK+	V6	2.5V/3.3V
17	GND		
18	GND		
19	LVDS_TX_E2-	U7	2.5V/3.3V
20	LVDS_TX_E2+	U8	2.5V/3.3V
21	LVDS_TX_E1-	AA7	2.5V/3.3V
22	LVDS_TX_E1+	AB7	2.5V/3.3V
23	LVDS_TX_E0-	AB6	2.5V/3.3V
24	LVDS_TX_E0+	AB5	2.5V/3.3V
25	GND		
26	GND		
27	LVDS_TX_O4-	AA8	2.5V/3.3V
28	LVDS_TX_O4+	AB8	2.5V/3.3V
29	LVDS_TX_O3-	AA10	2.5V/3.3V
30	LVDS_TX_O3+	AA9	2.5V/3.3V
31	LVDS_TX_OCLK-	Y10	2.5V/3.3V
32	LVDS_TX_OCLK+	Y9	2.5V/3.3V
33	GND		
34	GND		
35	LVDS_TX_O2-	R12	2.5V/3.3V
36	LVDS_TX_O2+	P12	2.5V/3.3V
37	LVDS_TX_O1-	AB10	2.5V/3.3V
38	LVDS_TX_O1+	AB11	2.5V/3.3V
39	LVDS_TX_O0-	Y11	2.5V/3.3V
40	LVDS_TX_O0+	AA12	2.5V/3.3V

Table 2-10: Board Reference Information for 40 Pin Prototyping Header J4

80 Pin Edge Connector

All BeMicro cards have an 80 Pin Card Edge Connector Interface.

CAUTION

The BeMicro Card Edge Connector is not a standard interface with regards to FPGA connectivity.   Ensure that any card you connect to the BeMicro's 80 Pin Card Edge Connector is intended for that particular BeMicro variant.   For further guidance consult the add-on card's documentation, along with the BeMicro CV Schematic at
http://parts.arrow.com/item/detail/arrow-development-tools/bemicrocv

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Power Supply

The development board gets its power from the USB connector.   For additional power, a 5V external supply can be provided to J8.

Table 2-11 summarizes the various power rails on the BeMicro CV Board.

Schematic Signal Name	Voltage (V)	Description
VCC	1.1	FPGA core power
VCCAUX	2.5	Auxiliary power
VCCA_FPLL	2.5	PLL analog power
VCCIO_3.3V	3.3	3.3V I/O power rail
VCCIO_VCCPD_2.5V	2.5	2.5V I/O and pre-driver power rail
VCCIO_1.5V	1.5	1.5V I/O power rail
VCCIO_1.2V	1.2	1.2V I/O power rail

Table 2-11:   BeMicro CV Board Power Rails

The BeMicro CV Board supports VCCIO of 2.5V or 3.3V for I/O Banks 3A, 3B, 4A and 5B.   Setting the I/O voltage for one of these banks sets it for all of the banks.   Table 2-12 describes how to set the VCCIO voltage.

VCCIO	J11 Jumper Location
2.5V	Connect pin 1 and 3
3.3V	Connect pin 1 and 2

Table 2-12:   Setting VCCIO for Banks 3A, 3B, 4A and 5B

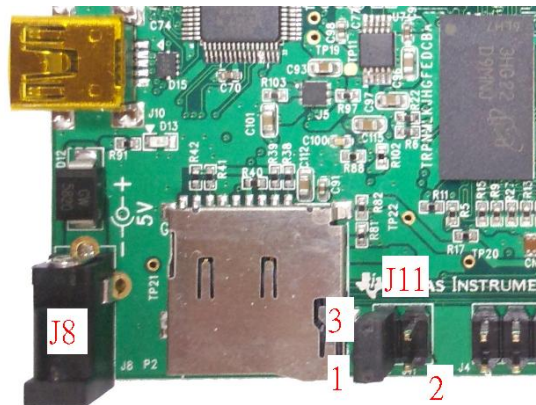Figure 2-4 identifies the pin information for header J11.

Figure 2-4: Setting the VCCIO Bank Voltage for Banks 3A, 3B, 4A, 5A and 5B

3. Board Components Reference

This chapter describes the Cyclone V E FPGA development board components. Table 3-1 lists the devices on the BeMicro CV Board along with Manufacturer Part Numbers and website information.

Board Reference	Component	Manufacturer	Manufacturer Part Number	Manufacturer Website
P1	FPGA, Cyclone V E, 5CEFA2F23C8N	Altera	5CEFA2F23C8N	www.altera.com
P2	Micro SD Card Reader	Cen Link	ZM90-15000-0AR1	www.cenlink.com.tw
P3	MAX V 5M80ZE64	Altera	5M80ZE64C5N	www.altera.com
S1,S2	Push buttons	Dawning Precision	TS-A02SA-2-S100	dawning2.en.alibaba.com
SW3	DIP Switch 2.54mm			
U1	1Gb DDR3 SDRAM (64Mb x 16)	Micron	MT41J64M16LA-15E	www.micron.com
U2	EPCS16SI8N	Altera	MX25L1606EM2I-12G	www.altera.com
U3	USB FIFO	FTDI	FT245RQ	www.ftdichip.com
U4	AT24C01BN-SH-T, 8S1, SOIC, SMD	Atmel	AT24C01BN-SH-T	www.atmel.com
U5	Dual NFETs	IR	IRLHS6276PbF	www.irf.com
U6	ADP5052	ADI	ADP5052ACPZ-R7	www.analog.com
U7	TPS51100DGQ	TI	TPS51100DGQ	www.ti.com
Y1	SOT23, 50MHz Oscillator, 1.8V	SiTime	SiT9201AC-S3-18E-50.000000Y	www.sitime.com
Y2	SOT23, 25 MHz Oscillator, 2.5V (unpopulated)	SiTime	SiT9201AC-S3-25E-50.000000Y	www.sitime.com
Y3	SOT23, 24MHz Oscillator, 2.5V	SiTime	SiT9201AC-S3-25E-24.000000Y	www.sitime.com

Table 3-1: Component Information for Devices on BeMicro CV Board

4. Additional Information

This chapter provides additional information about the document.

Board Revision History

The following table lists the versions of all releases of the Arrow Electronics BeMicro CV Cyclone V FPGA Development Board.

Release Date	Version	Description
September 2013	Initial release	Limited production run

Document Revision History

Date	Version	Description
September 2013	1.0	Initial Release
December 2013	1.1	Format Updates

For further information on the BeMicro CV Cyclone V E Development Board visit
http://parts.arrow.com/item/detail/arrow-development-tools/bemicrocv