# Introduction

These guidelines were created for use with the existing Memory Design Guidelines and provide information on the simulations necessary to create the information needed for those guidelines that are very important to. This set of guidelines will be created using Arria 10 IBIS models.

# **Background Knowledge Source**

The Altera External Memory Interface Handbook provides a thorough explanation of DDR4 topologies and board design guidelines for DDR4 systems. The External Memory Interface (EMIF) Handbook is very useful in understanding what needs to be done to create a successful system.

## http://www.altera.com/literature/hb/external-memory/emi\_plan.pdf

The EMIF handbook guidelines were created using useful numbers for spacing of the traces and other constraints for the system. If a 2D simulator available figures can be created for signal parallelism rules and length matching. Also duty cycle distortion for clocks and DQS signals can be examined to avoid timing problems in systems with high data rates.

In the document below the user will be lead through the simulation process using the 2D HyperLynx to determine the optimum drive and termination levels for the pseudo open drain (POD) DQ/DQS interface and create informed parallelism constraints for the topology.

# Contents

Introduction	1
Background Knowledge Source	1
Chapter 1: Background	5
Properties of DDR4 systems that have an effect on simulation	5
General Simulation Method	5
Topology	6
Fly-by with equidistant memories	6
Fly-by with "Ping Pong" configuration	6
Pre-Layout Simulations	7
Chapter 2: Board data and Simulation Models	7
Stackup	7
Stackup setup in HyperLynx	7
Simulation Models	8
Altera IBIS models from the website	8
Creating the Altera IBIS File from a Quartus Project	9
Memory Vendor IBIS Files	
EBD Simulation Files	
Chapter 3: Setting up HyperLynx	11
Locating Model Directories	11
Stackup Entry	12
Opening a new schematic	
Chapter 4: Command/Address Simulation and Analysis	
C/A Required simulation sets	
Basic C/A ISI, channel drive and termination simulation	13
C/A Drive and Termination	
New Schematic	13
Stackup entry	
Creating the topology	14
Simulation lossy channel setup	20
Nominal single channel ISI simulation run	20
Crosstalk Simulation Setup for C/A Channels for Parallelism	25

Crosstalk simulation theory	29
C/A Parallelism Simulation and Analysis	
Chapter 5: Clock Simulation and Analysis	
Basic Clock Schematic	
Pre-Layout Clock Simulation	
Pre layout clock crosstalk	40
Chapter 6: DQ/DQS Channel Simulation and Analysis	45
Termination	46
Initial setup	46
Nominal Topology to the Memory Device	47
Setting up and analyzing ISI termination simulations for DQ signals	
Nominal Topology from the Memory Device	51
Transmit Eye Mask Opening	53
Receive Eye Mask Opening	54
Crosstalk Constraint Simulations	54
Example of stripline crosstalk simulation for parallelism rules	54
A crosstalk topology	55
Setting up the simulations	55
Running the Simulations	56
Analysis of crosstalk for parallelism rules	57
DQ/DQS Simulation for ISI and Crosstalk Effects	58
ISI	58
Stackup and Topology Setup in HyperLynx	58
Termination variation simulation	58
Channel Simulation for crosstalk effects	60
Channel Simulation for SSN effects	61
Chapter 7: Further Investigations	61
Post Layout Simulation	61
Further Reading	61
EMIF Guidelines for Layout and Timing	62
Simulating for Timing Closure	62
Check these things	63

# **Chapter 1: Background**

# Properties of DDR4 systems that have an effect on simulation

The following table of properties constrains what needs to be simulated. Your requirements will vary due to device speeds and timing constraints.

### Table 1

Property	Value	Notes
I/O Voltage	1.2V	L version could be 1.05
Data Rates	1600MHz to 3200Mbps.	800MHz to 1.6GHz Clock (See
	[Arria 10 doesn't support	note 3)
	full range. Current	
	supported range is 1333	
	MHz max]	
Clock Signals	SSTL 1.2V differential	Externally Terminated (See note
		1)
Address and Control Signal Standard	SSTL 1.2V	Externally Terminated (See note
		1)
Address and Control Signal Rate	1T or 2T	(See note 4)
DQ bus	POD12	Lower SSN for systems
POD output drive strength	40 Ohms	Altera Standard (See note 2)
Board trace characteristic impedance	40 Ohms	Strongly Recommended (Micron)

Notes for Table 1:

- The Address, Command and Clock signals all use a threshold of 0.49\*VCC. For data rates up to 2133MTs the thresholds are +/-125mv. For 2400MTs the thresholds are +/-100mv.
- 2. POD12 is the acronym for the Pseudo Open Drain 1.2V interface. This interface is terminated to VCC(1.2V) to reduce simultaneous signaling noise and reduce the complexity of the system. The threshold voltage is therefore not 1/2VCC but something much higher. This voltage also depends on the strength of the driver in the long term so DDR4 memory devices have an adaptable threshold built in and bus inversion is included to help minimize DC drift in the system. The DDR4 JEDEC specification for drive strength is 39 Ohms.
- 3. The specification for DDR4 gives a clock range of 1.25ns maximum to 0.625ns minimum or 800MHz to 1600MHz.
- 4. The data rate is equal to the clock rate for 1T and half the clock rate for 2T. Using the 2T timing allows much more time for the signals to stabilize.

# **General Simulation Method**

In order to assure that a memory project will be successful a set of simulations should be created. This document covers the simulation methods necessary for DDR4.

The following subjects will be covered.

- Necessary Input
  - Topology
  - o Data Rate
  - Stackup
  - o Models
- Pre-layout Simulations
  - Command/Address group
  - Clock signals
  - o DQ/DQS Groups
- Post-layout Simulations

# Topology

DDR4 was designed to use a Fly-by topology for the Command/Address and Clock system. The DQ/DQS systems use read and write leveling to provide accurate timing for the exchange of data. The simulation set necessary for each group is unique.

The following topology details are necessary.

- The number of devices in the chain
- The expected distance between the FPGA, the memory devices, and the termination

## Fly-by with equidistant memories



## Fly-by with "Ping Pong" configuration



The challenge with the "Ping Pong" arrangement is lower impedance due to the capacitance of closely associated memory parts and branching of the controlled impedance paths.

## **Pre-Layout Simulations**

Pre-layout simulations provide information on what is needed to create a successful topology. A schematic is created using symbols for all of components and connections in the desired topology. Simulations are executed to provide information on the expected channel response and a graphical display is shown to use in analyzing the signal at the source and destination(s).

# **Chapter 2: Board data and Simulation Models**

## **Stackup**

In pre-layout simulations it is best to use the stackup that will be used for the PCB. Sometimes the final stackup is not available and one a simulation stackup can be created using the dielectric constant (Er) and the dielectric loss tangent  $(\tan \delta)$  of what will be the target dielectric. The Er only determines the propagation delay so whatever its value only changes the timing of the wave. The tan $\delta$  is important because it absorbs the high frequency portions of the waveform. This loss removes harmonics, causing smoothing of the corners of the waveforms and decreasing the risetime, therefor delaying the time of flight. A higher loss dielectric can be used to reduce the edge speed of a signal and reduce reflections as long as it does not interfere with transceiver signals that may accidently be placed on the routing layers for memory signals.

It is critical that, for microstrip simulations, the characteristics of the soldermask be known. Usually soldermask materials have a really high tan $\delta$  that make life interesting for fast edges.

### Stackup setup in HyperLynx

A stackup is needed to establish a baseline for the project. For this project the stackup data for the Arria 10 FPGA development kit (PCIe) was copied. Megrton6 was used for the board because of the transceiver requirements. Be sure to use the material that will be used to implement your project. Dielectric values are readily available from PCB manufacturers as well as from dielectric vendors.

If you have significant high-speed signal runs on the microstrip layer then be sure to have accurate data on the soldermask layer.

🚺 Stac	kup Edit	tor										
File I	idit Vie	aw He	alo									
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	Visible	Color	Pour Draw Style	Layer Name	Туре	Usage	Thickness mils	Er	Test Width mils	Z0 ohm	The	
1					Dielectric	Solder Mask	0.5	3.3				0.5 mils
2	<b>V</b>		Solid	то	Metal	Signal	1.675	<auto></auto>	6	49.9		1.675 mils
3					Dielectric	Substrate	3.3	3.4				TO 3.3 mils
4	<b>V</b>		Solid	VCC	Metal	Plane	1.35	<auto></auto>	6	70.7		1 35 mils
5			0.1.1		Dielectric	Substrate	3.3	3.4		50.0		
6	1		Solid	InnerSignal1	Metal	Signal	0.675	<auto></auto>	4	52.2		VCC
<u> </u>			0.11		Dielectric	Substrate	4	3.4		50.0		0.675 mils
8	<b>v</b>		Solid	InnerSignal2	Metal Dielectric	Signal	0.6/5	<auto></auto>	4	52.2		InnerSignal1 — 4 mils
10			Solid	CND	Dielectric	Distrate	3.3	J.4	6	70.7		
11	<b>V</b>		JUIU	GND	Dielectric	Substrate	2.2	2.4	0	70.7	-	0.675 mils
12			Solid	BOTTOM	Metal	Signal	1.675	<auto></auto>	6	49.9		InnerSignal2 — 3.3 mils
13			Solid	BOTTOM	Dielectric	Solder Mask	0.5	34	•	45.5		
					Dibiootilo	Coldor Madre	0.0	0.1				
												GND 3.5 mils
												——————————————————————————————————————
												BOTTOM 0.5 mils
												Draw proportionally Total thickness: 25.6 mils
•	_	_						_			•	Use layer colors
												No orroro in abackup
Me.	asuremen	it units: [	English 🔻									no enois in stackup.
Me	tal thickn	ess as:	Length 💌									
		do. [	Longar +									
Ľ												
												OK Cancel Help

After the circuit board layout is created, it can be imported into HyperLynx and the stackup will come with it. It is therefore important to be sure that the stackup for the board has accurate data on the actual board parameters for Dk and Df. (Er and Tan $\delta$ ).

# **Simulation Models**

For pre-layout simulations there are two options for obtaining IBIS files for use with HyperLynx. Models can be obtained from the Altera website or created from a Quartus<sup>®</sup> II project. Two types of models can be used, depending on where you are in the design of the FPGA.

The first is a set of IBIS models for all the IO capability available for the FPGA. These models have a generic set of values for the package RLC values.

The second is a set of IBIS models with models specific to the implementation and accurate RLC values for each pin. This file is very much smaller than the one you will get from the website.

## Altera IBIS models from the website

An IBIS file with models of all the possible I/O standards and strengths can be found by following the link below. There are multiple files for Arria 10 but the one that will have the models for DDR4 is Arria10.zip.

## https://www.altera.com/support/support-resources/download/board-layout-test/ibis/ibsibis\_index.html

You will need to place the unzipped data from the file somewhere you can find easily from HyperLynx.

## **Creating the Altera IBIS File from a Quartus Project**

To generate an IBIS file the project is to the point where:

- A system topology has been decided
- The pin-connection guidelines applied for the project
- A Quartus<sup>®</sup> II project with the desired I/O defined
  - Often referred to as a "Golden Top" design
    - With all of the I/O assigned to various pins
    - And the pin characteristics assigned and saved in the .qsf file for the project
    - Use the latest version of Quartus<sup>®</sup> II to insure that the latest IBIS models are generated

From the Quartus<sup>®</sup> II project, under the compilation flow, select the "EDA Netlist Writer" section and double click on "Edit Settings":

Task	û Time	1
🖻 🕨 I/O Assignment Analysis		
Fitter (Place & Route)	00:03:56	
Assembler (Generate programming files)	00:00:47	
👂 🕨 TimeQuest Timing Analysis	00:01:13	
4 🕨 EDA Netlist Writer	00:01:32	
Edit Settings		=
Tiew Report		
	Task         I/O Assignment Analysis         Fitter (Place & Route)         Assembler (Generate programming files)         TimeQuest Timing Analysis         EDA Netlist Writer         Edit Settings         View Report	Task     Time       Image: Interview     Image: Interview       Image: Interview <t< td=""></t<>

Select the IBIS format, the latest IBIS version, enable the model selector, and the per pin RLC model

Settings - a10_fpga_ddr4	
tegory:	Device
General	Board-Level
Files	Specify antione for generating output files for use with other EDA tools
Libraries	specify options for generating output mes for use with other EDA tools.
IP Seconds IP Catalog Search Locations	Board-level symbol
Design Templates	
<ul> <li>Operating Settings and Conditions</li> </ul>	Format:
Voltage	Output directory:
Temperature	
Compilation Process Settings	Board-level signal integrity analysis
Incremental Compilation	Sound 1975
Design Entry/Synthesis	Format: LBIS
Simulation	Output directory: board/ibis
Formal Verification	
Board-Level	IBIS version: 5.0
Compiler Settings	C Enable model selector
VHDL Input	Print per pip RIC package model with multiplication and D
Verilog HDL Input	Princ per prince package model with model coupling
TimeQuest Timing Analyzer	Board-level timing analysis
Assembler	
Design Assistant	Format: <none></none>
SignalTap II Logic Analyzer	Output directory:
Logic Analyzer Interface	
PowerPlay Power Analyzer Settings	Board-level boundary scan
Solv Analyzei	Formati (Mona)
	Output directory:
	Pre-configuration RSDL file
	Frecomgarador boot me
	Post-configuration BSDL file
	Reset

Where the selections for each arrow in this diagram are:

- A. Format of the output file, one can select HSPICE or IBIS, for our us it is IBIS
- B. IBIS Version: using 5.0 allows per pin RLC package model generation with mutual coupling
- C. Enabling model selector creates an IBIS files with multiple models for what-if simulation
- D. Per pin RLC package models deliver accurate package data

The resulting IBIS file, found in the directory for the Quartus project, will contain all of the models needed for successful pre and post layout simulation.

### **Memory Vendor IBIS Files**

IBIS simulation files are available from some memory vendors. These are usually generated from SPICE models and correlated with the physical device characteristics. The characteristics for devices from different vendors will be different.

### **EBD Simulation Files**

EBD files are available from some memory vendors. These are wrapper files that are used for boards in a system, such as DIMM modules.

# **Chapter 3: Setting up HyperLynx**

# **Locating Model Directories**

Once HyperLynx had been installed it is necessary to set up the project to point to the models being used. The project can be created anywhere accessible by the computer being used. The IBIS and EBD models for the devices to be used for the project can be anywhere also. What connects them together is the assignments made in HyperLynx using Models -> Edit Model Library Paths... which gives the opportunity to indicate where the model files for the project are located. It is a good idea to start with as many models as you can get from whatever manufacturers you have for the project to avoid having to go out and search for them in the middle of assembling a simulation topology.

Set Directories	83
.HYP and .FFS file path	
C:\_ddr4_simulation\	Browse
Use directory of last-opened file	Default
Model-library file path(s)	
C:\_ddr4_simulation\IBIS_Models\ C:\_ddr4_simulation\IBIS_Models\Altera_ibis\ C:\_ddr4_simulation\IBIS_Models\Micron_ibis\ C:\_ddr4_simulation\IBIS_Models\Micron_ibis\	Edit Default
Add design folder Add design folder subfolders	

Click the Edit button to assign model directories to the Model-library

	L DOIGNIN L L L
Select Directories for IC-Model Files	23
Directory list (top directory has highest precedence):	
⊡ · ☑ C:\_ddr4_simulation\IBIS_Models\ ☑ C:\_ddr4_simulation\IBIS_Models\Altera_ibis\	Add
	Add with Subfolders
	Delete
	Up
	Down
	Import
	Export
	Generate Model Index
Add design folder	Default
Add design folder subfolders Search a maximum of 3 subfolders	
OK Cancel Help	

Add folders and sub-folders where the models are located. The Add buttons open an explorer window to let you choose the ones you want. Clicking the Generate Model Index button loads the list of models into the project and returns to Set Directories.

# **Stackup Entry**

Next, set up the stackup with the materials you will be using. The graphic, above is about the minimum.

The remainder of the pre-layout section of this document will use the above stackup.

# **Opening a new schematic**

Now a schematic can be created. Clicking an icon on the task bar opens a new, free-form, schematic.



You can place IBIS drivers and receivers, transmission lines, terminators and other topology artifacts. Examples will be shown for each topology as we go.

# **Chapter 4: Command/Address Simulation and Analysis**

The Command/Address (C/A) system for DDR4 memories are SSTL signals. DDR4 differs from previous DDRx families in one respect, the 2T timing option for the C/A signals. This means that the data rate can be ½ of the SDR timing, allowing for a fairly long settling time when using this option.

# **C/A Required simulation sets**

- Inter Symbol Interference (ISI) for Drive and Termination strengths
- Crosstalk for layout parallelism rules

# Basic C/A ISI, channel drive and termination simulation

Setting up a sample C/A topology using the freeform schematic is easy.

## **C/A Drive and Termination**

For these signals the topology usually has the FPGA on one end and more than one memory device down the stream. The Fly-by topology is simple unless there are chips on both sides of the board in a "Ping Pong" configuration because of concentrated additional capacitance.

## **New Schematic**

- 1. Open a schematic window as shown above
- 2. Select File -> Save As and place the schematic in the simulation directory

## **Stackup entry**



3. In the schematic, open the stackup and fill it out with the board's materials and dimensions. Be sure to use the dielectric tab to update the Loss Tangent. Then

#### click OK to save it

Eile	ckup Edit Edit Vie	tor Pw He	ln									
<b>6</b> 6	) III E	3 6	i ci X 🖻	🖲 🖻 🔶 🕂	- 24 03		■ ?					
Basi	: Dieler	stric M	etal 70 Planning	Manufacturing	Custom View							
	Visible	Color	Pour Draw Style	Layer Name	Туре	Usage	Thickness mils	Er	Test Width mils	Z0 ohm	Thermal Co Btu/h	A
1					Dielectric	Solder Mask	0.5	3.3			0.17	0.5 mils
2	<b>V</b>		Solid	TOP	Metal	Signal	2.2	<auto></auto>	6	46.2	227.4	2.2 mils
3					Dielectric	Substrate	3	3.4			0.17	
4	<b>V</b>		Solid	VCC	Metal	Plane	1.3	<auto></auto>	6	70.1	227.4	10r 3 mils
5					Dielectric	Substrate	3.3	3.4			0.17	1.3 mils
6	<b>V</b>		Solid	InnerSignal1	Metal	Signal	0.6	<auto></auto>	6	42	227.4	VCC
7					Dielectric	Substrate	3	3.4			0.17	0.6 mile
8	<b>V</b>		Solid	InnerSignal2	Metal	Signal	0.6	<auto></auto>	6	42	227.4	0.0 mils
9					Dielectric	Substrate	3.3	3.4			0.17	InnerSignal1 3 mills
10	<b>V</b>		Solid	GND	Metal	Plane	1.3	<auto></auto>	6	70.1	227.4	0.6 mils
11					Dielectric	Substrate	3	3.4			0.17	InnerSignal2 3.3 mils
12	<b>v</b>		Solid	BOTTOM	Metal	Signal	2.2	<auto></auto>	6	46.2	227.4	
13					Dielectric	Solder Mask	0.5	3.3			0.17	1.0 mile
												GND 3 mils
												BOTTOM
м м	asuremen	it units: [ ess as: [	English V Length V								4	Draw proportionally     Total thickness: 24.8 mils     Use layer colors     No errors in stackup.

4. Since there will be more simulations coming up, use Setup -> Stackup -> Export to save the stackup so you can import it into a new schematic and save having to re-enter stackup data

### **Creating the topology**

1. Add components to the topology by clicking on the driver symbol on the ribbon



Add a symbol for each type of component in the topology being simulated



2. Double click on U1 and select the driver for the topology. NOTE: It is a good idea to open up the IBIS file, arria10.ibs, and read the notes section be familiar with the notation used for driver

# capabilities

3.

Assign Models		
IC		
	Buffer settings	S.C.
Pins:		
<b>7</b> U1.1 <b>?</b> U2.1	Part name:	Select Remove
Select the desired driver		
Select IC Model		
Information on selected d	evice	I/0 type ▶ <sub>T</sub> ⊄⊑
Library: arria10.ibs Device: Arria10		
Signal: sstl12_rtpio_r4	0_lv	Vinh = 750.0 mV VinL = 450.0 mV
Pin: 1706		Cref = 0.0 pF

Model:			Model Selector Vmea:	s= 540.0 mV
Select a library, device .EBD .IBS SPICE S-Parameter (Touchstone) All	e, and signal/pin Libraries: arria10.ibs mt40l512m8hx.ibs mt40lg4hx.ibs z80a.ibs	Devices:	Signal: sst112_rtpio_g60c_r24 * sst112_rtpio_g120c_r4 sst112_rtpio_g120c_r4 sst112_rtpio_g120c_r6 sst112_rtpio_g120c_r2 sst112_rtpio_g120c_r2 sst112_rtpio_r40_lv sst112_rtpio_r40_lv sst112_rtpio_r60_lv sst112_rtpio_r240_lv sst112_rtpio_r240_lv sst112_rtpio_r240_lv sst112_rtpio_r240_lv sst115_rtnin_g20c_lv	Select by Pin Signal
Find Model	Hint Try 'Find Model' to sear	ch for a component.		Help

4. The typical RLC values for all pins in this IBIS file are: 289milliohms, 2.16nH, and 1.43pf.

5. Repeat for U2 with the desired receiver

Select IC Model			8
Information on selected device		-1/0 typ	
Library: mt40lg4hx.ibs			IN
Device: MT40L1G4HX		Vinh =	725.0 mV
Signal: AU Dim 1:0		VinL =	: 475.0 mV
Model: INPUT_2133	Model Selector		
Notes: [forward]			
[Source] From silicon level SPICE model at Micron Technolog	y, inc. 🔹		
Select a library, device, and signal/pin			-Select by-
Libraries: Devices:	Signal:		
.IBS nt401512m8by ibs	A0 61		Summ.
SPICE mt40lg4hx.ibs	A2	Ξ	Pin
S-Parameter Z80a.ibs	A3		Circual
[louchstone]	A4 A5		Signal
All 🔮	A6		
	A7 A8		
	A9		
	A10		
	A12_BC_n		OK
<b>v</b>	A13	Ψ.	Canaal
- Hint			Cancer
Find Model Try 'Find Model' to search for a component.			Help

- 6. The RLC values for this pin are: 191.0milliohms 1.111nH 0.299pF, these values will be slightly different from signal to signal
- 7. Set U1 up as an output

Assign Models				23
IC	Buffer settings	<ul> <li>Input</li> <li>Output</li> <li>Output Inverted</li> </ul>	<ul> <li>Stuck High</li> <li>Stuck Low</li> </ul>	<b>S</b>
▶         U1.1706           ←         U2.L3	Part name:			elect

8. Click OK to return to the schematic where more accurate symbols have replaced the originals



9. Next, add transmission lines to the topology for the interconnect by selecting the transmission line symbol



10. Place one on the schematic



11. Double click on the transmission line to edit its properties

Edit Transmission Line			8
Transmission-Line Type	Values Loss		
🗆 🗆 Transmission-line type 🖣		Transmission-line properties	
Uncoupled (single line)	Coupled	Name: TL1	
🔘 Simple			
Stackup	🔘 Stackup	Z0: 83.3 ohms	
Microstrip		Delay: 0.448 ns	
Buried Microstrip		B: 0.503 obms	
🔘 Stripline			

12. Click on the Values tab then place the trace on the proper layer and adjust the linewidth get the system near your target impedance

Edit Transmission Line	X
Transmission-Line Type Values Loss	
Trace properties	Electrical properties
Choose a layer from the board stackup	Z0 = 49.9 ohms Delay = 468.7 ps
Layer: 3, Signal, InnerSignal1 👻	L = 23.4 nH
Length: 3.000 in Width: 4.30 mils	C = 9.4 pF R0 = 0.789 ohms Rs = 1.909 mOhm/m-sqrt(Hz) Gd = 1.549 pS/m-Hz

13. On clicking OK the dialog closes and the symbols can be copied and arranged to fill up the topology, in this case an array of four memory chips. Connection are made by clicking on a symbol pin and dragging to another pin





14. A termination needs to be added to the topology and wired in

15. Double click on the termination resistor and assign 50 for the value, then go to Setup -> Power Supplies and change VpullUp to 0.6 to get the termination values correct

Set Power-Sup	ply Voltages and Nets	<b>—</b>
New power-su	oply net:	
		Add Net
New voltage:		
0.600	Power-supply nets:	
	Vec	
0.000	VpullDn	
V 0.600	VpullUp	
✓ 0.000	Vss	Remove Net
5.000	Vt1 =	- Nelliove Net
5.000	Vt2	

16. Double click on each transmission line segment and set the length value in the values tab to those expected for the topology



## Simulation lossy channel setup

DDR4 memory systems operate at high speed and the drivers have fast slew rates. It is important that pre-layout simulations be ran with realistic material callout and lossy simulation enabled. Be sure that the Enable Lossy Simulation icon is blue before continuing.



The simulations will be for a memory clock rate of 1066MHz.

### Nominal single channel ISI simulation run

This fires simulation will be done using just the single set of parameters entered so far. To start with

either select Simulate SI -> Run Interactive Simulation or click on the single waveform icon icon on the task bar. Here you will get an oscilloscope view with a lot of controls. The simulation that is need to see if the channel will work OK is an eye diagram. Setting this up is a little convoluted. There are a lot of choices on the right hand side of the Digital Oscilloscope. When you are setting up an Eye Diagram it is very useful to first click on the Oscillator radio button and enter the frequency for the timing. For the C/A system this would be ½ the clock frequency because the A/C system is single data rate.

Note that, under "IC modeling" Typical is selected. Altera recommends using this setting.



For a 1066 simulation this works out to using a 533.3333 frequency for the channel.

🔘 Edge	MHz 533.3333
Oscillator	Duty 50.0 %

Then select the eye diagram option and the system should be set up for the simulation.

1. Select the devices you want to see the waveform for from the list. All of the inputs are of interest just now so select U2 through U5 of the latest waveforms. We also want to see the waveforms at the die instead of the pin because at these rates there is often a real difference

Located: Always at the d	die	•
Pins		С
- 📃 Latest W	/aveforms	
⊡∰ U1		
	1706 (at	
ē∰ U2		
	L3 (at die)	
_ ⊡∰ U3		
	L3 (at die)	
- 🗰 U4		_
	L3 (at die)	-
	10(-1.5-)	
	L3 (at die)	-
 ∠Insert diff probe	、 、	

2. Run the simulation to see how things may look by clicking "Start Simulation" in the upper right hand corner of the Digital Oscilloscope. Then zoom in on the resulting eye by clicking on the zoom to extents button on the scope.

Zoom		÷#	Ū
Ð	⊕	±#	U

Adjust the sweep settings to something you are happy with.



The results look something like this



There seems to be some sort of problem here and it does not seem to be a reflection from the end of the chain. The signal at U3 actually rings back to the threshold. Though it settles later the eye opening will be compromised.

3. The only selections for the driver are 40 Ohms and 60 Ohms. We will now match the impedance of the transmission lines to 40 Ohms, the termination to 39 Ohms, and see what the waveforms look like





4. It looks like using A lower board impedance could be really good. There is a push to use lower impedances for transceiver channels because matching to the BGA, vias and connector cutouts

is much easier when the board impedance is lower. It is a good idea to work with the whole team when making these decisions.

# **Crosstalk Simulation Setup for C/A Channels for Parallelism**

Now we will examine parallelism for the C/A channel. The victim trace will have four aggressors. This topology can be created easily from one of the above topologies. The DDR4 parts were removed and most of the T-lines.



When the parts have been arrayed and connected the T-lines will be coupled together by doing the following.

1. Double click on TL4 to open the Edit Transmission Line pop-up and then click on the Stackup option under Coupled

Edit Transmission Line					23
Transmission-Line Type Val	ues Loss				
Transmission-line type		- Transmission-line	e properties		
Uncoupled (single line)	Coupled	Name:	TL4		
O Simple		70	49.9	ohms	
🔘 Stackup 📃 🖵 📿	Stackup		+0.0	orins	
Microstrip		Delay:	0.469	ns	
Buried Microstrip     Chiefine		R:	0.789	ohms	
		Comment	Stackup	1	
Cable			- 22 A		
Connector			= 23.4 nH - 0.4 - F		
	- Coupling direction	⊂ Hint	= 3.4 pr		
	Dot Bight	R is the DC resi	stance of the t	ransmission line	э.
	Dot Left				
LE-te		Transmission line	e to paste		
If your lines are mostly on the "stackup" is the best type to	e same PCB, then use.				Сору
For information on coupled lin coupling dots, see Hints.	hes or Hints				Paste
		0	К	Cancel	Help

2. The pop-up will change to the coupled line version. Click OK to start the new coupled region.

Edit Transmission Line
Transmission-Line Type Edit Coupling Regions Field Solver Add to Coupling Region Loss
Coupling regions:           Ints   Hints This dialog box is asking to which coupling region you want to add the transmission line you just made coupled. • To add the line to a new coupling region, double-click in the list on the "New-Coupling" entry, or click once on "New-Coupling" and click another tab. • To add the line to a new sisting coupling region, double-click on the name of the existing region, or click once on the name and click another tab.
OK Cancel Help

3. Next, double click on TL2 and click on the Coupled Stackup button then click OK. Do not select "(New-Coupling)" as we are adding the transmission line to the existing coupling.



4. Repeat the above sequence, progressing down the array of T-lines to complete the topology. You will observe dashed lines indicating the coupling between the T-lines.

U4.1706 TL4 R4 49.9 ohms 50.0 ohms 468.677 ps Arria10 3.000 in sstl12\_rtpio\_r40\_lv Net004 Coupled Stackup Net004 U2.1706 TL2 R2 • 49.8 ohms 50.0 ohms 468.677 ps VpullUp ⊚ Arria10 3.000 in 0.6V sstl12\_rtpio\_r40\_lv Coupled Stackup Net002 Net002 U1.1706 TL1 R1 e) 49.8 ohms 50.0 ohms 468,677 ps Arria10 3.000 in sstl12\_rtpio\_r40\_lv Coupled Stackup Net001 Net001 U3.1706 TL3 R3 • 49.8 ohms 50.0 ohms 468.677 ps Arria10 3.000 in sstl12\_rtpio\_r40\_lv **Coupled Stackup** Net003 Net003 U5.1706 TL5 R5 • 49.9 ohms 50.0 ohms 468.677 ps Arria10 3.000 in sstl12\_rtpio\_r40\_lv **Coupled Stackup** Net005 Net005

Design File: Command\_Address\_prll.ffs <G:\\_ddr4\_simulation\Cmmd\_Addr\ > HyperLynx LineSim v9.2

5. Double click on any T-line to observe the position it has in the array for simulation.

Edit Transmission Line		- 23
Transmission-Line Type Edit Coupling Regions	Field Solver Move to Coupling Region Loss	
Coupling regions	Coupling region	
E- Coupling0002	Name: Coupling0002	
TOP Signal Layer VCC Plane	Edit Stackup Length: 3.000 ir	n
📮 InnerSignal1 Signal Layer 👘	Transmission line	
TL4	X position: 24.60 mils Trace width: 4.30 n	niis
	Layer 3, Signal, InnerSignal1	-
TL3	Trace-to-trace separation	5
ТІБ	Left: 8.00 mils Right: 8.00 mils	
	Trace-to-plane separation	
	Left: 8.00 mils Right: 8.00 mils	
1 25	Impedance (see Field Solver tab, View button)	
: V	Transmission Line Impedance Note: 🔶 🗹 Auto d	calc
	TL4 49.9 ohms diage Calcula	ate
	TL2 49.8 ohms diagc	
	TL149.8 ohms_diagc ▼	
	< III >	
	Reference conductor	
	Type: 🗾 👻 Delete	
X=0.0	Layer:	
Move trace: 🔺 🔻 🖌 📄 Auto zoom	X Position: mils Width: mils	
	Add Ref.Conductor Delete All Ref.Conductors	s
	OK Cancel Hel	p

There is a lot of information about the array in this tab of the pop-up. Observe TL1 is selected and the position of TL1 is shaded in the physical view.

1. Close the pop-up

## **Crosstalk simulation theory**

Now we will analyze the coupling between the C/A signals. Before you enter into this effort, a decision needs to be made concerning the goals of the process. The C/A section performs like a source synchronous interface, everything happens at fairly close to the same time. Transitions of these signals from high to low and low to high occur very close together in time. After this simultaneous switching event it is very calm. The transitions get a little messy then the steady state of the eye damps out to a very good opening. If you are designing a board for the PCIe form factor and, therefore, need to pack

the interface into a narrow channel on a crowded layer, then your needs are not going to be met for someone designing a signal integrity demonstration board with almost infinite space. Many high performance memory systems have been designed with a -20db crosstalk level for the C/A signals. Signals outside of this grouping may deed more isolation due to the possibility of transient events after the C/A signals should be settling. For this reason, the following investigation will be focused on a -20db crosstalk limit.

## **C/A Parallelism Simulation and Analysis**

In order to analyze the coupling between the aggressors and the victim in as short of time as possible the strategy of using a sweep of parameters we can control. The parameters we can control have to do with signal trace spacing and coupling length.

Here is how to set it up:

4.

or select Simulate SI -> Run Interactive Sweeps 2. Select the Run Interactive Sweeps... icon to open the Sweep Manager.

ange

3. Select Coupling regions and then the coupling setup where all the T-lines are

Sweep Manager

Setup Simulation Cases	
<ul> <li>Stackup layers</li> <li>Power supplies</li> <li>IC modeling</li> <li>Passive components</li> <li>Coupling regions</li> <li>Coupling0002</li> <li>Length = 3,000 in</li> <li>TL4: Width of trace = 4,300 mils</li> <li>TL2: Width of trace = 4,300 mils</li> <li>TL1: Width of trace = 4,300 mils</li> <li>TL3: Width of trace = 4,300 mils</li> <li>TL5: Width of trace = 4,300 mils</li> <li>Separation between TL4 and TL2 = 8,000 mil:</li> <li>Separation between TL1 and TL3 = 8,000 mil:</li> <li>Separation between TL3 and TL5 = 8,000 mil:</li> </ul>	
Highlight Length then select Add Range	
Passive components     Coupling regions	Add Range
	Domovo Dono
Length = 3.000 in	Remove Rang
···· IL4: Width of trace = 4.300 mils	Copy Range

TL2: Width of trace = 4,200 mile

5. In the pop-up Sweeping window select By list and enter values for the breakout and some other distances up to the longest expected trace length. You can run many simulations easily but it becomes a problem of managing the data.

Length of Coupl	ng0002			
) By initial / final va	lues			ОК
Initial:	1.000 in	Simulation count:	5	
Final:	3.000 in	Increment:	0.500 in	Cancel
) By tolerance —				Help
Value:	3.000 in	Simulation count:	0	
Tolerance:	0 %	Increment:	0.000 in	
By list				

6. Next the separation between the T-lines will need to be swept. Select the first Separation



y initial / final values			ок
Initial: 3.	.000 mils Simulation	count: 8	Concert Concert
Final: 10	0.00 mils Increment:	1.000 mils	
y tolerance			пер
Value: 8.	.000 mils Simulation	count: 0	
olerance:	0 % Increment:	0.000 mils	
y list			
3.000 mils 4. 5.000 mils 7. 9.000 mils 1(	000 mils 5.000 m 000 mils 8.000 m	ils 🔺	

### 7. Enter in some spacing values and increment data then click OK

- TL3: Width of trace = 4.300 mils
- TL5: Width of trace = 4.300 mils
  - Separation between TL4 and TL2 = 3.000 mils 10.00 mils, by 1.000 mils (8 steps)
- Separation between TL2 and TL1 = 8.000 mils
- Separation between TL1 and TL3 = 8.000 mils
- Separation between TL3 and TL5 = 8.000 mils
- 9. Then select the next Separation and click on Paste Range as a Lock to connect them together.

#### Coupling regions



Paste Range as a Lock

10. Repeat for the other separation selections

🚊 🗹 Coupling regions
🗄 🗹 Coupling0002
··· TL4: Width of trace = 4.300 mils
··· TL2: Width of trace = 4.300 mils
··· TL1: Width of trace = 4.300 mils
··· TL3: Width of trace = 4.300 mils
··· TL5: Width of trace = 4.300 mils
✓ Separation between TL4 and TL2 = 3.000 mils - 10.00 mils, by 1.000 mils (8 steps)
Separation between TL2 and TL1 = locked (interactively) to Coupling0002 Separation between TL4 and TL2
Separation between TL1 and TL3 = locked (interactively) to Coupling0002 Separation between TL4 and TL2
Separation between TL3 and TL5 = locked (interactively) to Coupling0002 Separation between TL4 and TL2
in Pin-specific buffer models

11. Now everything is set up except for the drivers. Close the Sweep Manager and set the driver for

U1 as Stuck High			
Assign Models			
IC			
Pins:	Buffer settings	<ul> <li>Input</li> <li>Output</li> <li>Output Inverted</li> </ul>	<ul> <li>Stuck High</li> <li>Stuck Low</li> </ul>
<ul> <li>► U1.1706</li> <li>► U2.1706</li> <li>► U3.1706</li> <li>► U4.1706</li> <li>► U5.1706</li> </ul>	Part name: Library: arria10.ibs Device: Arria10 Signal: sst112_rtpio_	r40_lv	Sele Ren H

12. The other drivers are just left as Output to switch together and provide the highest aggressor interference

Assign N	/lodels					23
IC Pins:	]		Buffer settings	<ul> <li>Input</li> <li>Output</li> <li>Output Inverted</li> </ul>	<ul> <li>Stuck High</li> <li>Stuck Low</li> </ul>	<b>S</b>
T T T T	U1.1706 U2.1706 U3.1706 U4.1706 U5.1706	^	Part name: Library: arria10.ibs Device: Arria10 Signal: sst112_rtpio_ Pin: 1706	r40_lv		elect emove Help

13. Reopen the Sweep Manager and click Run Sweeps. Here we will use the settings from the termination run and not worry about the frequency of the clock because the slew rate of the drivers is the determining factor for coupling. Set up the simulation for eye diagram to get some randomization of the coupling, select the termination resistor of the victim driver for analysis

and click Start Sweeps.

Operation	Tur Diaman	Start Sweeps
Standard	Eye Diagram	Sinuiator
Stimulus		Auto 👻
Global		Simulate t-planes
Per-Net/Pin		Time Resolution
	_	Auto    10 ps
Configure		
IC modeline		SPICE Uptions
Slow-Weak	Typical	Fast-Strong
Show		
🔽 Deedaut taut	Probes:	
Eye mask	Located:	
	Always at t	he die 🔻 🔻
Visibility Voltage Current Zoom 	Pins - Lates + # L +	C st Sweep Wa J1 J2 J3 J4 I5 S1 2 (at pin) 2 33 34 44 35 obe>
Thresholds for:		



14. After the sweeps finish there should be an output that looks like this.

- 15. Now to analyze the data:
  - Use the Save/Load button to export the data to .csv file for analysis



16. Open the .csv file in a spreadsheet to enable analysis. This will be a huge spreadsheet but there is room at the top to calculate the crosstalk in db for the data. This is created by taking the maximum minus the minimum voltage for each column, dividing this by 1.2 and then calculating 20\*log() of that value. It is up to the engineer to select the parallelism value for the interface. Many systems have been created using the value for -20db with good success.

	C8	• (*	$f_{x}$	<i>f</i> <sub>x</sub> =MAX(C11:C1034)-MIN(C11:C1034)		
	А	В	(	С	D	E
5	Created			П		
6	Probe 5: d	isabled		$\sim 11$		
7	Probe 6: R	1.2 (at pin)		V		
8	Coupling	voltage delta		0.0658708	0.0933505	0.100298
9	Coupling i	in db		-25.20976616	-22.18129195	-21.55777946
10		Time	Probe V V [R	1.2 (at pin)] 3	Probe V V [R1.2 (al p	Probe V V [R1.2 (al p

	C9	• (	f <sub>x</sub>	=20	*LOG <b>(</b> C8/:	1.2)		
	Α	В		С			D	E
5	Created							
6	Probe 5: d	lisabled		- 4	5			
7	Probe 6: R	1.2 (at pin)		_ /	1			
8	Coupling	voltage delta			.0658708		0.0933505	0.1002
9	Coupling	in db		-25.	20976616		-22.18129195	-21.557779
10		Time	Probe V V [F	R1.2 (a	at pin)] S P	robe V	V [R1.2 (at p Pr	obe V V [R1.2 (at p

# **Chapter 5: Clock Simulation and Analysis**

Clock simulation is very much like the C/A analysis except it is differential and very sensitive to Duty Cycle Distortion (DCD). Setting up the simulation is much complicated by the need to start with coupled differential signals with balanced length and using differential IBIS models. To this point we have the tools for most of this and the drivers are just named differently as disclosed in the IBIS file header. Because the 40 Ohm drivers worked well with 40 Ohm transmission lines it will be a good place to start.

# **Basic Clock Schematic**

To place a differential IBIS part, select the differential driver symbol . Then assign a differential driver to the symbol. When you add the differential model, the opposite polarity model is assigned to

the other output.

Select IC Model	evice		_ 1/0	type
Library: arria10.ibs Device: Arria10 Signal: dsstl12_rtiop_r4 Pin: 699 Model: Notes:	lOc_lv	[	Vin Vin Model Selector Vmea	h = 750.0 mV L = 450.0 mV f = 0.0 pF as= 540.0 mV
Select a library, device, an Libra .IBS () Mt4l SPICE () S-Parameter (Touchstone) All ()	nd signal/pin aries: 10.ibs 0151 2m8hx.ibs 01g4hx.ibs a.ibs	Devices:	Signal: dsstl12_rtiop_g120c_i dsstl12_rtiop_g120c_i dsstl12_rtiop_g120c_i dsstl12_rtiop_g120c_i dsstl12_rtiop_g120c_i dsstl12_rtiop_g120c_i dsstl12_rtiop_r40_lv dsstl12_rtiop_r40_lv dsstl12_rtiop_r60_lv dsstl12_rtiop_r60_lv dsstl12_rtiop_r240_lv dsstl12_rtiop_r240_lv dsstl15_rtinn_g20c_lv dsstl15_rtinn_g30c_lv	Select by
Find Model His	nt y 'Find Model' to searc	h for a component.		Help

Once you have the Arria 10 model assigned, repeat the process for the memory devices by adding a

differential symbol from the ribbon () and assigning the proper model from the memory IBIS file. Once you have one instantiated, copy it for the remainder of the memory parts so you do not have to repeat the assignment.

Place T-lines, adjust their lengths and couple the differential segments according to the board stackup plan. Be careful to give each segment its own coupling region.



Then add the termination to the topology.

#### The finished schematic could look something like this:

Design File: Command\_Address\_basic\_40.ffs <G:\\_ddr4\_simulation\Cmmd\_Addr\> HyperLynx LineSim v9.2



## **Pre-Layout Clock Simulation**

Since the clock is an oscillation the simulation setup is a little different.

- 1. Just open the interactive simulation window
- 2. Set up the simulation as Standard, Global, Oscillator, and 1066.667 MHz

<ul> <li>Operation</li> <li>Standard </li> </ul>	en Fre Diagram	Start Simulation
Stimulus Global -		Simulator Auto Simulate t-planes Time Besolution
<ul> <li>Edge</li> <li>Oscillator</li> </ul>	MHz 1066.667	SPICE Options
A modeling Slow-Weak	. 💿 Typical	Fast-Strong
C Overview p Readout te	ane Probes: <sup>xt</sup> <u>Located:</u>	
<ul> <li>Loaded res</li> <li>Previous re</li> <li>Latest result</li> </ul>	ults Always at sults ts Pins	the die 🔹

3. Run the simulation to see the waveform. If there are not at least 10 cycles of the signal, then increase the horizontal scale to obtain many cycles so that the DC balance is good. Then reduce the horizontal scale and use the position bar on the display to scroll to the right end to observe

#### the waveforms for the clock.



4. There are a couple of things that are of interest in these waveforms. One of them is the overshoot difference, especially with reference to the signal U2. The other is duty cycle distortion (DCD). The DDR4 JEDEC specification indicates that DCD is constrained to fairly small values. Turn off all the waveforms except U2 and analyze the zero crossing time for each half cycle.



This turns out to be 468.6ps for the positive side and 467.4 for the negative side. This is not a big difference. The DCD is really low, so we are probably good to go with a 40 Ohm driver, 40 Ohm board impedance and 39 Ohm termination.

5. Other simulations can be created with different impedance driver/board/termination values to see what happens. This effort is and optional exercise for the designer to see what seems best.

# Pre layout clock crosstalk

1. First, set up the topology using the same widths as were used for the single line clock simulation. Start with all of the T-lines uncoupled, as above, and go down through the

schematic, coupling the lines



- 2. Configure the drivers by double clicking on any driver
  - The positive side of U1 to Stuck High
  - The positive sides of U2 and U4 to Output

Assign Models	
IC Pins:	Buffer settings
<ul> <li>▶ U1.699</li> <li>▶ U1.700</li> <li>▶ U2.699</li> <li>▶ U2.700</li> <li>▶ U3.699</li> <li>▶ U3.700</li> <li>▶ U4.699</li> <li>▶ U4.700</li> </ul>	Part name: Library: ania 10.ibs Device: Ania 10 Signal: dsstl 12_rtiop_r40c_lv Pin: 699 Model: dsstl 12_rtio_r40c_lv
► 05.699 ► 05.700	Vcc pin:
Reference designator: U5 Pin name: 699 V Assign model's pin name	Model to paste Copy Paste Paste All

• The positive sides of U3 and U5 to Output Inverted to cause the most coupling

- 3. Set up the simulation for crosstalk by opening the interactive sweeps window
- 4. Add ranges for the length and couple separation, use the "Copy Range" and "Paste Range as a Lock" buttons when doing more than one separation in sync. This limits the number of

simulations that need to be run



5. Click on Run Sweeps and set the oscilloscope up for Standard operation, Global Stimulus, 1066.666MHz Oscillator at 50% duty cycle, then double click on <Insert diff probe>



6. Select the two resistors for the victim channel, in the case of the schematic, above, these are R1 and R2 then click OK



7. The only signal that needs to be selected for the simulation is the one just added, the differential probe



8. Select Start Sweeps and zoom in on the results, notice that there seems to be very little coupling when starting with the nominal, 8mils, differential spacing



- 9. Click on Save/Load and save the results to a .csv file
- 10. Open the .csv file in a spreadsheet and analyze the crosstalk amounts
  - Use the same sort of formulas as shown for the C/A system analysis, above
  - o Note that the maximum coupling is not very much, it is always less than -84db
  - o This indicates that 8 mils is probably going to be OK 84 db is quite a lot of isolation

	А	В	С	D	E	F	G
1	HyperLynx O	scilloscope					
2							
3	Design file: C	LOCK_40_>	(TLK.FFS Designer: David	l Lieby			
4	Created on: V	Vednesday	, October 07, 2015 Time: 9:	53:49 AM			
5	Max diff		2.91E-05	3.2E-05	3.27E-05	4.27E-05	2.96E-05
6	db coupling	-84.1573	-87.51699405	-86.6822	-86.4845	-84.1573	-87.3303
7		Time	Probe V V [R1.2 (at pin)/R2.	Probe V V	Probe V V	Probe V V	Probe V V
8		0.00E+00	0.6914212	0.69065	0.689881	0.689114	0.688348

# Chapter 6: DQ/DQS Channel Simulation and Analysis

The drive standard for the DQ/DQS system for DDR4 is specified to be Pseudo Open Drain (POD). In POD the signal lines are terminated by an impedance to Vcc and not a synthesized Vtt for the system. The reason for this is the reduction of simultaneous switching noise for the system. The impact that this

standard has on the system is profound. With no Vtt constantly establishing a nominal threshold for the eye diagram things get a little fuzzy when it comes to determining the best driver/board/termination values for a particular system.

# **Termination**

The nominal impedance for the DDR4 has been set to 40 Ohms during the C/A simulations. A DQ topology, below, was created to determine what the optimal impedance would be for the drivers and receivers.

## **Initial setup**

Create a single ended topology with the same T-line as the CA system with a single ended driver on each

 $\triangleright$ 

end using the single line model placement on the top ribbon.



Selecting the driver for the Arria 10 is fairly straight forward. Double click on the symbol for U1.1 and select a POD symbol with 40 ohm drive and termination

II Select IC Model			8
Information on selected device		-1/0	) type
Device: Arria10 Biggal: pod12_rtnp_g40c_r40p1_lv		Vi	nh = 990.0 mV
Pin: 1362		Vi Diadal Calasta	nL = 690.0 mV ref = 0.0 pF
Notes: [Source] Altera Corporation			eas= 54U.U mV
Seect a library, device, and signal/pin			Select by
Libraries:	Device: Arria10	Signal: pod12 rtnio q34c r48p1 lv	-
SPICE mt400512monx.lbs mt401g4hx.ibs S-Parameter z80a.ibs		pod12_ttrio_g34c_r60cp0_v pod12_ttrio_g34c_r60cp1_v pod12_ttrio_g34c_r60cp1_v	Pin
(Touchs:one)		pod12_rtnio_g34c_r60p1_lv pod12_rtnio_g40c_r34cp0_v	Signal
		pod12_rtnio_g40c_r34cp1_v pod12_rtnio_g40c_r34p0_lv	
		pod12_ttrio_g40c_r34p1_tv pod12_ttrio_g40c_r40cp0_v pod12_ttrio_g40c_r40cp1_v	
		pod12_rtrie_g40c_r40p0_h pod12_rtrie_g40c_r40p1_lv	OK.
		" <mark>+pod12_rtwic_g48c_r48cp8_</mark> ++ <b>-</b>	Cancel
Find Model Try 'Find Model to se	arch for a component.		Нер

and click OK.

Repeat the process for U2 by selecting DQ0 from the device.

## Nominal Topology to the Memory Device



The memory device IBIS file was created to use sub-models and selecting them is done using the model selector. The user should also be familiar with how the IBIS file provider meant for the models to be used. The Micron models provide drive termination separate from receive termination to keep the models clean so the simulation requires changing the sub-model and not just changing it from input to output.

1. Double click on U2 to bring up the Assign Models pop-up then click on Select to bring up the Select IC Model pop-up

		•				
Assign N	1odels					23
IC						
Pins:			Buffer settings	<ul> <li>Input</li> <li>Output</li> <li>Output Inverted</li> </ul>	<ul> <li>Stuck High</li> <li>Stuck Low</li> </ul>	<b>Star</b>
►- 	U1.1362 U2.C2	*	Part name: Library: mt40/512 Device: MT40L5 Signal: DO0	Èm8hx.ibs 12M8HX		elect emove Help

2. Click on the Model Selector to discover the options

Library: mt40l512m8hx.ibs Device: MT40L512M8HX	
Signal: DQ0	
Pin: C2	
Model: DQ_40_2400	Model Selector

3. Select the model needed

· · · · · · · · · · · · · · · · · · ·	 
Model Selector	23
Available models:	ОК
DQ_34_2133 34 Ohm Data I/O with no ODT (1600, 1866, 2133Mbps)	
DQ_40_2133 40 Ohm Data I/O with no ODT (1600,1866,2133Mbps)	Cancel
DQ_48_2133 48 Ohm Data I/O with no ODT (1600,1866,2133Mbps)	
DQ_IN_ODT34_2133 Data Input with 34 Ohm ODT Submodel (1600, 1866, 2133Mbps)	
DQ_IN_ODT40_2133 Data Input with 40 Ohm ODT Submodel (1600,1866,2133Mbps)	
DQ_IN_ODT48_2133 Data Input with 48 Ohm ODT Submodel (1600, 1866, 2133Mbps)	
DO IN ODTED 2133 Data Input with 60 Ohm ODT Submodel (1600-1866-2133Mbps)	
then click OK up through the pop-ups.	

## Setting up and analyzing ISI termination simulations for DQ signals

Open up the interactive sweep manager by clicking on the icon - Simulate SI -> Run Interactive Sweeps

1. FPGA Drive strengths of 34, 40, 48, and 60 Ohms and terminations of 34, 40, 48, and 60 Ohms were selected for the memories. The impedance of the T-line is still 40. Select Run Sweeps to get to the Oscilloscope window.



2. Set the simulation up for an eye diagram at 1066.667MHz and select U2 for analysis and click "Start Sweeps" to get the job done.

	<b>U U</b>		
Operation	Start Sweeps		
Stimulus	Simulator		
<ul> <li>Global</li> </ul>	Auto		
Per-Net/Pin Eye diagram	Time Resolution		
Configure.			
	SPICE Options		
IC modeling Slow-Weak	◉ Typical 💿 Fast-Strong		
Show			
	Probes:		
Eve mask	Located:		
	Always at the die 🔹 🔻		
	Pins C		
Visibility	- Latest Sweep Wa		
Voltage	i ∰ U1		
Zoom			
<b>A A</b>	<pre>L2 (at die) L2 (at die) L</pre>		
	theore an proper		

3. When the simulation is complete, open the probes pop-up by clicking on the + indicated below

🔲 Eye mask	Eye mask Always at the die			
	Pins	С	•	
Visibility	- Latest Sweep			
Voltage	i ∰ U1			
Current	⊡∰ U2			
Zoom	Ė-+Ì⊠ _C2 (a			
⊕ Æ	-^\ <b>V</b> ∪		-	
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Thresholds for:	└─── <u>└</u> ── U		Ŧ	
<no pin="" selecte="" td="" 💌<=""><td></td><td></td><td>-</td></no>			-	

4. You can expand the pop-up width to see the characteristics of the drivers and receivers, and make changes to the color of each to compare the waveforms

Pins		Color	
Ė∰ U1			
Ė∰ U2			
<u></u> - + <b>↓</b> □ c:	2 (at die)		
$\neg$	U2 DQ mode = DQ_IN_ODT34_2133 U1.1362 Model = pod12_rtnio_g34c_r34p1_lv (		
$-\sqrt{2}$	U2 DQ mode = DQ_IN_ODT34_2133 U1.1362 Model = pod12_rtnio_g40c_r40p1_lv (		
$-\sqrt{2}$	U2 DQ mode = DQ_IN_ODT34_2133 U1.1362 Model = pod12_rtnio_g48c_r48cp1_lv (		
$-\sqrt{2}$	U2 DQ mode = DQ_IN_ODT34_2133 U1.1362 Model = pod12_rtnio_g60c_r60cp1_lv (		
$-\sqrt{2}$	U2 DQ mode = DQ_IN_ODT40_2133 U1.1362 Model = pod12_rtnio_g34c_r34p1_lv (		
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$-\sqrt{2}$	U2 DQ mode = DQ_IN_ODT40_2133 U1.1362 Model = pod12_rtnio_g60c_r60cp1_lv (		
$-\sqrt{2}$	U2 DQ mode = DQ_IN_ODT48_2133 U1.1362 Model = pod12_rtnio_g34c_r34p1_lv (		
$-\sqrt{2}$	U2 DQ mode = DQ_IN_ODT48_2133 U1.1362 Model = pod12_rtnio_g40c_r40p1_lv (		
$\neg$	U2 DQ mode = DQ_IN_ODT48_2133 U1.1362 Model = pod12_rtnio_g48c_r48cp1_lv (		
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	U2 DQ mode = DQ_IN_ODT60_2133 U1.1362 Model = pod12_rtnio_g34c_r34p1_lv (		
	U2 DQ mode = DQ_IN_ODT60_2133 U1.1362 Model = pod12_rtnio_g40c_r40p1_lv (		
	U2 DQ mode = DQ_IN_ODT60_2133 U1.1362 Model = pod12_rtnio_g48c_r48cp1_lv (		
$\neg$	U2 DQ mode = DQ_IN_ODT60_2133 U1.1362 Model = pod12_rtnio_g60c_r60cp1_lv (		
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1000.0			
800.0			
600.0		1999	
000.0			

5. The best eye is given when the driver and termination match the T-line impedance



6. If you use imbalanced drivers and terminations to achieve an eye with more vertical height it will not help in the long run. One must be careful not to introduce excessive overshoot or deterministic jitter around the crossing point.

### Nominal Topology from the Memory Device

Design File: isi\_pod.ffs <C:\\_AN\_Docs\DDR4\_sim\_guide\> HyperLynx LineSim v9.2



Running a set of sweeps as was done above for the transmit eye the following waveforms were observed at the die.



Date: Thursday Apr. 16, 2015 Time: 11:06:55 Net name: Net001



### The same simulation created with the observation point at the pin of the FPGA looks like this.

This illustrates the apparent RLC interference with the signal when observed with an oscilloscope. This simulation result should be provided in a signal integrity report for the interface so the engineers in the lab will not be confused with the measurements they may make.

The best waveform set for the receive system was one that used 34 Ohm for the ODT and OCT values as seen here.



### **Transmit Eye Mask Opening**

The eye mask for the DQ/DQS systems in DDR4 is determined differently from previous generations of DDR. For the eye opening height the number to use is Vcent\_dq +/- the threshold value determined by the data rate of the interface.



For data rates up to 2133Mbps the value is +/- 68mv. For data at 2400Mbps it is +/-65mv and above that is +/-62.5mv.

The training that must take place during initialization for any DDR4 implementation establishes the best level for the internal threshold voltage for the entire chip. As a result of this training the best possible eye should resul0t.

## **Receive Eye Mask Opening**

The process used for determining the best reverence voltage on the FPGA side should be identical to the one used to set the DRAM threshold. The eye opening height is +/-70mv from that value.

## **Crosstalk Constraint Simulations**

Crosstalk is the coupling between two or more conductors running close to each other. Some teams use the term "Simultaneous Switching Noise" (SSN) for this but here we will use crosstalk to differentiate it from the effects on the signal due to power supply collapse normally indicated by SSN. The amount of crosstalk is determined by several factors. On a printed circuit board with controlled impedance traces, the coupling variables are the spacing between the traces and the length of the coupling. There will be more than one set of constraints, one for microstrip traces and another for the stripline traces.

There may be more than one layer of stripline traces in the case where a dual stripline stackup is involved. If the thickness and of the board is not as much an issue as the isolation between signals then single stripline an excellent solution. In the case of a PCIe form factor board that can only be 0.062" thick, then dual stripline will be necessary.

## Example of stripline crosstalk simulation for parallelism rules

Before the board is laid out a set of parallelism rules must be established. These rules are established to guarantee that the signal will not be distorted beyond certain limits by nearby signals. Below is a description of how to use HyperLynx to determine parallelism spacing rules.

## A crosstalk topology

The topology is created on one layer of a dual-stripline layer with one victim (U3->U8) and four aggressors. The simulation is run with the output of U3 stuck high and all of the aggressors toggling at once and in phase to yield the worst-case crosstalk. These should be executed using the drive strength and termination found above for eye optimization.

This simulation is for a stripline layer. The simulation topology for a microstrip layer is similar.



### Setting up the simulations

Newer versions of HyperLynx can run interactive sweeps of various properties in the topology.

Open up the interactive sweep manager by clicking on the icon - Simulate SI -> Run Interactive Sweeps

For this system we will sweep:

- The length of the T-lines from 1 inch to 6 inches in 0.5 inch increments
- The spacing between the T-lines from 4mils to 10mils

Sweep Manager	
Setup Simulation Cases	
<ul> <li>Barton Stackup layers</li> <li>Power supplies</li> <li>IC modeling</li> <li>Programmable buffers</li> <li>Passive components</li> <li>Pin-specific buffer models</li> <li>✓ Coupling regions</li> <li>✓ Coupling regions</li> <li>✓ Coupling the state of the s</li></ul>	Run Sweeps Add/Edit Range Remove Range Copy Range Paste Range as a Lock
	Close
Sweep simulations requested: 77	Help

The simulation was run at 1066.666MHz for this system. The results for a faster or slower clock would not matter much as the coupling is related to the risetime of the signal and not the repetition rate.

You may need to adjust the sweep parameters to suit the needs of your system.

## **Running the Simulations**

Clicking on the "Run Sweeps" button takes you to the Digital Oscilloscope where the simulations are executed. After the eye diagram simulation is set up and the latest sweeps are all checked, turn off the display of all the traces except the input to the victim signal, in this case U8.



The results of this simulation are shown here.

This looks very messy for a good reason. The beginning spacing of the lines for some cases is very close and the coupling is fairly high for those cases, also the propagation time for each length is different.





When the .csv file is opened with a spreadsheet program, formulas can be written to extract the peak to peak noise contribution for each set of spacing and lengths. The amount of crosstalk that can be tolerated should be determined by the system architect. The crosstalk will have an effect on the eye opening so a simulation should be created for the topology under consideration to determine the sensitivity of the channel. A simulation, below, will show the effects of the crosstalk.

## Analysis of crosstalk for parallelism rules

When the "Saved" file is opened in a spreadsheet program the coupling values can be readily determined. The data is used by finding the minimum spacing for given coupling lengths for a given amount of crosstalk. The crosstalk in decibels can be calculated by finding the peak to peak maximum for each case and using the nominal voltage swing for the POD 1.2V interface for the considered drivers. Each designer has an idea about what a tolerable amount of coupling is. For this instance a 40 Ohm driver was used and the nominal eye height was determined to be 950mv.

## DQ/DQS Simulation for ISI and Crosstalk Effects

Above the amount of crosstalk for a given parallelism was determined. If the engineer has decided that a -20db effect is sufficient, in the spreadsheet, above, the spacing was 7mils. It remains to see how that interferes with the system. First the disturbance caused by successive symbols on the eye diagram (ISI) is analyzed and then the effects of crosstalk added to see if the resulting eye diagram satisfies the system design goals. For more data on crosstalk please see the documentation at <a href="http://www.alterawiki.com/wiki/Arria\_10\_EMIF\_Simulation\_Guidance">http://www.alterawiki.com/wiki/Arria\_10\_EMIF\_Simulation\_Guidance</a>

### ISI

Inter Symbol Interference (ISI) is the interference between successive signals on a channel. Given a good driver, a channel with smooth impedance, and a termination that matches the transmission line, the signal should show no ISI. In the real world there are many things in the channel that are not matched to the board characteristic impedance. In addition the termination resistor value being off can cause a huge amount of interference. . For more data on ISI distortion please see the documentation at http://www.alterawiki.com/wiki/Arria 10 EMIF Simulation Guidance

### Stackup and Topology Setup in HyperLynx

The stackup and topology are the same as those for crosstalk, above.

### **Termination variation simulation**

Here we vary the ODT termination value between 40 Ohms, 48 Ohms and 60 Ohms with a 48 Ohm driver. Only the topology for U3 to U8 is used and the line spacing set to 20mils to eliminate crosstalk effects.



Here, when examined closely, it is evident that the 40 Ohm ODT receiver has the least amount of jitter at the crossing.



Date: Friday Feb. 27, 2015 Time: 16:39:19 Net name: Net001 Because DDR4 has a calibration mode that must be used to set the threshold value for the individual part, this should be the best possible eye.

Other topologies can be simulated using these techniques. Please refer to the last section of this document titled "Further Reading" for references to additional material.

## **Channel Simulation for crosstalk effects**

When we add the -20db spacing value determined from the crosstalk simulation above (7 mils) and run the simulations for ISI and ISI with crosstalk the signal looks fairly good. See the waveforms below.

The blue signal is ISI with aggressors quiet, the red signal is with aggressors running for a 3 inch topology. Aggressors for this are out of phase with the victim.



Date: Friday Apr. 17, 2015 Time: 10:19:25 Net name: Net001



This plot is the same topology with the memory devices driving the circuit the difference here is the impedance of the FPGA package.

# **Channel Simulation for SSN effects**

Simultaneous switching noise is defined here as the effects on the power supply of many signals switching together and the effect of this on the channel. This sort of simulation is not possible in HyperLynx LineSim.

# **Chapter 7: Further Investigations**

## **Post Layout Simulation**

In order to determine the overall usefulness of the layout a post-layout simulation of the channel should be executed.

It is important to use an IBIS model for the FPGA that is generated from a Quartus<sup>®</sup> II project that is created for the system. The IBIS model created this way will have correct values for the package parasitic values.

# **Further Reading**

Altera has a wealth of information on developing and simulating DDR devices. The address and command signals for DDR4 are similar to those for DDR3 except for the voltage level of the interface.

EMIF Guidelines for Layout and Timing http://www.altera.com/literature/hb/external-memory/emi\_plan.pdf

## **Simulating for Timing Closure**

The Altera wiki sight has a lot of information on this subject. Please refer to the following documents for detailed information on this subject.

The following links have a lot of information on timing parameters.

http://www.alterawiki.com/wiki/Arria\_10\_EMIF\_Simulation\_Guidance

http://www.alterawiki.com/wiki/Measuring\_Channel\_Signal\_Integrity

A definitive document on DDR4 voltages and timing is available from Micron Semiconductor. Understanding the POD training is very valuable to the designer. A full PDF of the datasheet has all the data in one place. Search on their website for "4Gb\_DDR4\_SDRAM" for a copy.

# **Check these things**

Trace impedance plays an important role in the signal integrity. Users should perform board level simulation to determine the best characteristic impedance for their PCB. For example, it is possible that for multi rank systems 40 ohm would yield better result than the traditional 50 ohm characteristic impedance.

To minimize PCB layer propagation variance, Altera recommend that you route signals from the same net group on the same layer.

- 1. Use 45° angles (not 90° corners).
- 2. Disallow critical signals across split planes.
- 3. Route over appropriate VCC and GND planes.
- 4. Keep signal routing layers close to GND and power planes.
- 5. Avoid routing memory signals closer than 0.025 inch (0.635 mm) to memory clocks.
- 6. Match the (package + board) trace delays up to 20 ps of skew for DQ/DQS/DM signals within a DQS group.
- 7. Details on how to do package de-skew is available in EMIF HB vol2 chapter 4.



- 8. All the address, command and control signals should match up to +/- 20 ps compare to the mem\_clk trace.
  - For example if the mem\_clk trace delay is 500 ps then the allowed range for any address/command/control signal is 480 ps to 520 ps.

- For discrete components; make sure above recommendation is met for each component in the fly-by chain.
- For DIMMs: For single or multiple DIMM configurations make sure this guideline is met at each DIMM connector.

The timing between the DQS and clock signals on each device calibrates to meet tDQSS.

- 9. Make sure that DQS arrives after clock :
  - (CKi ) DQSi > 0; 0 < i < number of components 1
- 10. Total skew of CLK and DQS signal between groups is less than one clock cycle:
  - (CKi + DQSi) max (CKi + DQSi) min < 1 × tCK

If you are using a DIMM topology, your delay and skew must take into consideration values for the actual DIMM.



CK<sub>i</sub> = Clock signal propagation delay to device *i* 

 $DQS_i = DQ/DQS$  signals propagation delay to group *i*