F-tile Fast Simulation Macros

for

Altera FPGA IP

Overview of Recent Macro Developments for Enhanced Simulation Speeds in Altera F-Tile FPGA IPs

This document details the recent advancements in macro development aimed at improving simulation speeds for Altera F-Tile FPGA IPs. The purpose of this documentation is to provide clarity on the specific macros applicable to various IPs and their compatibility with different Quartus versions.

Identifying Macro Usage for IP Simulation

To determine which macro is used for a specific IP, please refer to Table 1 below. This table provides a comprehensive overview, indicating the applicable macros for each IP. The applicable macros are highlighted in green within the corresponding IP columns. This visual cue helps in quickly identifying the right macro for your simulation needs.

Compatibility with Quartus Versions

It is important to note that not all fast simulation macros are supported in every version of Quartus. To find out which macros are supported by different Quartus versions, look at the same table. Each macro row is highlighted in green in the columns corresponding to the supported Quartus versions. This ensures that you can easily determine the availability of each macro for your specific Quartus version.

By following the detailed information provided in Table 1, users can effectively utilize the appropriate macros to optimize their simulation processes, ensuring compatibility and enhanced performance.

								Quartus versions			
S.no	FAST SIM MACRO	FGT	Ethernet	AN/LT	PCIe	DR	All IPs	Q 23.2	Q23.3	Q23.4	Q24.1
1	IP7581SERDES_UXS2T1R1PGD_PIPE_SPEC_FORCE										
2	IP7581SERDES_UXS2T1R1PGD_PIPE_SIMULATION										
3	IP7581SERDES_UXS2T1R1PGD_PIPE_FAST_SIM										
4	IP7581SERDES_UXS2T1R1PGD_PIPE_SKIP_LOAD_SPEC										
5	IP7581SERDES_UX_SIMSPEED										
6	IP7581SERDES_UX_ETH_SIMSPEED										
7	BK_FASTSIM_MODEL										
8	GDR_FLUX_CPUCLK_SIM_SPEEDUP										
9	FAST_SIM_ENABLE										
10	OPTIMIZED_SIM_ENABLE										
11	SKIP_CPI_ARB										
12	INTC_SIM_AN_LT_ENABLE										
13	GDR_ANLT_SIM_SPEEDUP										
14	GDR_OVERCLK_FASTSIM										
15	gdrb_GDR_PCIE_SS_DV										
16	GDR_AIB_DLL_FASTSIM										
17	GDR_ETH_FASTSIM										
18	GDR_FEC_FASTSIM										
19	SRC_SPEC_SPEED_UP										
20	REMOVE_SRC_NIOS										
21	DR_F_GAVMM_SPEEDUP										
22	UX_WORD_CLK_DRIFT_CORRECTION										
23	UX_VIP_EN_MODE (Quartus 24.3)										

Table 1: Fast Sim Macro Compatibility and Usage for Altera FPGA IPs

IP7581SERDES_UXS2T1R1PGD_PIPE_SPEC_FORCE

Macro Description: Includes optimizing the PMA and not needed to include if FGT fast Sim model is used with switch: IP7581SERDES_UX_SIMSPEED.

Limitations: None

Directions to Customer: Users have the ability to utilize this Fast Sim Macro for all designs featuring available FGTs.

IP7581SERDES_UXS2T1R1PGD_PIPE_SIMULATION

Macro Description: Includes optimizing the PMA and not needed to include if FGT fast Sim model is used with switch: IP7581SERDES_UX_SIMSPEED.

Limitations: None

Directions to Customer: Users have the ability to utilize this Fast Sim Macro for all designs featuring available FGTs.

IP7581SERDES_UXS2T1R1PGD_PIPE_FAST_SIM

Macro Description: Includes optimizing the PMA and not needed to include if FGT fast Sim model is used with switch: IP7581SERDES_UX_SIMSPEED.

Limitations: None

Directions to Customer: Users have the ability to utilize this Fast Sim Macro for all designs featuring available FGTs.

IP7581SERDES_UXS2T1R1PGD_PIPE_SKIP_LOAD_SPEC

Macro Description: Includes optimizing the PMA and not needed to include if FGT fast Sim model is used with switch: IP7581SERDES_UX_SIMSPEED.

Limitations: None

Directions to Customer: Users have the ability to utilize this Fast Sim Macro for all designs featuring available FGTs.

IP7581SERDES_UX_SIMSPEED

Macro Description: Enables behavioral model of the FGT PMA

Limitations:

1. Utilizing this macro with PTP affects accuracy.
2. Incompatible with standard AN/LT and DR modules (not compatible with FGT firmware, CPU utilized in typical flows). However, compatible with simulated AN/LT (when FAST_SIM_ENABLE=1).
3. Not supported for simplex and CDR modules (Video IPs utilize DS).

Directions to Customer: Utilize this macro for any design where its functionality remains unrestricted by the known limitations.

IP7581SERDES_UX_ETH_SIMSPEED

Macro Description: This switch enhances the FGT PMA SIM model. It should be paired with the IP7581SERDES_UX_SIMSPEED switch exclusively for Ethernet use cases (non-PCIe).

Limitations: Compatible with Ethernet IP and not compatible with custom Cadence Ethernet variants (e.g., Dynamic Reconfiguration). Additionally, async AVST variants are not supported. The clk_tx_div function abruptly halts when employing this macro (resolution anticipated in version 24.3). Xcelium is currently unsupported.

Directions to Customer: Utilize this macro during IP simulation outside of the Example Design environment, while keeping in mind its known limitations.

BK_FASTSIM_MODEL

Macro Description: This Macro Increases the FHT CPU clock speed from 450MHz to 3GHz.

Limitations: None

Directions to Customer: Users have the ability to utilize this Fast Sim Macro for all designs featuring Ethernet IP.

GDR_FLUX_CPUCLK_SIM_SPEEDUP

Macro Description: This Macro Increases the FGT firmware clock speed to 2GHz.

Limitations: None

Directions to Customer: Users have the ability to utilize this Fast Sim Macro for all designs featuring FGT IP

FAST_SIM_ENABLE

Macro Description: By setting this macro, ETH IP GUI parameter along with the Auto-negotiation and Link Training (ANLT) IP GUI parameter, RX Auto Adaptation is effectively bypassed along with the Auto-negotiation and Link Training functionality. This action updates the Auto-negotiation and Link Training status registers, marking them as completed.

Limitations: This macro is incompatible with the standard Auto-negotiation and Link Training + Dynamic Reconfiguration. Additionally, when “FAST_SIM_ENABLE” is set to 1, the use of “INTC_SIM_AN_LT_ENABLE” is prohibited.

Directions to Customer: Enable this macro only when users wish to bypass Auto-negotiation and Link Training functionality during simulation and disable this macro if user want to simulate silicon behavior.

OPTIMIZED_SIM_ENABLE

Macro Description: By configuring this macro in the Ethernet IP GUI parameter along with the AN/LT IP GUI parameter, it accelerates the ANLT operation while retaining the functionality of AN and LT

Limitations: None

Directions to Customer: Enable this macro when users aim to enable ANLT functionality while achieving faster simulation times compared to regular ANLT simulation, resembling hardware behavior.

SKIP_CPI_ARB

Macro Description: Enabling this macro skips Converged PHY Interface (CPI) arbitration within the ANLT IP.

Limitation: This macro cannot be enabled if the CPI bus is utilized by other entities such as Dynamic Reconfiguration IP, toolkits or user logic which may issue CPI commands.

Directions to Customer: Enable this macro when users aim to enable ANLT functionality while achieving faster simulation times compared to regular ANLT simulation, resembling hardware behavior.

INTC_SIM_AN_LT_ENABLE

Macro Description: Utilized this macro in standard Auto-negotiation and Link Training simulations, where RX Auto Adaptation is enabled by default, and the SRC waits for the CPI sequencer to complete loading before releasing acknowledgment, allowing IPs to exit the reset state.

Limitations: "IP7581SERDES_UX_SIMSPEED" macro cannot be utilized with “INTC_SIM_AN_LT_ENABLE” because it bypasses or disables RX Auto Adaptation, which is essential for this macro’s operation. Additionally, it's important to note that this macro cannot be utilized when “FAST_SIM_ENABLE” is set to 1, as this setting also bypasses or disables RX Auto Adaptation.

Directions to Customer: Enable this macro only when full Auto-negotiation and Link Training flow with RX Auto Adaptation enabled is required in simulation.

GDR_ANLT_SIM_SPEEDUP

Macro Description: Enabling this Macro excludes unnecessary CPI commands during the initial/bootup CPI sequencer loading process.

Limitations: None

Directions to Customer: Employ this macro in cases of ANLT designs where FGT firmware is enabled, this it can help reduce simulation time during CPI sequencer loading.

GDR_OVERCLK_FASTSIM

Macro Description: Enabling this macro decreases configuration load time by increasing the PCIe core clock frequency.

Limitations: None

Directions to Customer: Users have the ability to utilize this Fast Sim Macro for all designs featuring PCIe IP.

gdrb_GDR_PCIE_SS_DV

Macro Description: Using this macro bypasses the SerDes, exposing the PIPE interface directly to customers. It should be used in conjunction with IP7581SERDES_UX_SIMSPEED to bypass the Equalization phase.

Limitations: The 'Enable PIPE Mode Simulation' checkbox in the GUI is intended solely for simulation purposes. It does not support Quartus Compilation and is not compatible with Questa_fe (Questasim).

Directions to Customer: The VIP or BFM employed in the simulation must meet the standard PCIe pipe mode specification. When generating the Example Design, ensure to check the 'Enable PIPE Mode Simulation' checkbox in the GUI. Note that this GUI option is applicable only to simulation. Utilize this macro in conjunction with IP7581SERDES_UX_SIMSPEED to achieve maximum simulation time reduction.

GDR_AIB_DLL_FASTSIM

Macro Description: This Macro is related to Hard IP configurations that are implemented to enhance simulation speed in FEC, CRC, SYSPLL, and Tile AIB blocks.

Limitations: None

Directions to Customer: Users have the ability to utilize this Fast Sim Macro for all designs.

GDR_ETH_FASTSIM

Macro Description: Utilizing this macro, The FEC alignment marker's am_lock state machine has been optimized. Additionally, the ehip_crc_function has been rewritten to enhance runtime efficiency by adding a cache for common queries.

Limitations: This macro is incompatible with designs incorporating PCIe IP integration.

Directions to Customer: User can Incorporate this macro into any design, while being mindful of its known limitations.

GDR_FEC_FASTSIM

Macro Description: By adding this macro into the design, the FEC C-model is enabled instead of the full Verilog RTL implementation.

Limitations: During mid-simulation reset and Dynamic Reconfiguration, the reset function is invoked at time 0 using an initial block. While the FEC RTL has four resets per core, the C-functional model resets all four cores simultaneously, lacking support for individual core resets. This applies to both mid-simulation reset and Dynamic Reconfiguration scenarios.

Directions to Customer: Enable this macro setting only when user is authorized to do the resetting of all four FEC cores simultaneously during simulation.

SRC_SPEC_SPEED_UP

Macro Description: This macro is Speedup version of the NIOS-based Soft Reset Controller. This enhancement results in quicker Total Turnaround Time (TTT) significantly. However, it’s important to note that, defining the “REMOVE_SRC_NIOS” macro along with the “SRC_SPEC_SPEED_UP” will not have any implication of this macro.

Limitations: This macro has no restrictions and can be utilized across all Example design simulations. Note that using "REMOVE_SRC_NIOS" along with "SRC_SPEC_SPEED_UP" won't have any impact of this macro.

Directions to Customer: User can Incorporate this macro into any design, except those incorporating the PCIe IP.

REMOVE_SRC_NIOS

Macro Description: To utilize the non-NIOS version of the Soft Reset Controller present within the F-tile, facilitating faster execution of tile reset sequences and thereby improves the Time to Traffic. This option gives user the faster results compare to SRC_SPEC_SPEED_UP.

Limitations: Available for all Ethernet Example Designs. If the ETH IP is utilized outside of the Ethernet Example Design, users are required to trigger resets to the IP upon startup and maintain them until acknowledgment is received.

Furthermore, the following limitations apply (particularly when employing ETH IP outside the Example Design):

- Dynamic Reconfiguration and Auto-negotiation and Link Training are not supported.
- Multiple ports with multiple rates are not supported.
- Resetting multiple ports simultaneously is required.

Please note: Removal of these limitations and support for other IPs is planned for upcoming quarters.

Directions to Customer: Utilize this macro during simulations of IPs outside the ED environment, noting that there are specific limitations associated with its use.

DR_F_GAVMM_SPEEDUP

Macro Description: This macro bypasses the GAVMM accesses, facilitating direct communication between the DR controller and the tile. This eliminates the 32-8-32 and serialization steps. As a result, DR register sequences are accelerated by approximately three times.

Limitations: It is not compatible with any other IP, such as Auto-negotiation and Link Training, that utilizes the GAVMM interface. Additionally, it requires the reconfigurable clock to be sourced from the DR controller.

Directions to Customer: Utilize this macro in all DR use case simulations unless GAVMM access is needed by other IPs.

UX_WORD_CLK_DRIFT_CORRECTION

Macro Description: Activate this macro to address word clock accuracy issues in fast simulation. It must be used in conjunction with IP7581SERDES_UX_SIMSPEED

Limitations: In Quartus Version 24.1, When operating outside the ED environment, there are cases where rx_ready is not asserted. In such instances, it is necessary to remove the UX_WORD_CLK_DRIFT_CORRECTION macro.

In Quartus version 24.2, when this macro is used along with UX_VIP_EN_MODE, the above issue is resolved.

PTP regressions indicate a clock drift-related failure after 10ms of simulation clock time.

Directions to Customer: User can Incorporate this macro into any FGT design, while being mindful of its known limitations

UX_VIP_EN_MODE

Macro Description: Enable this macro only when employing an external VIP. Avoid deploying this switch for Tx to RX loopback scenarios. To ensure proper functionality, utilize this switch in conjunction with IP7581SERDES_UX_SIMSPEED

Limitations: This macro is not suitable for Tx to RX loopback scenarios.

Directions to Customer: Utilize this switch exclusively when employing an external VIP. Avoid its usage in TX to RX loopback scenarios.