



Designing SERDES-SERDES Interfaces with the 82546GB Ethernet Controller

Application Note (AP-466)



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Revision History

Revision	Revision Date	Description
1.3	April 2005	Added link status information to Section 2.1.4.2 Signal Detect.
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1.0	April 2004	<ul style="list-style-type: none">Added reference documents to Section 6.0.Added reference schematics (Section 7.0).Reworded some sentences for better clarity.
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1.0 Introduction

The goal of this document is to enable customers to construct a board layout design using the Serializer-Deserializer (SERDES) interface on Intel Gigabit Ethernet (GbE) controllers. A typical application using the SERDES interface is GbE fiber design where the electrical interface connects to an optical module. However, another possible application would use the SERDES interface to drive and receive electrical signals over a backplane for board to board communication such as in modular servers. The benefit for using the internal SERDES for a backplane is that it reduces the cost, power and board size real estate of a design since neither optical module with associated fiber connectors nor copper PHY related components, such as magnetics and cable connectors, are required. Instead, the electrical signals are sent from the internal SERDES to traces that go to a backplane connection, then over a backplane and another backplane connector to the SERDES capable link partner for communication.

The use of SERDES is called out in many industry specifications. For example:

- IEEE 802.3z: Gigabit for fiber
- 1000BaseCX: Gigabit over 30 meters of $75\ \Omega$ coax cable
- 1000BaseX
- PICMG 3.1: Gigabit over $100\ \Omega$ differential backplane

This document was created in response to customer requests for a basic level of insight into SERDES to SERDES connections for use in aiding the design of modular servers or embedded designs that are based on GbE as the protocol for onboard and board-to-board communications. Additionally, it is anticipated that many designs will require compliance with the PICMG 3.1 specification. However, since different Local Area Network (LAN) devices with a SERDES interface might use different DC-biasing and have different signaling voltage levels, there is no single SERDES-SERDES circuit that allows the LAN to work properly with every different possible pair of LAN components. This document is intended to provide basic circuit information; design considerations and testing for PICMG 3.1 compliance that should help a designer overcome many of these issues.

1.1 Scope

This application note was written specifically for the 82546GB GbE controller but the overall information can be applied to the 82545GM and 82571EB GbE controllers. All testing results were performed on modified Intel Network Interface Cards (NICs) using the 82546GB GbE controller. Similar devices with a SERDES can benefit from this document; however if using a GbE controller other than the 82546GB, designers should verify all device specifications to ensure they meet the requirements of the design.

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2.0 Basic Circuit Design

SERDES is short for a dedicated SERializer / DESerializer pair where typical inputs enter the serializer in a parallel fashion and are then serially aligned so that in one clock period one set of parallel bits (one word) is transmitted.

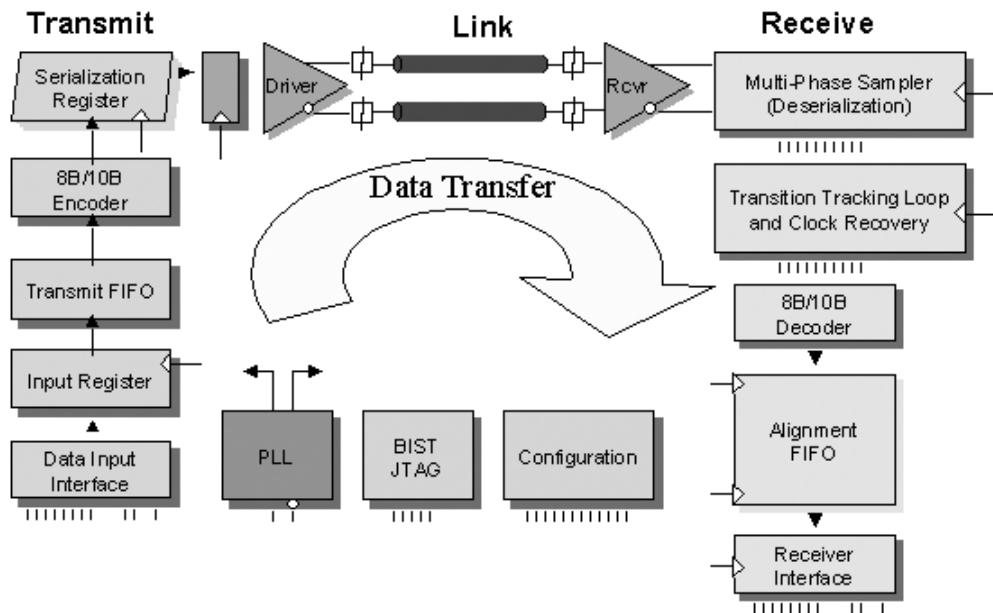


Figure 1. SERDES Functional Block Diagram

A SERDES design must be treated similar to a typical data transmission network design. The goal is to send data across some distance and have enough S/N (Signal to Noise) ratio at the receive end so that an acceptable level of errors are observed.

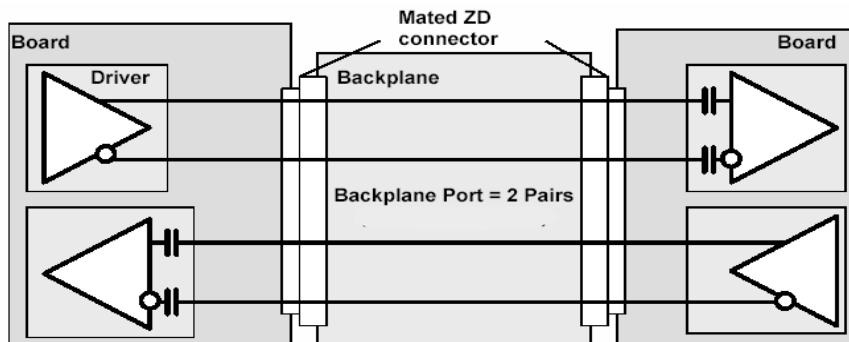


Figure 2. Basic SERDES-SERDES Backplane Circuit

Designers must consider the signal strength of the transmitter (differential output voltage), the loss due to the transmission media (trace size, shape, length) and receiver sensitivity level (minimum signal level) that detects when a 1 or 0 is being sent. The basic equation is as follows:

Transmitter Output - Physical Medium Induced Loss Receiver Sensitivity

Ideally the higher the transmit voltage output level on a SERDES device the better the design performs. However, most SERDES devices are specified with an output performance range so designers should always design with the minimum, worst case differential output level to ensure a robust design. Figure 3 shows examples of various devices and the range of their signaling levels.

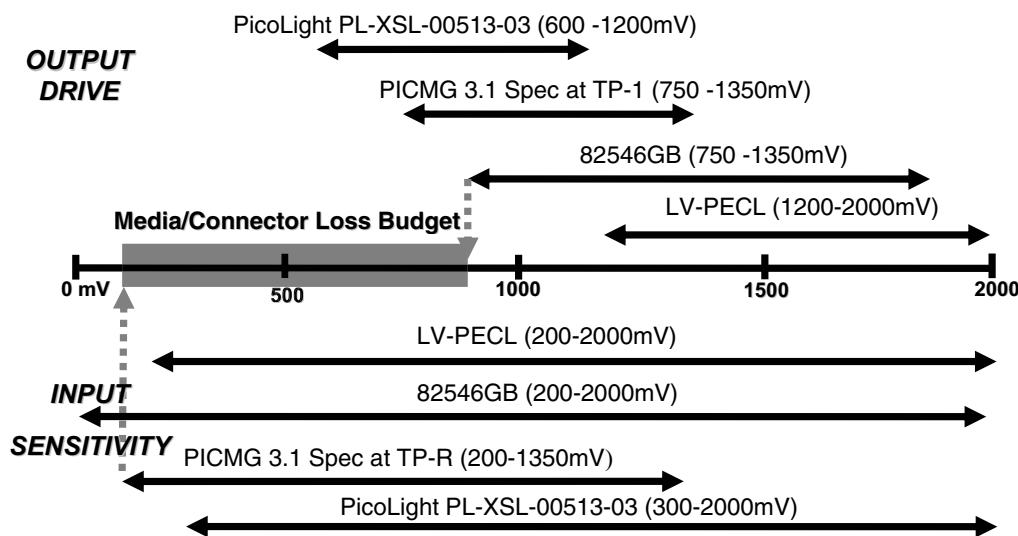


Figure 3. Peak-to-Peak Voltage Signaling Level of Various Devices

Another factor is the trace shape and length which can be a challenge to a successful design. This is mainly due to the I2R losses of the transmission trace and it determines the loss in signal strength that the transmitted signal is exposed to prior to reaching the receive device. Mechanical connectors can come into play as they disturb the impedance match between the transmitter and receiver which can degrade the signal strength.

The 1000Base-BX GbE backplane specification requires the transmit device and receive device be $100\ \Omega$ differentially terminated. Therefore connectors that might distort this impedance generate more loss or noise distortion due to standing waves or Voltage Standing Wave Ratio (VSWR), also termed “insertion loss”. A 1:1 VSWR implies a perfect impedance match between the SerDes device and electrical trace. Any difference or mismatch of these impedances can degrade an optimal power transfer.

Finally the receive device must be chosen so that when the data signal reaches the end of the line that enough voltage amplitude remains to determine if a 1 or 0 has been sent. The receiver component should be carefully chosen to include adequate design margin above the receive sensitivity. For example, a receiver with the lowest input sensitivity level provides the best margin for a design as it helps make up for the variability of the transmitter, connector, and medium losses.

2.1 Design and Layout Considerations

2.1.1 Board Layout Recommendations

In Gigabit SERDES-SERDES systems, the main design elements are the GbE controllers, the backplane connectors, and the backplane. Since the transmission line medium extends onto the Printed Circuit Board (PCB), special attention must be paid to layout and routing of the differential signal pairs as well as to the choice of the connectors. This section delves into the most critical aspects of optimizing and maintaining a usable, valid signal in a SERDES-SERDES design in both directions over the backplane.

The differential pairs should be routed to be as short and symmetrical as possible. The overall length of differential pairs is dependent on meeting Bit Error Rate (BER) requirements which in turn is dependent on material characteristics, S21 loss in the channel, the maximum transmitter output and the minimum receiver input voltage (Rx sensitivity). The general formula used to calculate the minimum received signal for successful reception is:

$$Rx_{min} = Tx_{max} - (Connector\ S21\ attenuation + Backplane\ Trace\ S21\ attenuation)$$

The lengths of the differential traces (within each pair) should be equal within 50 mils (1.25 mm) and as symmetrical as possible. Asymmetrical and unequal length traces in differential pairs contribute to common mode noise. Strip line is best to use, routed as close to connectors' layer as possible, edge coupled with $100\ \Omega$ differential trace pairs. Traces should have at minimum 100 mils spacing between differential pairs with greater than 300 mils recommended to minimize crosstalk between differential pairs. To help minimize EMI problems do not route differential traces near board edges. Within pairs keep traces close as possible to meet $100\ \Omega$ differential (<10 mils).

Keep traces as symmetrical as possible when laying out such things as components, pads, and test points keeping components as small as possible. It is critical to minimize stubs which attenuate the signal negatively. Use standard, good trace routing such as avoiding 90 degree bends; instead use two 45 degree bends with beveled corners to obtain 90 degree turns. Avoid routing differential traces near digital signal traces on the same layer and ensure that digital signal traces on adjacent layers cross at 90 degree angles to the differential traces. Keep vias to a minimum, if used at all, using no more than two per trace.

Avoid highly resistive traces by making traces as wide as possible and as thick as possible while maintaining the $100\ \Omega$ differential trace impedance. Trace width greater than 8-10 mils width is desirable. Keep transmit traces to the backplane as short as possible with two to four inches being desirable to reduce S21 loss. Additionally, trace routes of long distances should be routed at an off-angle at the x-y axis of the PCB, to distribute the effects of fiberglass bundle weaves and resin rich areas of the dielectric.

2.1.2 Board Layout Recommendations for Software Compatibility

It is recommended that all fiber-based implementations connect the energy sense output of the attached optics to Software Defined Pin (SDP) 1. This allows the software to detect a valid cable much more accurately than possible without it. Intel NIC implementations follow this recommendation and by choosing to include this in the design allows better software re-use and compatibility without requiring significant driver changes. The device EEPROM must be modified to reflect the nature of the pin being a Input pin. Please consult the appropriate EEPROM documentation for details.

For pure SERDES implementations based on the 82545 family and 82546 family it is also recommended that an EEPROM be used in order to store driver-needed data for SERDES amplitude attenuation values. This allows for environmental tuning without significant modifications from the Intel driver baseline.

These recommendations are based on Intel's own experience with cost savings and higher product quality via a more refined end user experience. The marginal cost increase of adding these extra hardware resources can be justified by the savings of software resources to overcome the lack of these recommendations.

2.1.3 Impedance Matching

Maintain $100\ \Omega$ $\pm 10\%$ differential impedance by choosing the appropriate backplane connector and PCB layout. Match the connectors' impedance as closely as possible. Transmit and receive pairs should be AC coupled through a 0.01uF capacitor to overcome differences in DC levels between the different logic types such as PECL, LVDS and etc. Place capacitors shown in the termination networks as close as possible to the receiver pins. Keep the connectors as close to the GbE controller as possible.

Connectors must be impedance matched and specified for 1.25 GHz first harmonic of the data rate and 625 MHz fundamental frequency. Pairs must be separated from adjacent pairs by having grounds between them on the connectors. The Tyco® HM-Zd or equivalent connector is a valid reference for performance when selecting a connector for your design.

2.1.4 82545GM/82546GB Gigabit Ethernet Controller Dependencies

2.1.4.1 Output Voltage Adjustment

The differential output amplitude can be adjusted by changing the value of the Extended PHY Specific Control 2 Register (Address: 26) bits 3:0. Each bit set increases the amplitude as listed in Table 1.

Table 1. SERDES Typical Output Peak-to-Peak Differential Voltage vs. Bit Setting

Bits 3:0 Register Setting	Typical P-P Voltage Output at TP-1
008h	980 mV
009h	1020 mV
00Ah	1160 mV
00Bh	1270 mV
00Ch (default)	1370 mV
00Dh	1450 mV
00Eh	1530 mV
00Fh	1590 mV

A driver, including Intel's, can be used to set the above register during initialization by placing the values desired in bits 3:0 of Word 06h in the EEPROM. For customer developed drivers, design the driver to read these bits and transfer the values to the Extended PHY Specific Control 2 Register.

2.1.4.2 Signal Detect

The signal detect pin on the GbE controller should be pulled up if no optical module exists to control link detection. When not using auto-negotiation, such as when the link partner does not support it, software should check for link before transmitting. This can be done by verifying that the MAC is synchronized by checking that bit 30 in the Receive Configuration Word Register [RXCW (00180h; R)] is set (1) and that there are no symbol errors by checking that bit 27 of RXCW is clear (0). If both partners support auto-negotiation this software check is not necessary as that process resolves the link process. However, in both cases link detect should be pulled up to 3.3 V dc.

Some devices might be capable of looking at the incoming stream of Rx symbols and determining link/synchronization status solely from the symbol content. However, when in internal SERDES mode, the Ethernet controller uses SIGDET as the primary indication of link up/down status.

Link status is a direct function of SIGDET regardless of whether HW auto-negotiation is enabled or not. Therefore, even if HW auto-negotiation is enabled, if SIGDET is not asserted, link up is not indicated.

In circumstances where SIGDET is connected to VCC and HW auto-negotiation is disabled, the Ethernet controller always reports that link is up.

2.1.4.3 Signal Reception

The receiver on the GbE controller must be able to receive any signal transmitted by a compliant transmitter through a compliant channel. For example, the GbE controller's link partner's transmitter must transmit signals that the GbE controller is capable of successfully receiving and deciphering through the backplane traces that meet the layout, length and other specifications as described in the PICMG 3.1 specification. Conversely, the link partner of the GbE controller must be capable of receiving and correctly understanding signals transmitted from the GbE controller. This requires verifying that the SERDES output and input of the GbE controller is compatible with its link partner's SERDES input and output respectively by carefully reviewing both parts' receiver and transmitter specifications.

Rigorous testing should then be performed on a prototype to verify that both parts and the signals transmitted minus losses are able to meet this receiver requirement. This testing should again be repeated on multiple finished product boards over all conditions that the finished product is subjected to such as supply voltage variations, ambient temperature variations, humidity, and etc. Failing to do this testing can result in failures of the product at a customer's site.

2.1.4.4 Pre-Emphasis

Pre-emphasis control is available in the Extended PHY Specific Control 2 Register (Address: 26), bit 13 in GbE controllers. With the default setting of (0) the transmitted differential output amplitude includes 7% pre-emphasis value and can be increased to 15% by setting bit 13 to (1). The benefits of pre-emphasis are in high-speed data rate applications across longer (>30 inches) backplane lengths with multiple connectors (> 2). When a high-speed signal is traveling through a long PCB trace, the signal is degraded due the electrical properties of the PCB trace. The higher the frequency and the longer the PCB trace, the higher the degradation due to the bandwidth limitation of the PCB trace. When the data rate is higher than the bandwidth of the PCB trace, degradation of the signal occurs.

Although the simple resolution might seem to be to increase the amplitude of the signal, this does not address the problem of signal roll off or pattern dependent jitter and tends to increase noise and power consumption. The pre-emphasis technique has been proven to be an effective way to reduce such effects, especially in backplane designs, because it boosts the high frequency energy whenever there is a transition in the data which is when most problems occur.

Since high frequency components are attenuated more than low frequency components this results in a more equalized eye pattern at the receiver making it easier for the receiver to decipher the signal. A combination of both adjusting the output voltage level and the pre-emphasis bit setting is useful when problems arise with receiving transmitted information assuming that the design meets the layout requirements in this document. With improper layout it is quite likely that it will not be possible to overcome the problem without correcting the layout.

3.0 82545GM/82546GB SERDES Specifications

3.1 Transmit and Receive Specifications

Table 2. SERDES Specifications

Parameter	Value
Transmit Measured at TP-T	
Data Rate	1000 Mb/s
Nominal Signal Speed	1250 MBd
Clock Tolerance	+/-100 ppm
Differential Output Amplitude (peak-to-peak)	750 - 1350 mV (Adjustable)
Return Loss	15 dB Maximum (at TP-1)
Impedance	100 +/- 10% Ωs
Total Jitter (Random and Deterministic)	<223 pS
Receive Measured at TP-R	
Data Rate	1000 Mb/s
Nominal Signal Speed	1250 MBd
Clock Tolerance	+/-100 ppm
Input Sensitivity	200 - 2000 mV
Differential Skew	175 pS Maximum
Differential Return Loss	15 dB Maximum
Common Mode Return Loss	6 dB Maximum (200 MHz to 2.5 GHz)
Impedance	100 +/- 10% Ωs
Fastest Rise Time	85 pS Maximum
Total Jitter (Random and Deterministic)	<528 pS

3.2 Device ID Specifications

For the 82546GB, the Device ID must be forced to 107Bh for SERDES-SERDES interface operation. For the 82545GM, the Device ID should be 1028h. This ensures proper functionality with Intel drivers and the boot agent.

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4.0 Testing for PICMG 3.1 Compliance

Thorough testing of the circuit is a fundamental requirement for all backplane designs. If resources are not available to perform these tests, outside contractors with these capabilities will be able to assist. While full PICMG 3.1 testing is optimal, the crucial tests for SERDES-SERDES backplane designs are listed here and in the PICMG 3.1 specification:

1. Insertion loss: Use a Vector Network Analyzer (VNA) to check insertion loss. It is also very useful to provide frequency domain measurements, measure impedance characteristics, transfer functions and various other losses in the channel.
2. Jitter: Jitter is tested as described in the PICMG specification using an eye pattern and a Signal Integrity Analyzer. Backplane jitter is specified in terms of both total jitter (TJ) and deterministic jitter (DJ):
 - a. $TJ = \text{sum of the peak-to-peak DJ and RJ (random jitter)}$
 - b. $RJ = \text{jitter generation from the several random processes}$
3. $DJ = \text{jitter from a variety of systematic effects (Duty Cycle Distortion, Inter Symbol Interference, periodic jitter).}$

The analyzers acquire signals and perform statistical analysis to separate DJ & RJ from TJ. Some scopes can also be used for eye diagram and jitter analysis. Such scopes provide the masks for Eye Diagrams.

4. Bit Error Rate (BER): The BER provides a good indication of real world network performance. BER testing should be performed with the length of backplane desired and several link partners. The test limit is 10-12 for any size of frame. BER is measured with a Bit Error Ratio Tester (BERT) available from several manufacturer of network test equipment. A BERT is used to create the “stressed eye” or worst-case packet waveform as seen by the receiver. Stressed eye includes both worst-case waveform amplitude and edge variation. BER can also be measured using the Intel® gigabit IEEE conformance test kit which includes the software, pattern files and suggested test setups to perform BER testing. Contact your Intel FAE to obtain this kit.
5. Return loss: Use a vector network analyzer to check return loss.

4.0.1 PICMG Test Setup and Specifications

1000BASE-BX is the PICMG electrical specification for transmission of 1000BASE-X encoded data over a $100\text{-}\Omega$ backplane. The test points TP-T and TP-R are mandatory compliant points. All specifications are differential (see Figure 4).

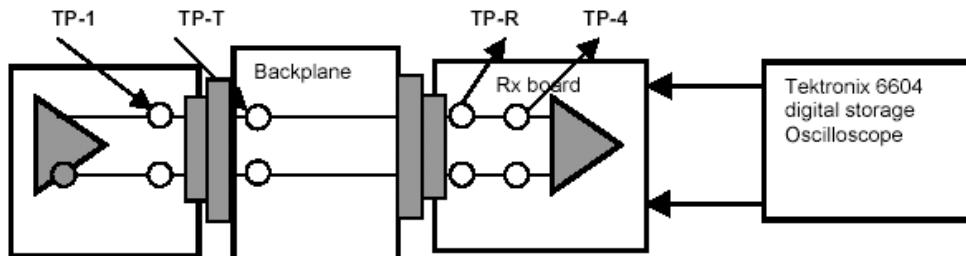


Figure 4. SERDES Ethernet Electrical Environment and Test Points

Confirm that the input impedance at connection TP-1 in Figure 4 is $100 \pm 30 \Omega$ and at connection TP-1 is $100 \pm 10 \Omega$ and $100 \pm 30 \Omega$ at TP-T.

Transmitted Electrical Specification at TP-T

- The output driver is assumed to have output levels supporting the PICMG 3.1 test point (TP-T).
- The test point is the backplane side of the mated HM-ZD connector as shown in Figure 5.

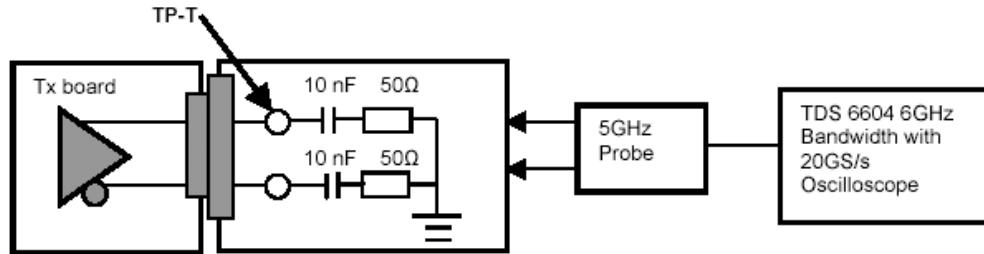


Figure 5. Transmit Test Point at TP-T

Note: Capacitor and resistor tolerance is $\pm 1\%$.

Transmitter Testing at TP-T

1. Differential output amplitude (peak-to-peak)
2. Rise/Fall time (20%-80%)
3. Differential skew
4. Normalized eye diagram mask at TP-T
5. Absolute eye diagram mask at TP-T
6. Transmitted total jitter and deterministic jitter

Note: Maximum drive amplitude of any PICMG 3.1 driver must not exceed 1600 mV peak-to-peak.

Table 3. Transmitter Specifications at TP-T

Test Parameter	PICMG 3.1 Value
Differential Output Amplitude (peak-to-peak)	750 - 1350 mV
Rise Time (20% - 80%)	85 - 327 pS
Fall Time (20% - 80%)	85 - 327 pS
Differential Skew (Maximum)	25 pS

Table 4. Transmitted Eye Diagram Mask Specification at TP-T

Test Parameter	PICMG 3.1 Eye Diagram Mask Requirement	
Normalized Eye Diagram Mask	Normalized Amplitude	Normalized Time (UI)
	0.2 - 0.8	X1 (0.14), X2 (0.34)
Absolute Eye Diagram Mask	Differential Amplitude (mV)	Normalized Time (UI)
	325 ~(-325)	X1 (0.14), X2 (0.34)

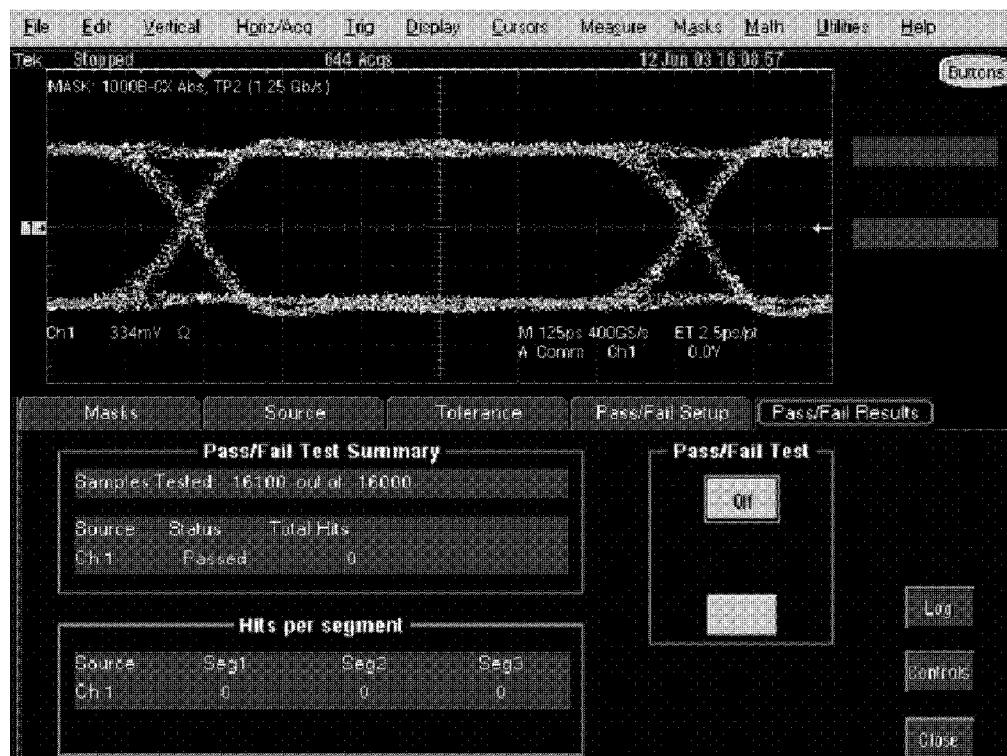
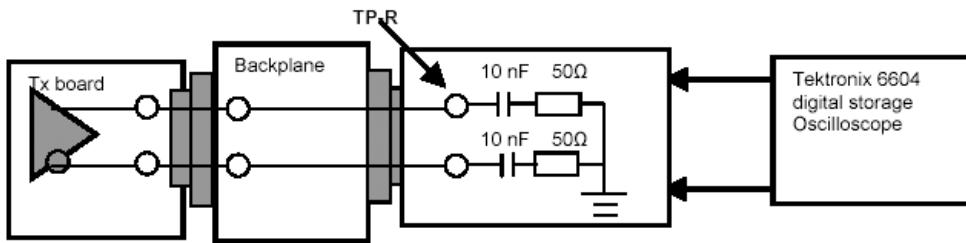

Figure 6. Absolute Transmit Eye Diagram Mask at TP-T

Table 5. Transmitted Jitter Specifications at TP-T

PICMG 3.1 Transmit Jitter Budget				
Parameter	Total Jitter		Deterministic Jitter	
	UI	PS	UI	PS
Data TIE	0.279	223	0.14	112
Data PLL TIE	0.279	223	0.14	112
Clock TIE	0.279	223	0.14	112
Clock PLL TIE	0.279	223	0.14	112

Receiver Electrical Specifications at TP-R

The receiver is AC-coupled to the media through a receiver network. The receive network terminates the Tx/Rx connection by an equivalent impedance of $100\ \Omega$, as specified in Figure 7.

**Figure 7. Receiver Testing**

1. Received differential skew (max) at TP-R
2. Received input sensitivity at TP-R
3. Received eye diagram mask at TP-R
4. Bit error rate (BER) testing at TP-R
5. Received total jitter and deterministic jitter

Table 6. Received Eye Diagram Mask Specification at TP-R

PICMG 3.1 Receive Eye Diagram Mask Requirement		
Backplane Eye Mask Test	Differential Amp (mV)	Normalized Time (UI)
	100~(-100)	0.3, 0.5, and 0.7

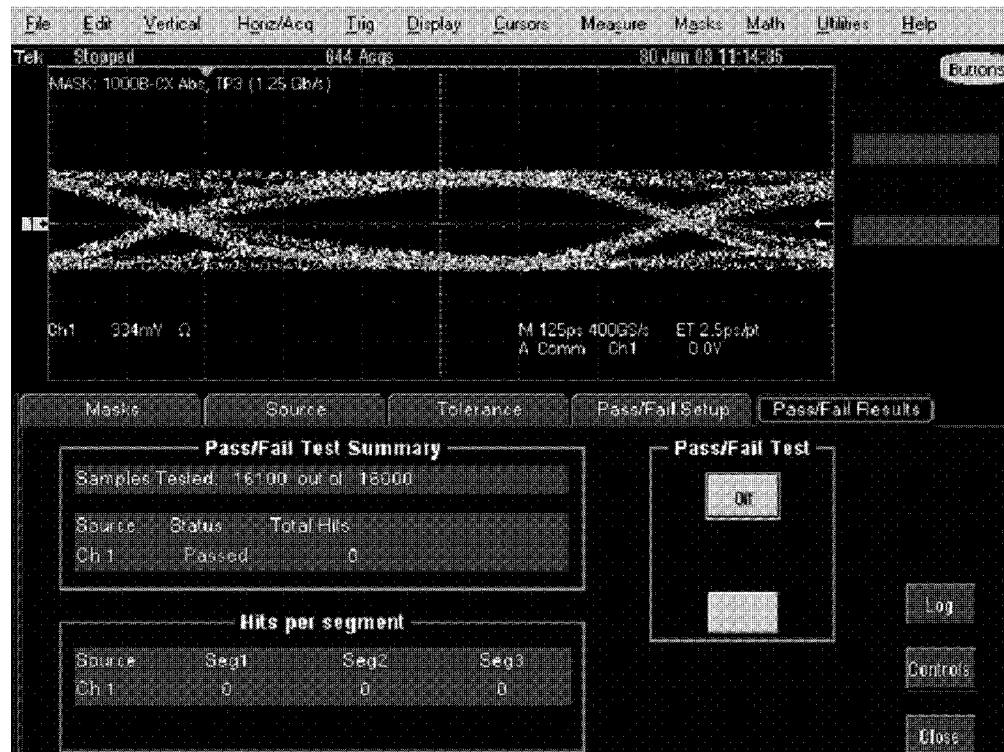


Figure 8. Received Eye Mask at TP-R After 25-Inch Backplane

Table 7. Received Input Specifications at TP-R

PICMG 3.1 Receive Specifications				
Sensitivity		200 to 1350 mV		
Differential Skew		175 pS		
Jitter Budget		Total Jitter		Differential Jitter
		UI	PS	UI
Data TIE	0.66	528	0.4	320
Data PLL TIE	0.66	528	0.4	320

Anasoft® provides a complete signal integrity simulation package, linking mechanical drawings to electrical simulation packages to board layouts for 3-D field solver analysis.

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5.0 Software Interface

There are a variety of applications that use GbE SERDES for its cost saving benefits. However, designers must carefully select components that provide the required performance. The GbE controllers were designed to be compliant with the PICMG 3.1 specifications and thus minimize risk of a backplane design. As a general rule, backplane designs should be kept as short as possible due to signal degradation in long traces, especially when using FR4 fabric for the PCB.

Other less “lossy” PCB materials, such as “Rogers”, are available but these can be more costly than FR4. When making design trade-offs to save costs, designers need to understand the impact on the performance and overall back plane design. This means careful attention to layout to maintain the $100\ \Omega$ differential impedance and testing thoroughly both on the prototype and the final production boards. Should the backplane exceed 30 inches there is much more likelihood that signal degradation may be too great to compensate, even with amplitude adjustment -- especially on FR4 PCB material.

Also, using connectors of a lower quality than HM-Zd type can increase signal distortion. With shorter backplanes, there should be less trace signal degradation and the design might be able to afford slightly more signal degradation at the connector. In all cases, customers should perform thorough testing to ensure the critical components on multiple boards thorough all the conditions meet the requirements in their final application(s). The PICMG 3.1 specification is a valid reference for this compliance testing.

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6.0 References

It is assumed that the designer is acquainted with high-speed design and board layout techniques. Documents that might provide additional information are:

- 82546GB Dual Port Gigabit Ethernet Controller Datasheet.
- 82545GM Dual Port Gigabit Ethernet Controller Datasheet.
- 82545EM, 82545GM, 82546EB and 82546GB Gigabit Ethernet Controllers Design Guide, Application Note.
- PICMG® 3.1 Ethernet/Fibre Channel Over PICMG 3.0 Specification.

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7.0 Reference Schematics

This section contains reference schematics for the 82546GB Gigabit Ethernet controller.

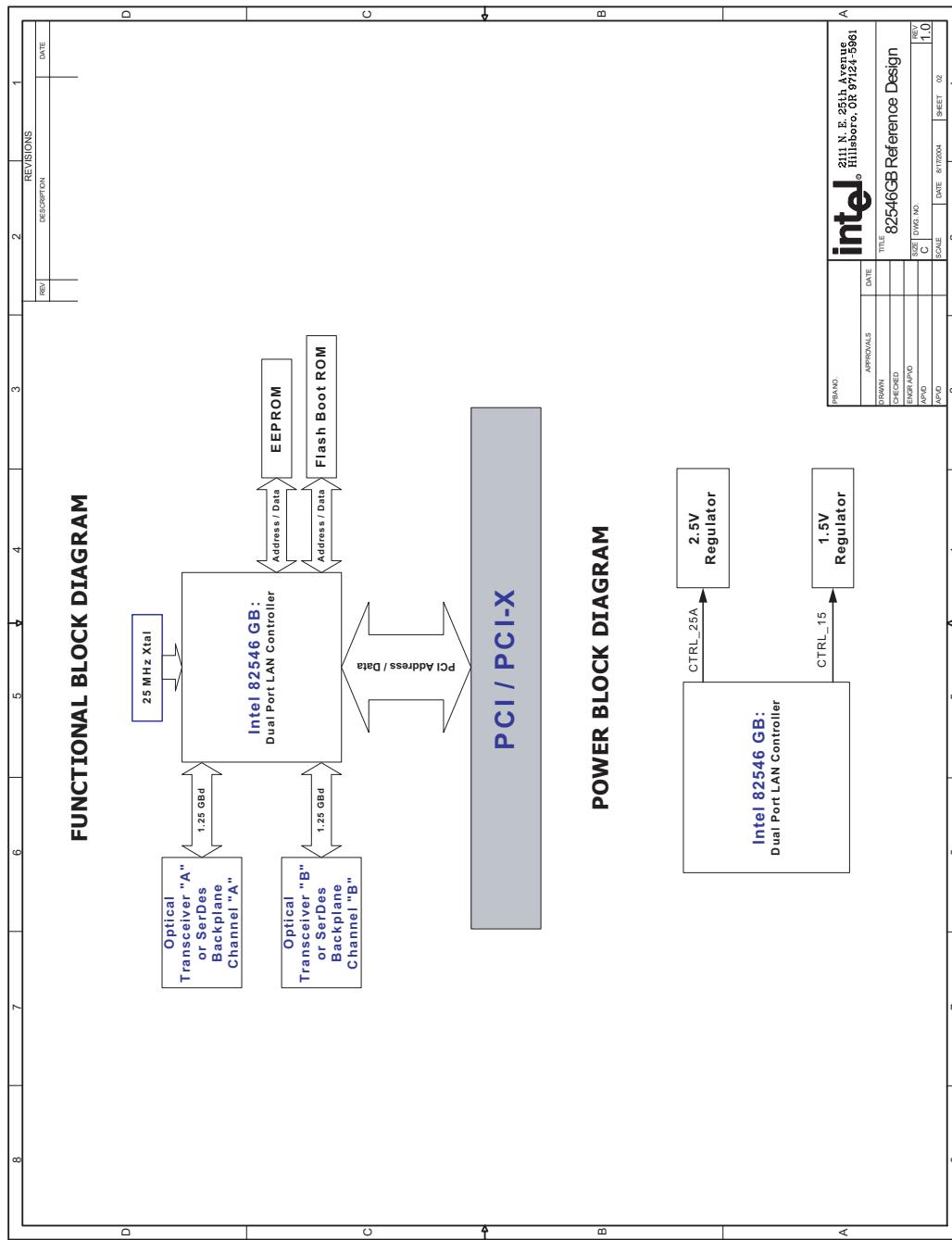
82546GB REFERENCE DESIGN (SERDES/FIBER)

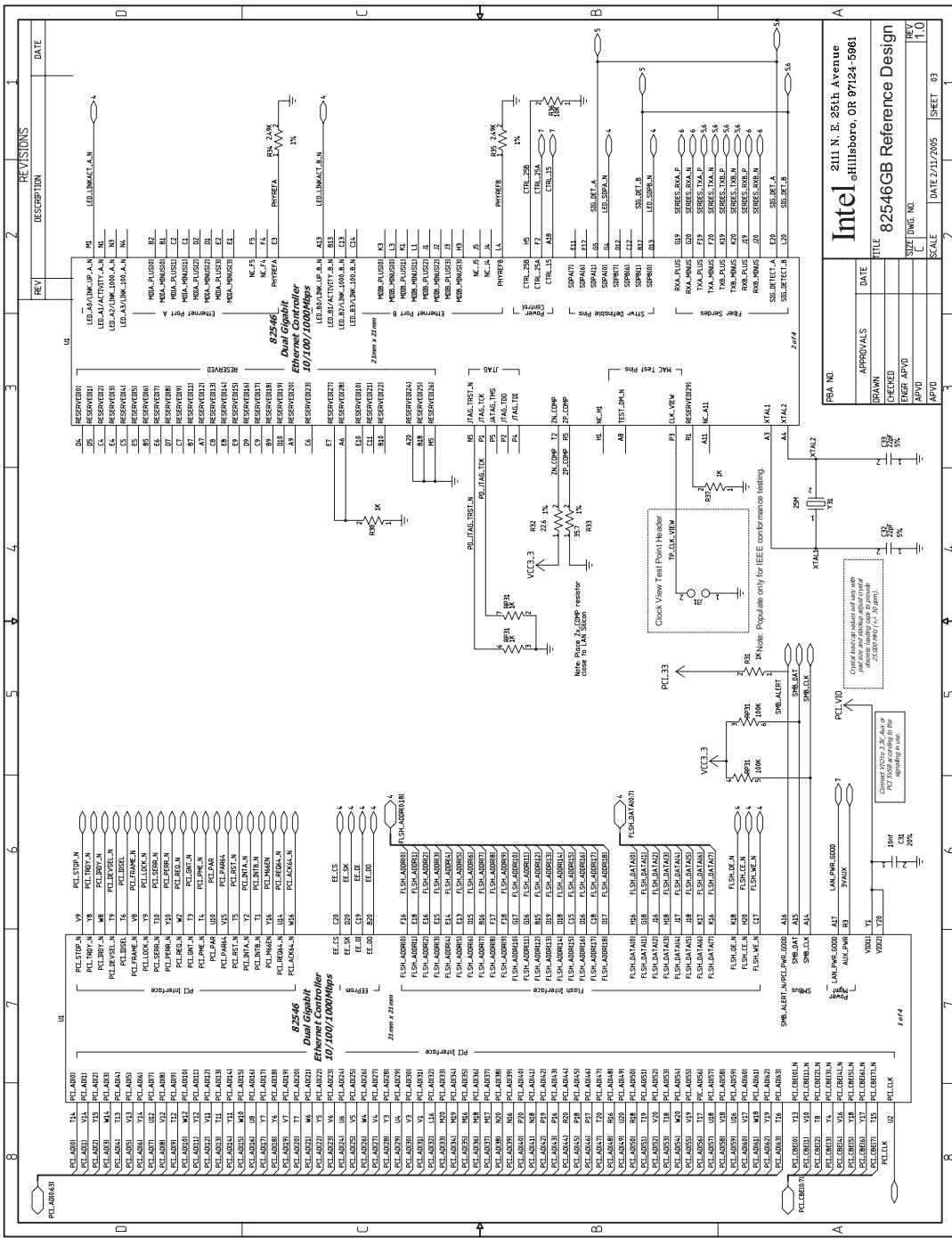
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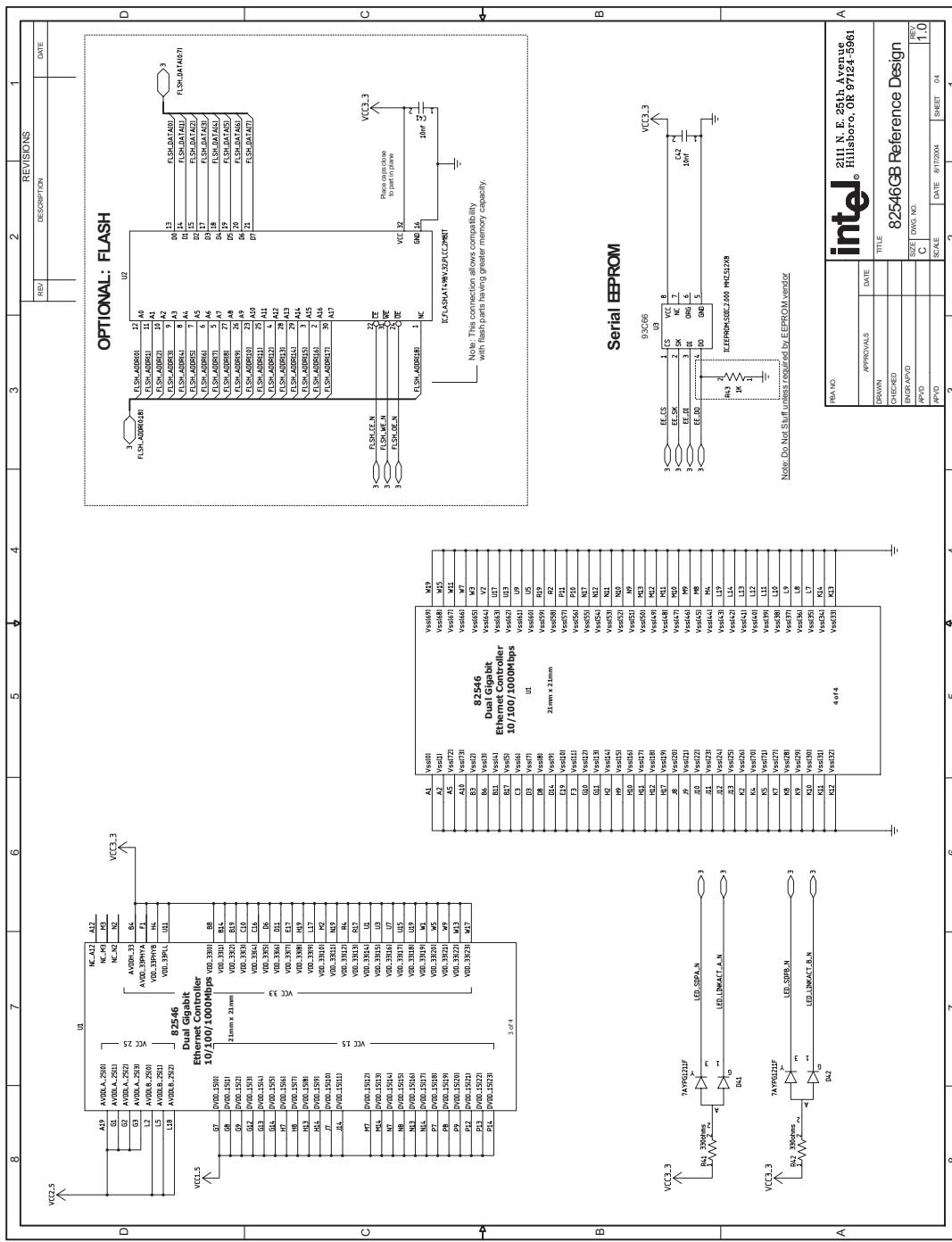
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PBA NO. APPROV/ALS DRAWN CHECKED ENGR/APV'D APV'D	DATE SIZE DWG. NO. C SCALE REV. 01
TITLE 82546GB Reference Design	
A	
3 - RJ45 10Gb LAN Controller (1/2) 4 - 82546GB LAN Controller (2/2), EEPROM, Flash 5 - FIBER Laser connections 6 - Voltage Regulators 7 - SERDES Backplane Connections 8 - Decoupling	

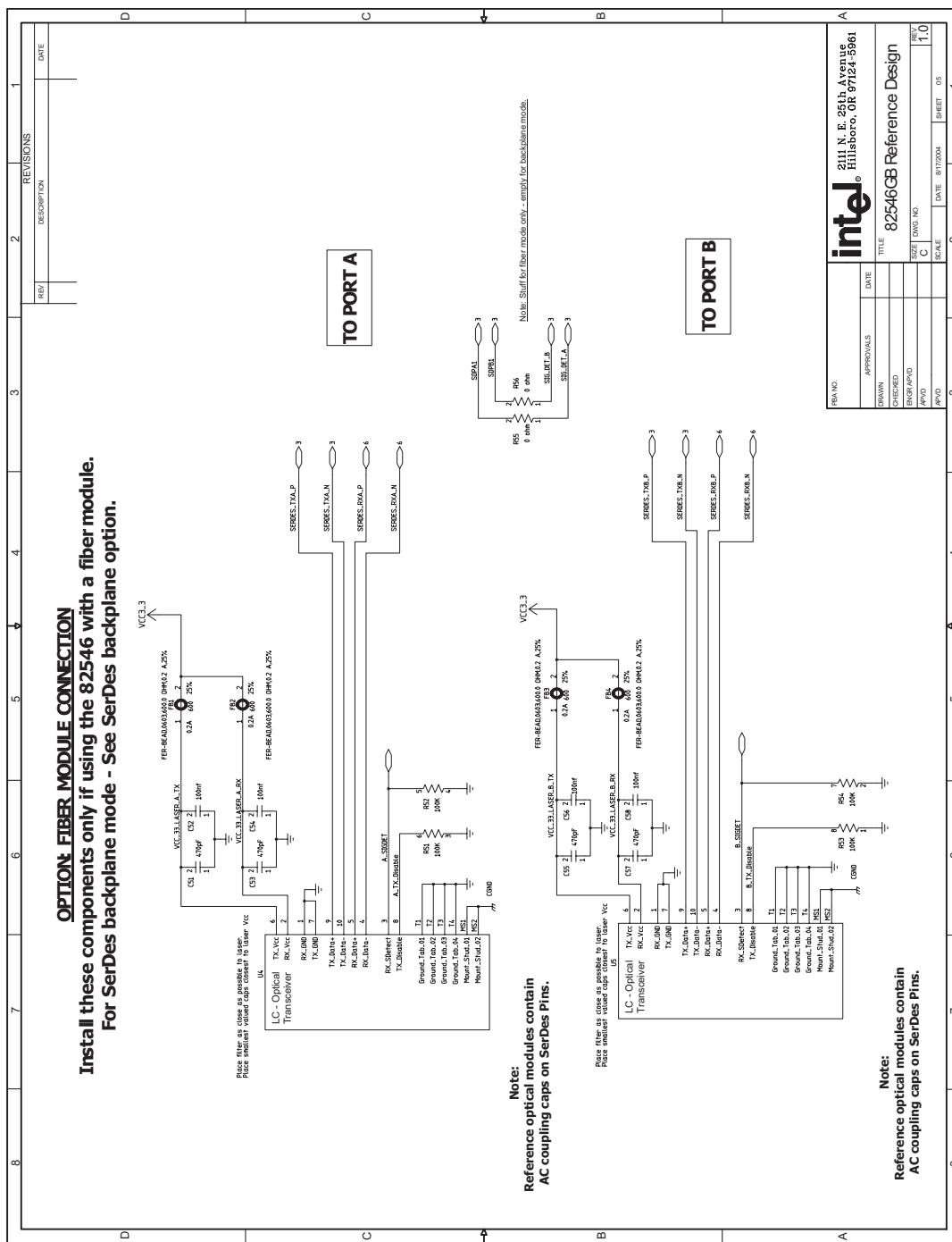
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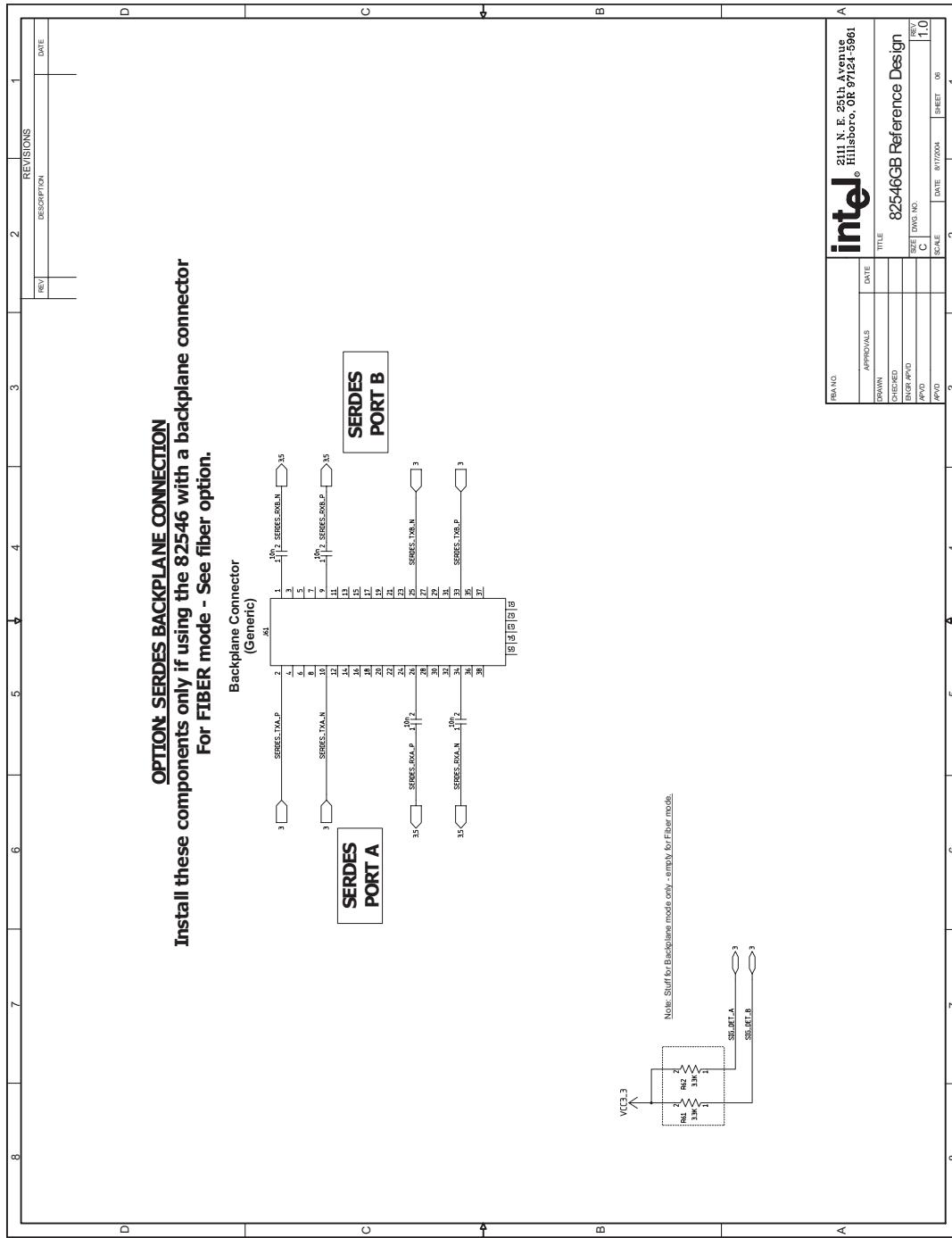
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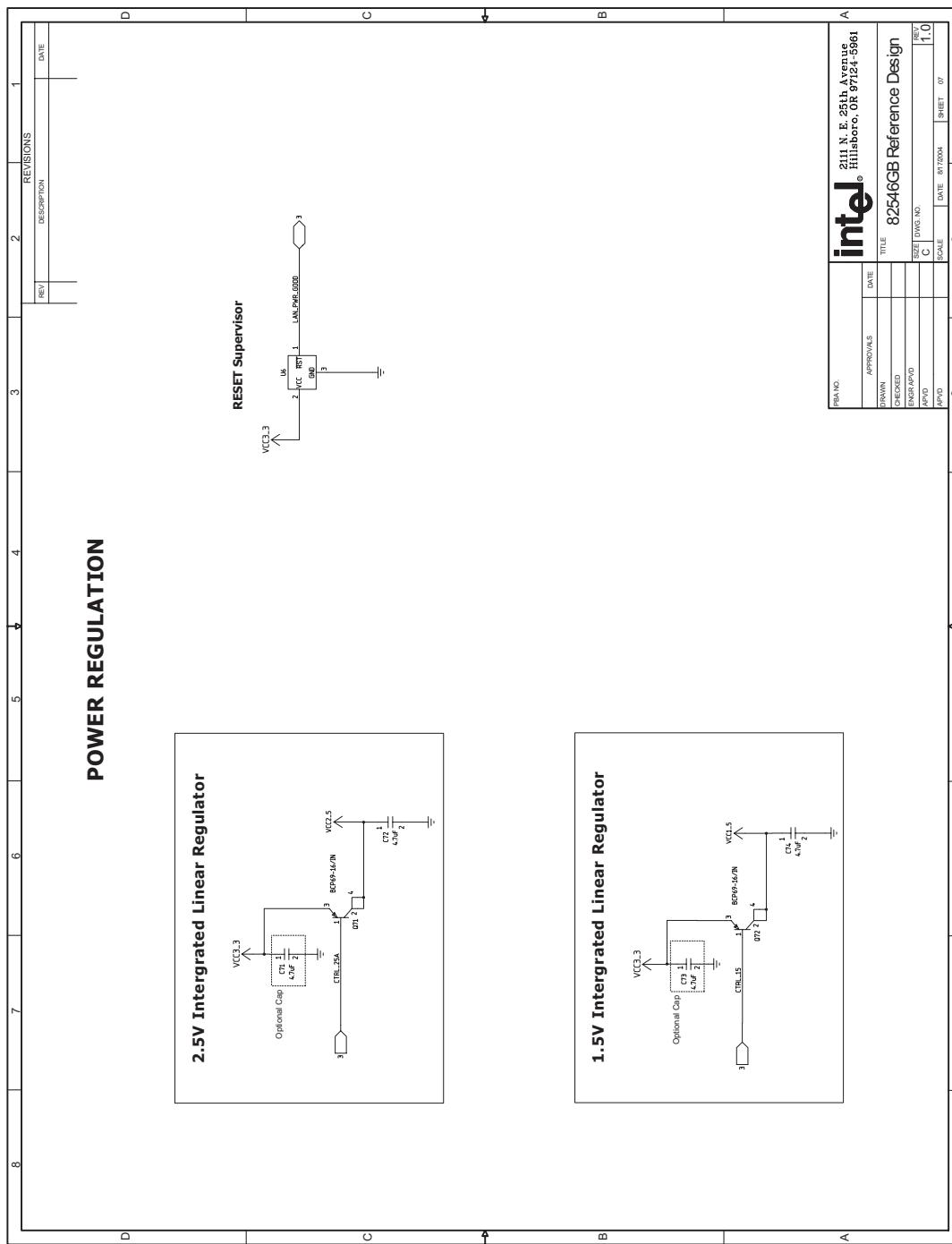


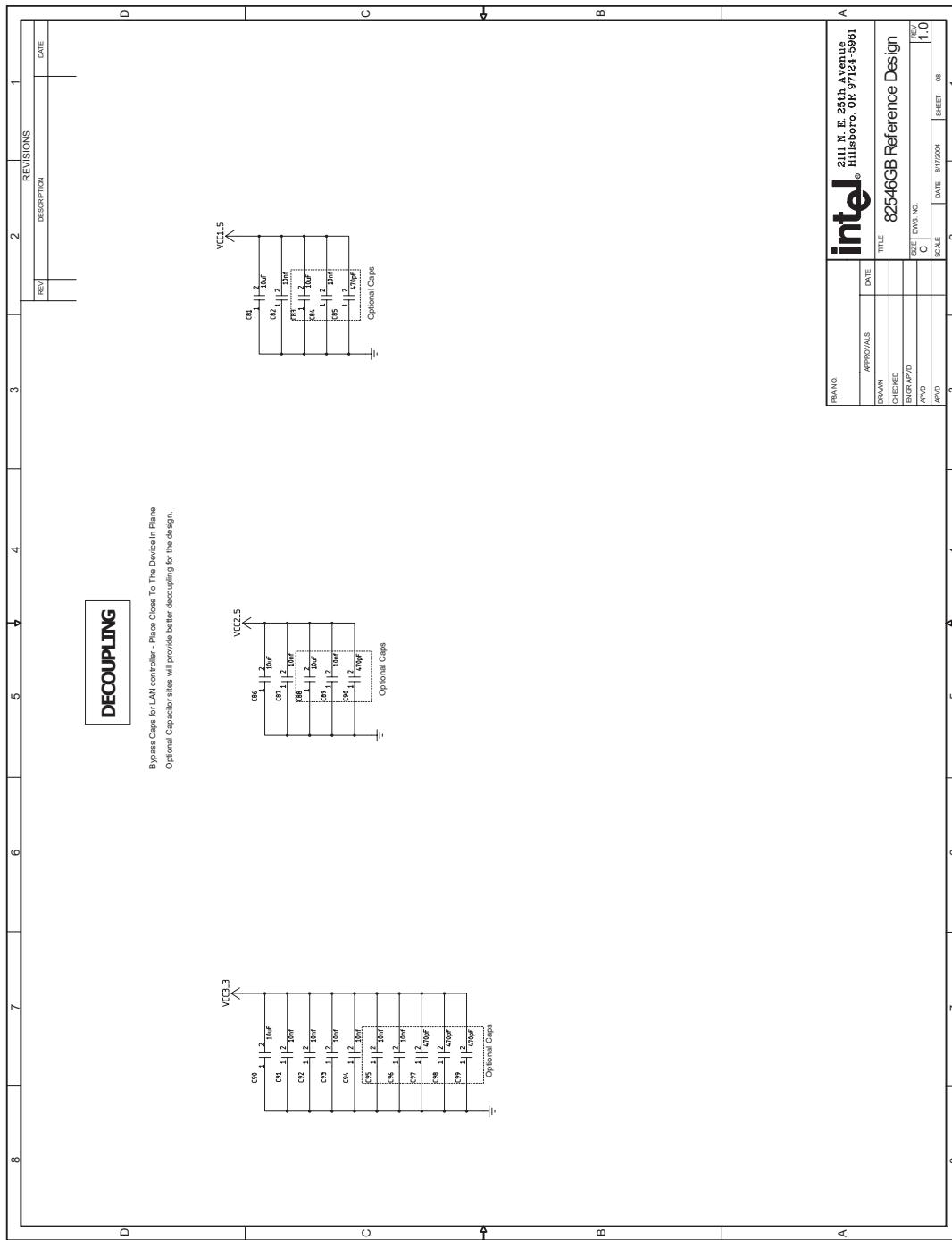












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