IDF2012
INTEL DEVELOPER FORUM

Intel® Transactional Synchronization Extensions

Ravi Rajwar, CPU Architect, Intel
Martin Dixon, Principal Engineer, Intel

ARCS004

Agenda

- The Synchronization Problem
- Intel® Transactional Synchronization Extensions
- Implementation Insights‡
- Software Enabling and Considerations
- Summary

‡ For the next generation Intel® microarchitecture (Haswell)

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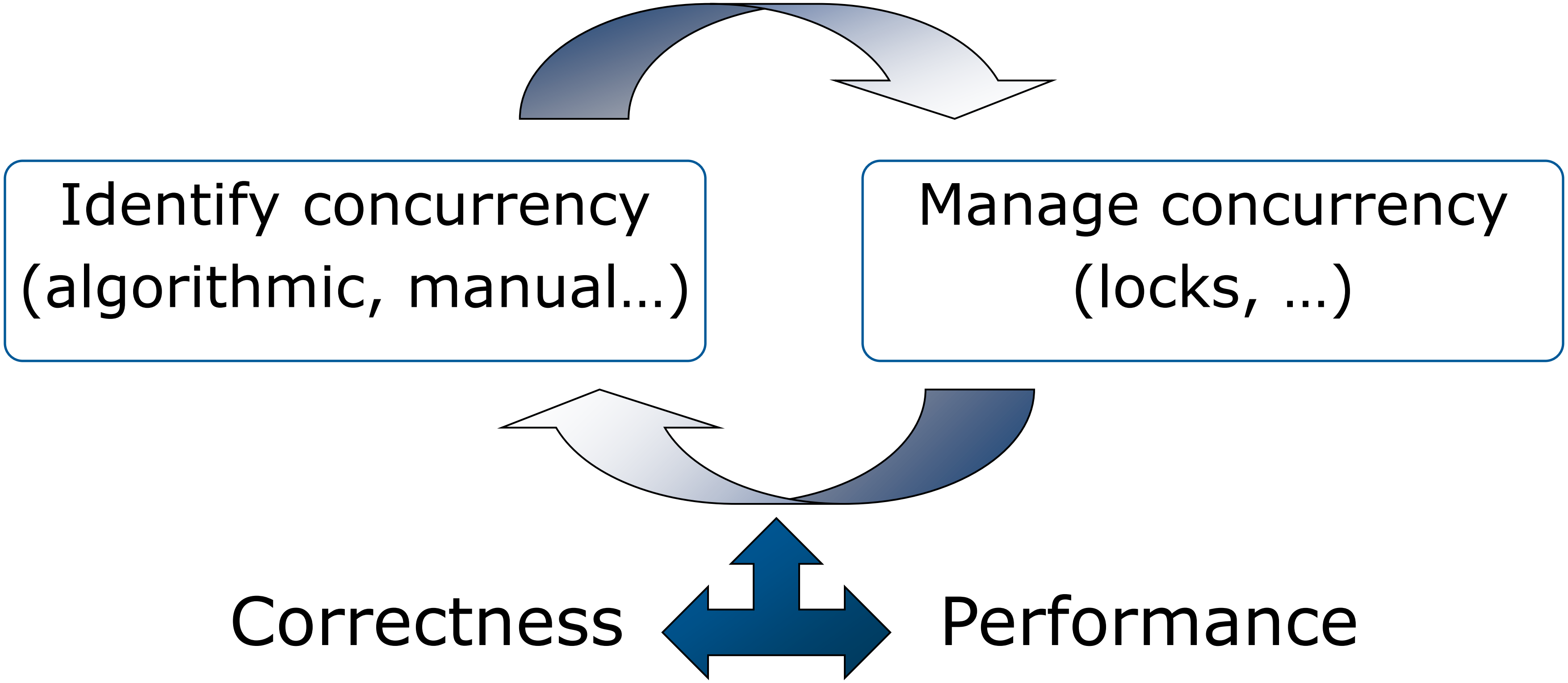
Difficulty of Software Development



Identify concurrency (algorithmic, manual…)

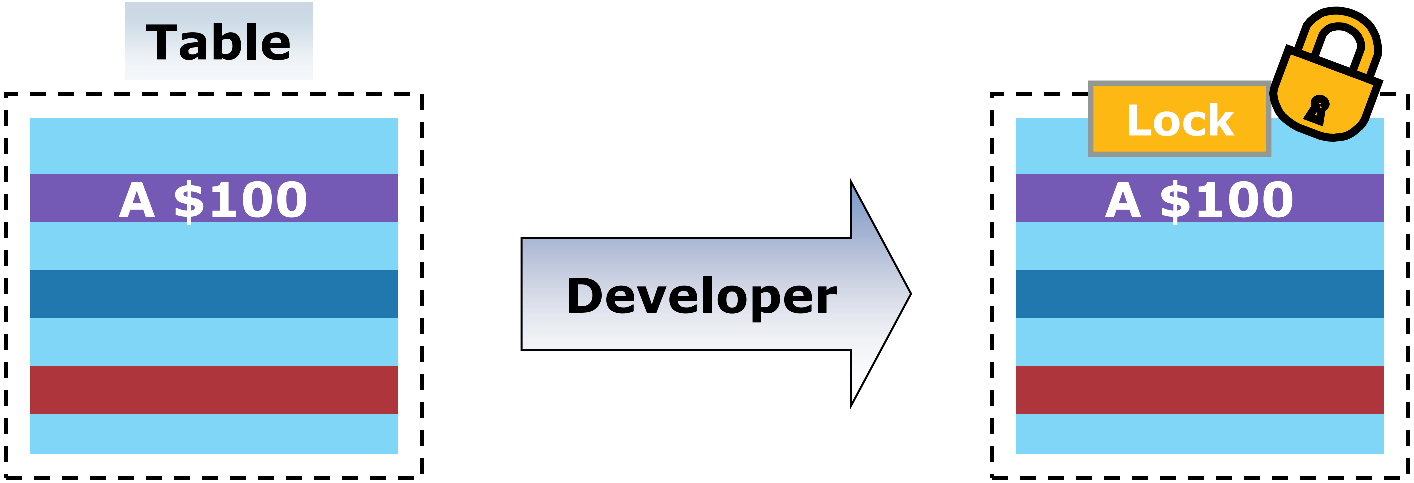
Manage concurrency (locks, …)

Correctness

Performance

Hard to Write Fast and Correct Multi-Threaded Code

The Need for Synchronization



Alice wants $50 from A

- A was $100, A is now $50

Bob wants $60 from A

- A was $100, A is now $40

A should be -10

Alice wants $50 from A

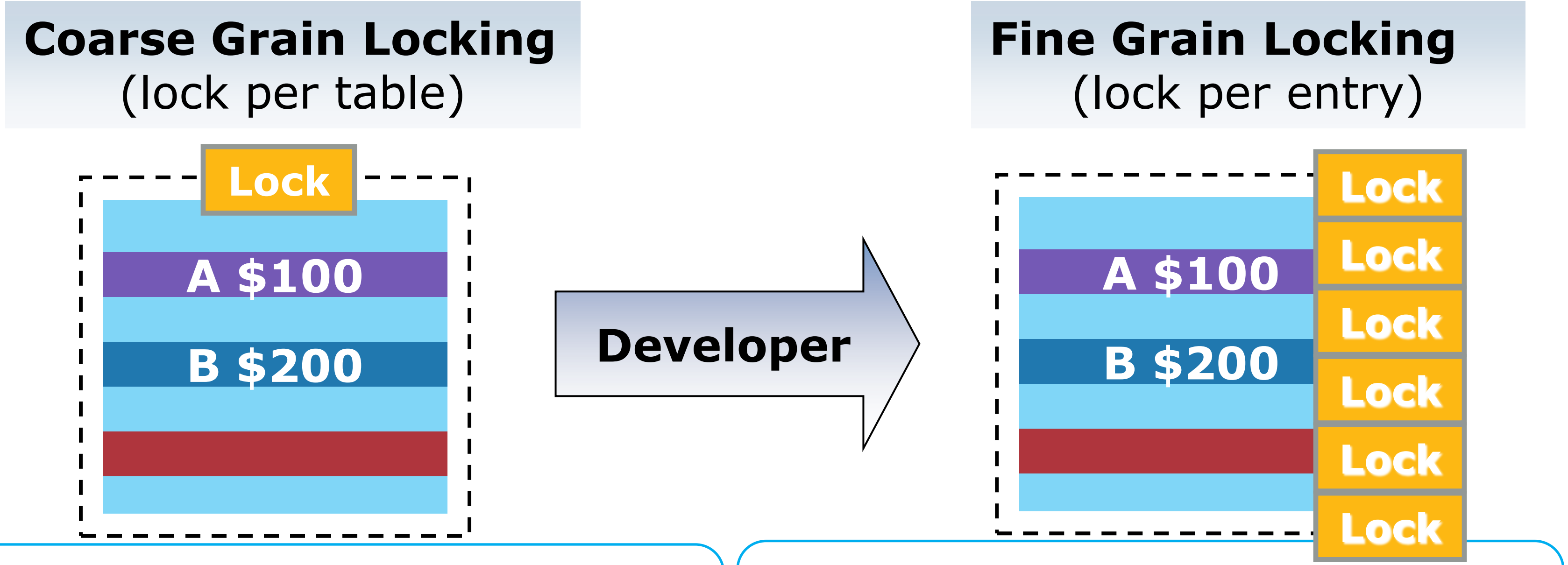
- Alice locks table
- A was $100, A is now $50

Bob wants $60 from A

- Bob waits till lock release
- A was $50, Insufficient funds

Bob and Alice saw A as $100. Locks prevent such data races

Lock Granularity Optimization



Alice withdraws $20 from A

- Alice locks table

Bob wants $30 from B

- Waits for Alice to free table

Alice withdraws $20 from A

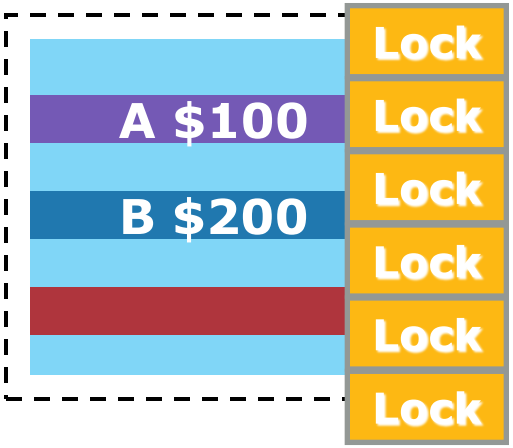
- Alice locks A

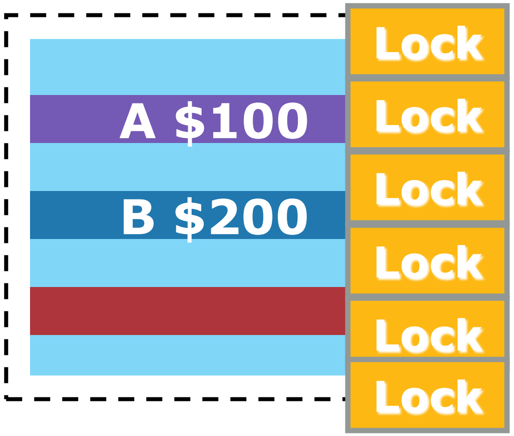
Bob wants $30 from B

- Bob locks B

Such Tuning is Time Consuming and Error Prone

Complexity of Fine Grain Locking





Alice transfers $20 from A to B

- Alice locks A and locks B

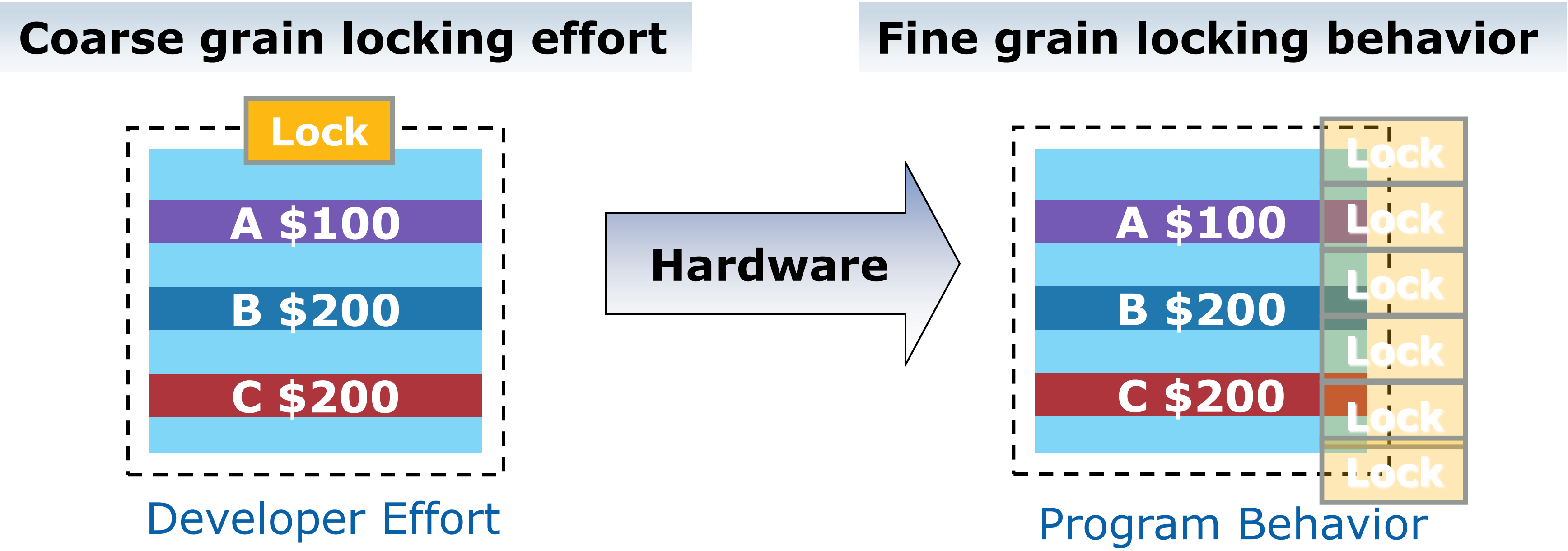
Performs transfer

- Alice unlocks A and unlocks B

Alice transfers $20 from A to B	Bob transfers $50 from B to A
Locks A	Locks B
Cannot lock B	Cannot lock A

Expensive and Difficult to Debug Millions of Lines of Code

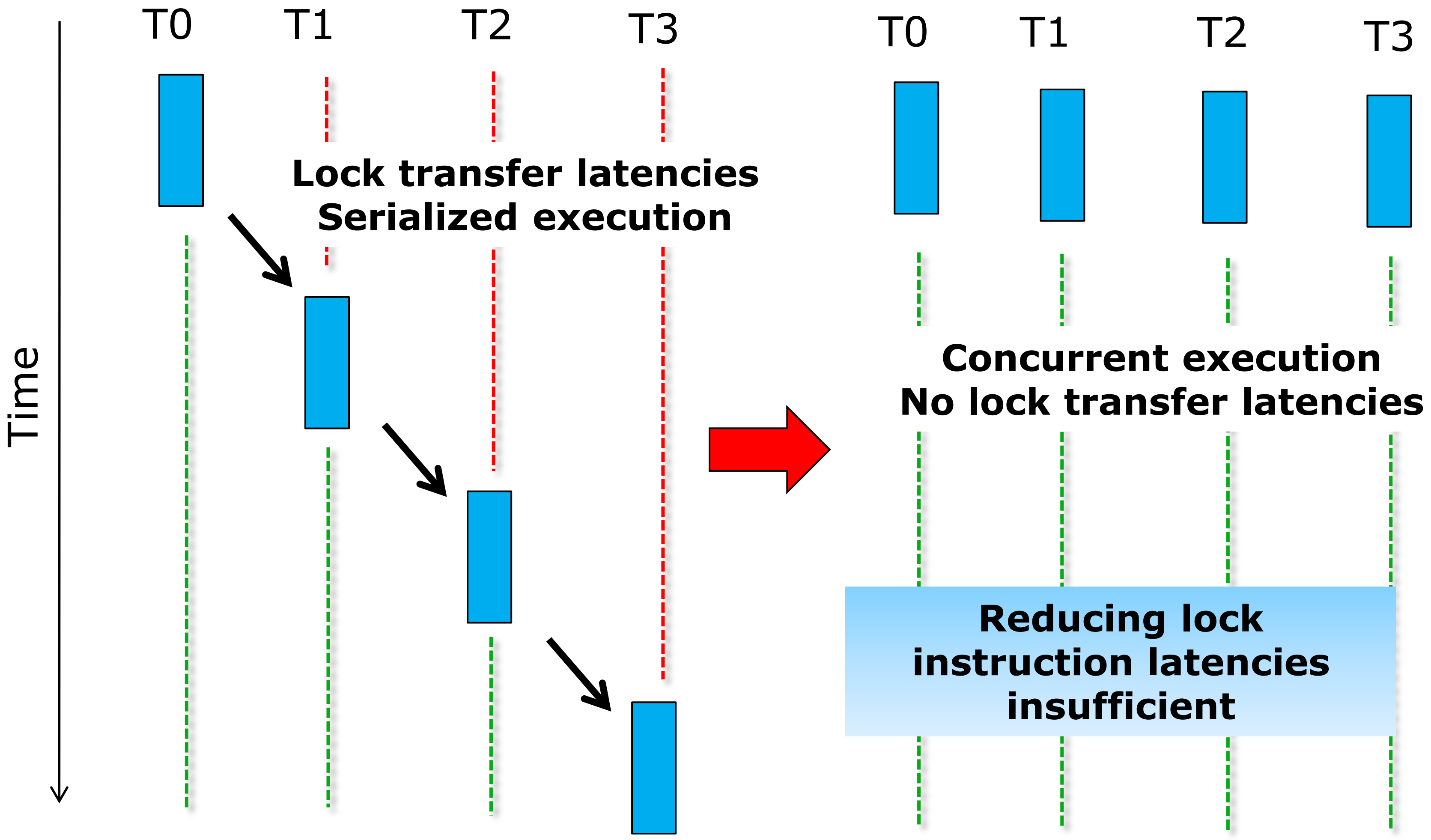
What We Really Want…



- Developer uses coarse grain lock
- Hardware elides the lock to expose concurrency
  - Alice and Bob don’t serialize on the lock
  - Hardware automatically detects real data conflicts

Lock Elision: Fine Grain Behavior at Coarse Grain Effort

Benefit of Lock Elision



Lock transfer latencies
Serialized execution

Concurrent execution
No lock transfer latencies

Reducing lock instruction latencies insufficient

Exposes Concurrency & Eliminates Unnecessary Communication

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Transactional Synchronization

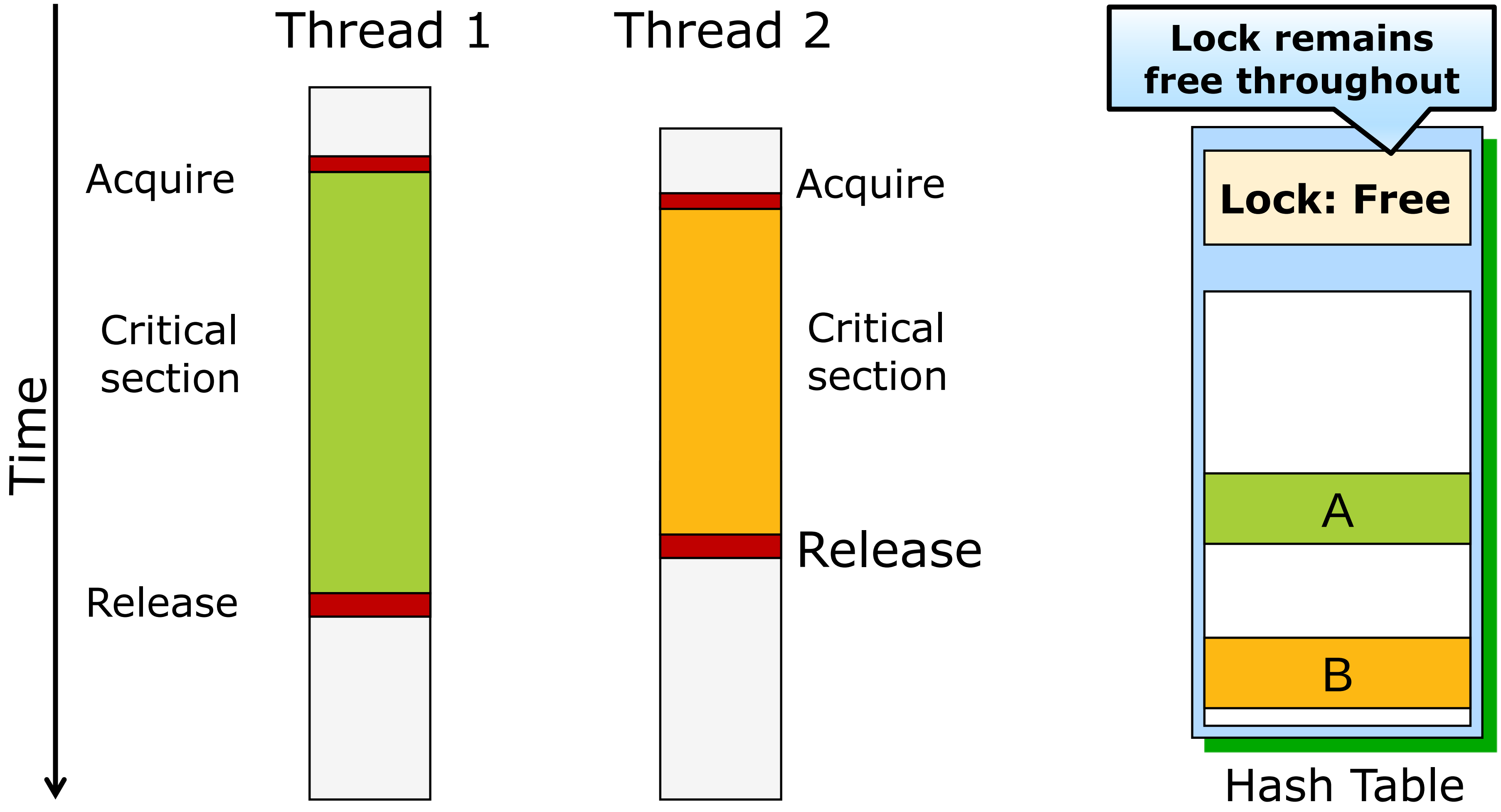
- **Hardware support to enable lock elision**
  - Focus on lock granularity optimizations
  - Fine grain performance at coarse grain effort
- **Intel® TSX: Instruction set extensions for IA‡**
  - Transactionally execute lock-protected critical sections
  - Execute without acquiring lock → expose hidden concurrency
  - Hardware manages transactional updates – All or None
    - Other threads can't observe intermediate transactional updates
    - If lock elision cannot succeed, restart execution & acquire lock

Intel® TSX Exposes Concurrency through Lock Elision

‡Intel® Architecture Instruction Set Extensions Programming Reference (http://software.intel.com/file/41604)

Intel® Transactional Synchronization Extensions (Intel® TSX)

A Canonical Intel® TSX Execution



Lock remains free throughout

No Serialization and No Communication if No Data Conflicts

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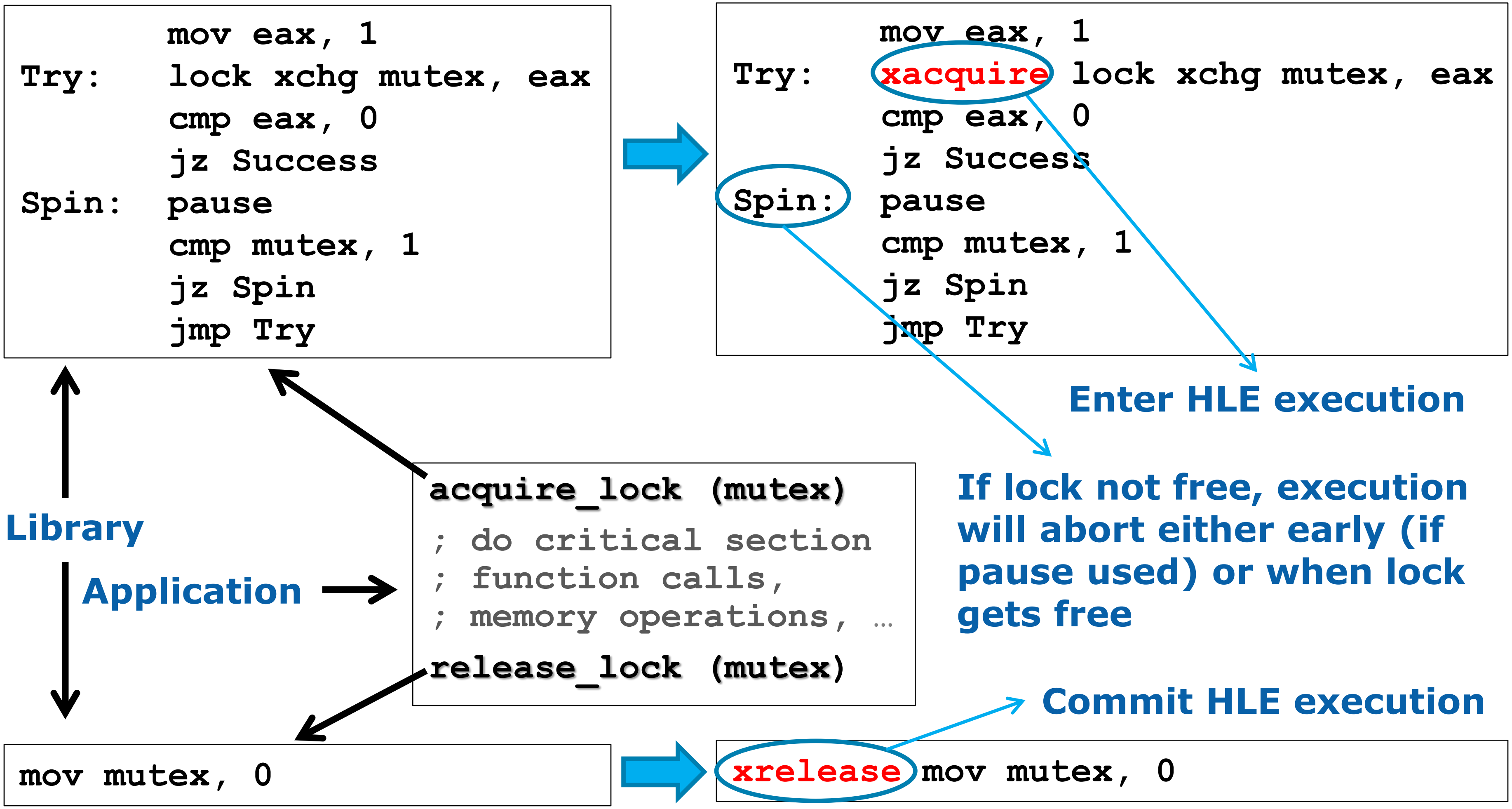
Intel® TSX Interfaces for Lock Elision

- **Hardware Lock Elision (HLE) – XACQUIRE/XRELEASE**
  - Software uses legacy compatible hints to identify critical section. Hints ignored on hardware without TSX
  - Hardware support to execute transactionally without acquiring lock
  - Abort causes a re-execution without elision
  - Hardware manages all architectural state
- **Restricted Transactional Memory (RTM) – XBEGIN/XEND**
  - Software uses new instructions to specify critical sections
  - Similar to HLE but flexible interface for software to do lock elision
  - Abort transfers control to target specified by XBEGIN operand
  - Abort information returned in a general purpose register (EAX)
- **XTEST and XABORT – Additional instructions**

Flexible and Easy To Use

Intel® TSX Interface: HLE



```
        mov eax, 1
Try:    lock xchg mutex, eax
        cmp eax, 0
        jz Success
Spin:   pause
        cmp mutex, 1
        jz Spin
        jmp Try
```

```
        mov eax, 1
Try:    xacquire lock xchg mutex, eax
        cmp eax, 0
        jz Success
Spin:   pause
        cmp mutex, 1
        jz Spin
        jmp Try
```

Enter HLE execution

If lock not free, execution will abort either early (if pause used) or when lock gets free

Library

Application

```
acquire_lock (mutex)
; do critical section
; function calls,
; memory operations, …
release_lock (mutex)
```

Commit HLE execution

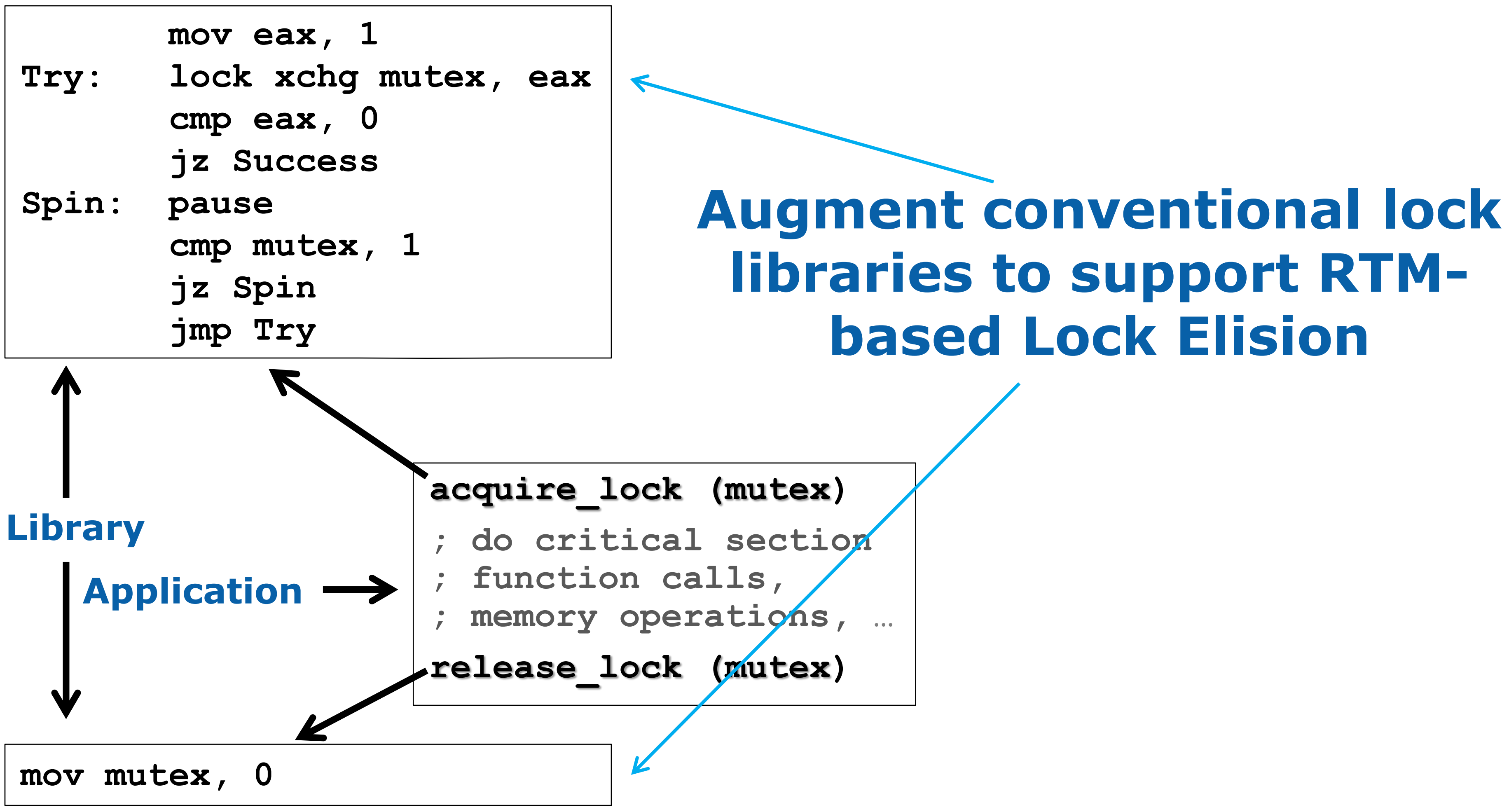
```
mov mutex, 0
```

```
xrelease mov mutex, 0
```

Legacy Compatible Enabling Within Libraries

Code example for illustration purpose only

Intel® TSX Interface: RTM



```
        mov eax, 1
Try:    lock xchg mutex, eax
        cmp eax, 0
        jz Success
Spin:   pause
        cmp mutex, 1
        jz Spin
        jmp Try
```

Augment conventional lock libraries to support RTM-based Lock Elision

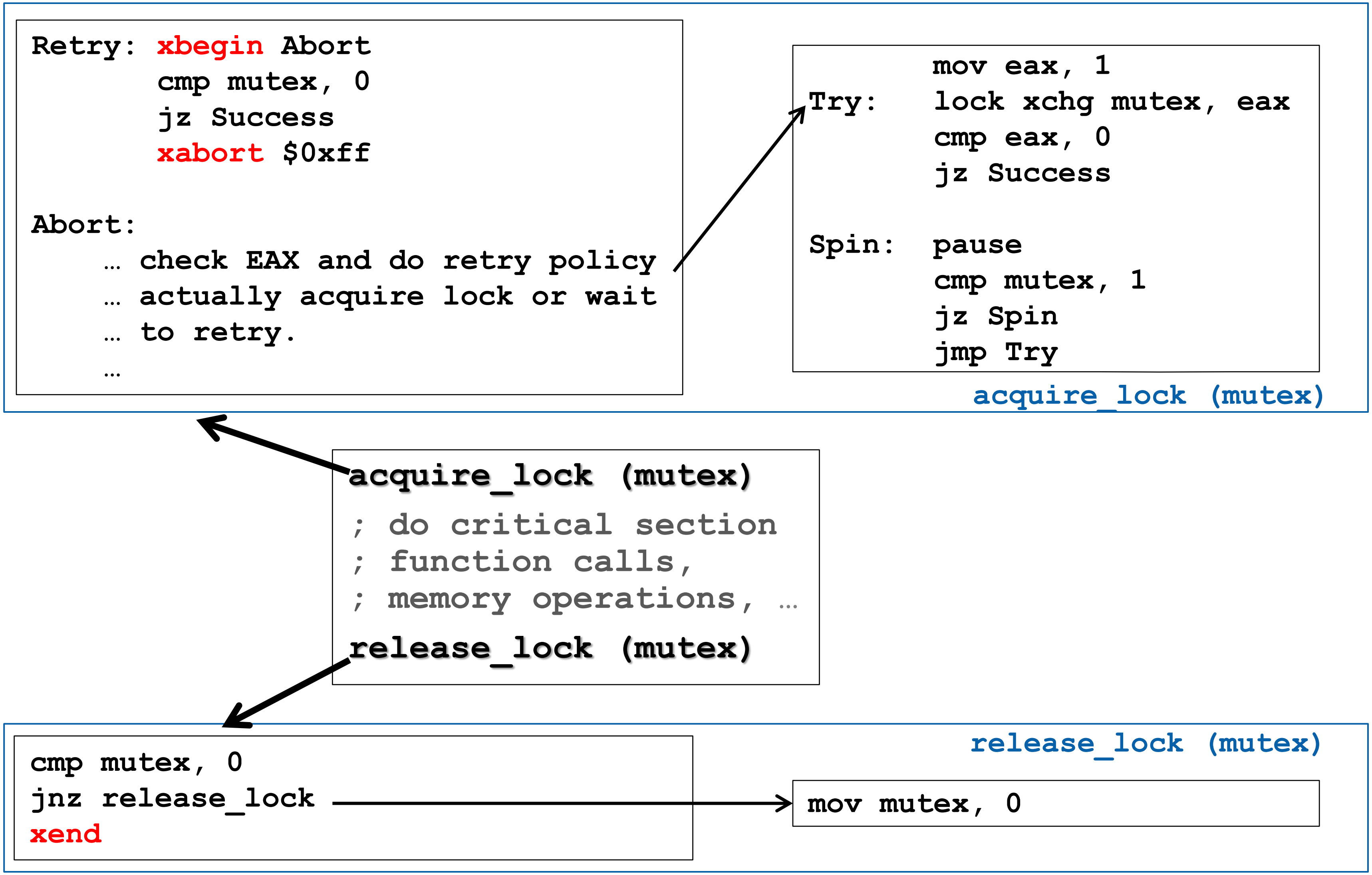
```
acquire_lock (mutex)
; do critical section
; function calls,
; memory operations, …
release_lock (mutex)
```

```
mov mutex, 0
```

Lock Elision using RTM Also Enabled Inside Libraries

Code example for illustration purpose only

Intel® TSX Interface: RTM



```
Retry: xbegin Abort
       cmp mutex, 0
       jz Success
       xabort $0xff

Abort:
    … check EAX and do retry policy
    … actually acquire lock or wait
    … to retry.
    …
```

```
        mov eax, 1
Try:    lock xchg mutex, eax
        cmp eax, 0
        jz Success

Spin:   pause
        cmp mutex, 1
        jz Spin
        jmp Try
```

acquire_lock (mutex)

```
acquire_lock (mutex)
; do critical section
; function calls,
; memory operations, …
release_lock (mutex)
```

release_lock (mutex)

```
cmp mutex, 0
jnz release_lock
xend
```

```
mov mutex, 0
```

Code example for illustration purpose only

Intel® TSX Interface: RTM

```
Retry: xbegin Abort
       cmp mutex, 0
       jz Success
       xabort $0xff

Abort:
     … check EAX and do retry policy
     … actually acquire lock or wait
     … to retry.
     …
```

… Enter RTM execution, Abort is fallback path

… Check to see if mutex is free

… Abort transactional execution if mutex busy

… Fallback path in software

… Retry RTM or explicitly acquire mutex

```
acquire_lock (mutex)
; do critical section
; function calls,
; memory operations, …
release_lock (mutex)
```

```
cmp mutex, 0
jnz release_lock
xend
```

… Mutex not free →was not an RTM execution

… Commit RTM execution

Code example for illustration purpose only

Intel® TSX Usage Environment

- **Available in all x86 modes**
- **Some instructions and events may cause aborts**
  - Uncommon instructions, interrupts, faults, etc.
  - Always functionally safe to use any instruction
- **Software must provide a non-transactional path**
  - HLE: Same software code path executed without elision
  - RTM: Software fallback handler must provide alternate path

Architected for Typical Lock Elision Usage

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‡ For the next generation Intel® microarchitecture (Haswell)

Focus: Simplify Developer Enabling

- **Easy to start using Intel® TSX**
  - Simple and clean instruction set minimizes software changes
    - Can be hidden in software synchronization libraries
    - Supports nesting critical sections
  - Minimizes implementation-specific causes for aborts
    - Micro-architectural events such as branch mispredicts, cache misses, TLB misses, etc. do not cause aborts
    - No explicit limit on number of instructions inside critical section
- **Simplify decision process of when to use**
  - Designed to support typical critical sections
  - Competitive to typical uncontended critical sections

Developer Focused Architecture and Design

Implementation specific to the next general Intel® microarchitecture code name Haswell
Intel® Transactional Synchronization Extensions (Intel® TSX)

Intel® TSX Operational Aspects

1. **Identify and elide**
   - Identify critical section, start transactional execution
   - Elide locks, keep them available to other threads

2. **Execute transactionally**
   - Manage all transactional state updates

3. **Detect conflicting memory accesses**
   - Track data accesses, check for conflicts from other threads

4. **Abort or commit**
   - Abort discards all transactional updates
   - Commit makes transactional updates instantaneously visible

Implementation specific to the next general Intel® microarchitecture code name Haswell

Identify and Elide: HLE

mutex value

	self	*others*
mutex:	0	0
mutex:	1	0

```
xacquire lock cmpxchg mutex, ebx
```

- Hardware executes XACQUIRE hint
- Hardware elides acquire write to mutex
- Hardware starts transactional execution

```
mov ecx, mutex
```

- Reading mutex in critical section sees last value written (1)
- Other threads reading see free value (0)

mutex:	1	0
mutex:	0	0

```
xrelease mov mutex, 0
```

- Hardware executes XRELEASE hint
- Hardware elides release write to mutex
- Hardware commits transactional execution

Hardware Automatically Manages Elided Locks

Implementation specific to the next general Intel® microarchitecture code name Haswell

Identify and Elide: HLE

- **Hardware support to elide multiple locks**
  - Hardware elision buffer manages actively elided locks
  - XACQUIRE/XRELEASE allocate/free elision buffer entries
  - Skips elision without aborting if no free entry available
- **Hardware treats XACQUIRE/XRELEASE as hints**
  - Functionally correct even if hints used improperly
  - Hardware checks if locks meet requirements for elision
  - May expose latent bugs and incorrect timing assumptions

Hardware Management of Elision Enables Ease of Use

Implementation specific to the next general Intel® microarchitecture code name Haswell

Identify and Elide: RTM

mutex value

	self	*others*
mutex:	0	0
mutex:	0	0

`xbegin <fallback_path>`

- Hardware executes XBEGIN
- Hardware starts transactional execution
- Software checks for a free mutex, skips acquire

`mov ecx, mutex`

- Reading mutex in critical section sees 0
- Other threads reading see free value (0)

mutex:	0	0
mutex:	0	0

`xend`

- Hardware executes XEND
- Hardware commits transactional execution

RTM Provides Increased Flexibility for Software

Execute Transactionally

- **State updated during transactional execution**
  - State includes registers and memory
  - Hardware recovers register and memory state on aborts
- **Hardware manages all transactional updates**
  - Other threads cannot observe any intermediate updates
  - If lock elision cannot succeed, hardware restarts execution
  - Hardware discards all intermediate updates prior to restart

Software Does Not Worry About State Recovery

Implementation specific to the next general Intel® microarchitecture code name Haswell

Execute Transactionally – Memory

- **Buffering memory writes**
  - Hardware uses L1 cache to buffer transactional writes
    - Writes not visible to other threads until after commit
    - Eviction of transactionally written line causes abort
  - Buffering at cache line granularity

- **Sufficient buffering for typical critical sections**
  - Cache associativity can occasionally be a limit
  - Software always provides fallback path in case of aborts

Hardware Manages All Transactional Writes

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Detect Conflicts

- **Read and write addresses for conflict checking**
  - Tracked at cache line granularity using physical address
  - L1 cache tracks addresses written to in transactional region
  - L1 cache tracks addresses read from in transactional region
    - Cache may evict address without loss of tracking
- **Data conflicts**
  - Occurs if at least one request is doing a write
  - Detected at cache line granularity
  - Detected using existing cache coherence protocol
  - Abort when conflicting access detected

Hardware Automatically Detects Conflicting Accesses

Implementation specific to the next general Intel® microarchitecture code name Haswell

Abort or Commit

- **Transactional abort**
  - Occurs when abort condition is detected
  - Hardware discards all transactional updates

- **Transactional commit**
  - Hardware makes transactional updates visible instantaneously
  - No cross-thread/core/socket coordination required

No Global Communication for Commit and Abort

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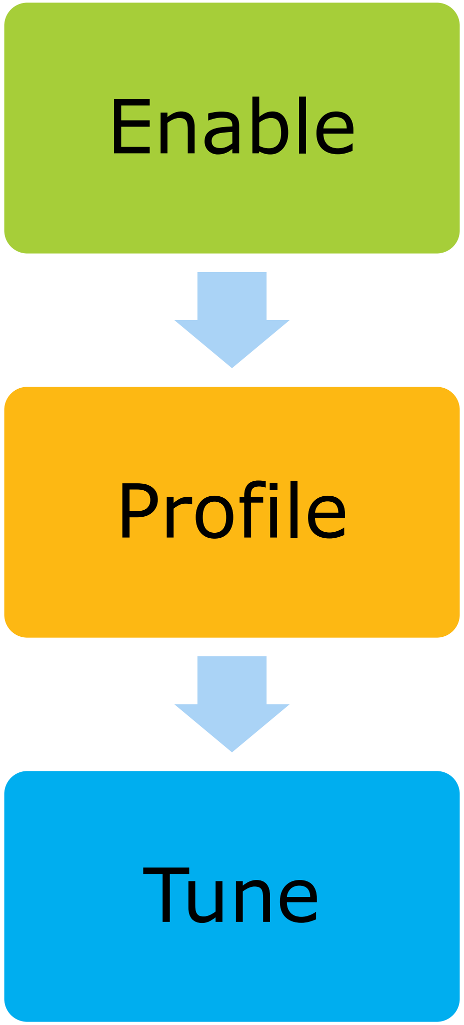
Software



Enable

Architected for enabling ease

Profile

Extensive performance monitoring
and
profiling support

Tune

Easy to pin-point problem spots
Low touch changes

Software Enabling

- **Doesn't need operating system changes to use**
- **Compiler support through intrinsics and inline assembly**
  - Intel® Compiler (ICC) (v13.0)
  - GCC (v4.8)
  - Microsoft* VS2012
- **Various managed runtimes**
  - Enabling inside runtime, hidden from application developer
- **Changes can be localized to libraries**
  - Augment existing lock library to support Intel® TSX-based elision
  - Dynamic linking ➔ no need to recompile
    - Example: Linux GLIBC for pthreads (rtm-2.17 branch)

Easy to Get Started with Intel® TSX

Profiling

- **Extensive support for performance monitoring**
- **Performance Counters**
  - Count various Intel® TSX specific events
  - Count events within transactional regions
  - Gives first order look into transactional region characteristics
- **Performance Profiling**
  - Extensions to Precise Event Based Sampling (PEBS)
  - Allows detailed profiling of transactional aborts
    - Includes cycles in aborted transactional regions

See Intel Software Developer Manual for More Details

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Software Considerations

- **Good coding practices will also help Intel® TSX**
  - Avoid false or inadvertent sharing
  - Avoid timing based synchronization
- **Most common locks are already elision friendly**
  - Some locks need effort to make them elision friendly
  - RTM provides improved flexibility
- **Not everything can or should use Intel® TSX**
- **Intel® TSX is not a magic bullet**

Watch for the Programmer Optimization Guide

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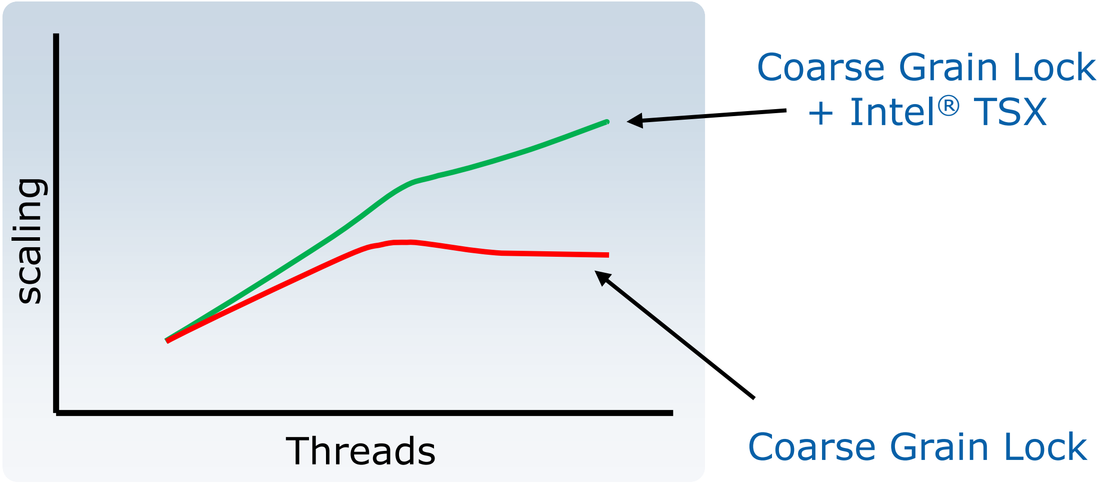
Applying Intel® TSX

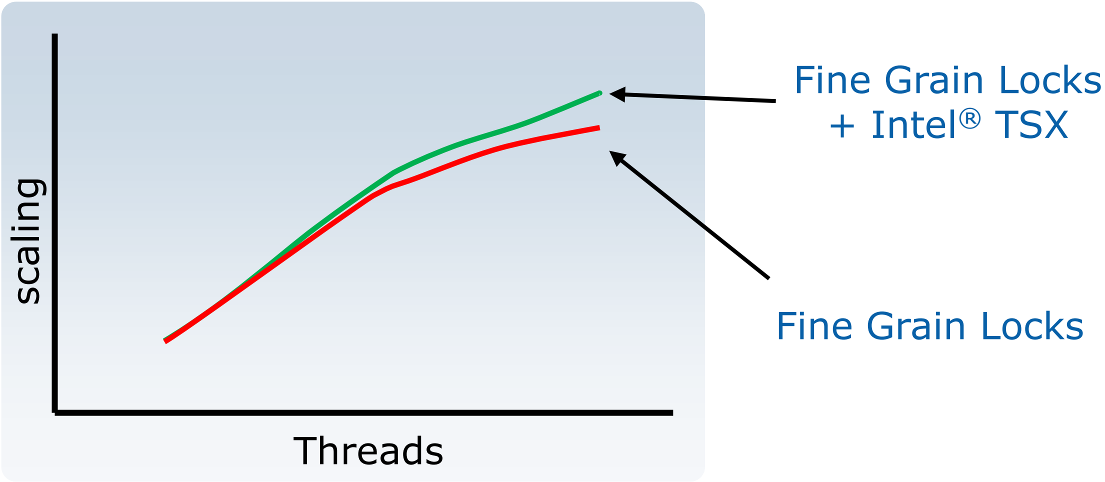
Application with Coarse Grain Lock



Coarse Grain Lock + Intel® TSX

Coarse Grain Lock

Application re-written with Finer Grain Locks



Fine Grain Locks + Intel® TSX

Fine Grain Locks

An example of secondary benefits of Intel® TSX

Fine Grain Behavior at Coarse Grain Effort

Enabling Simpler Algorithms

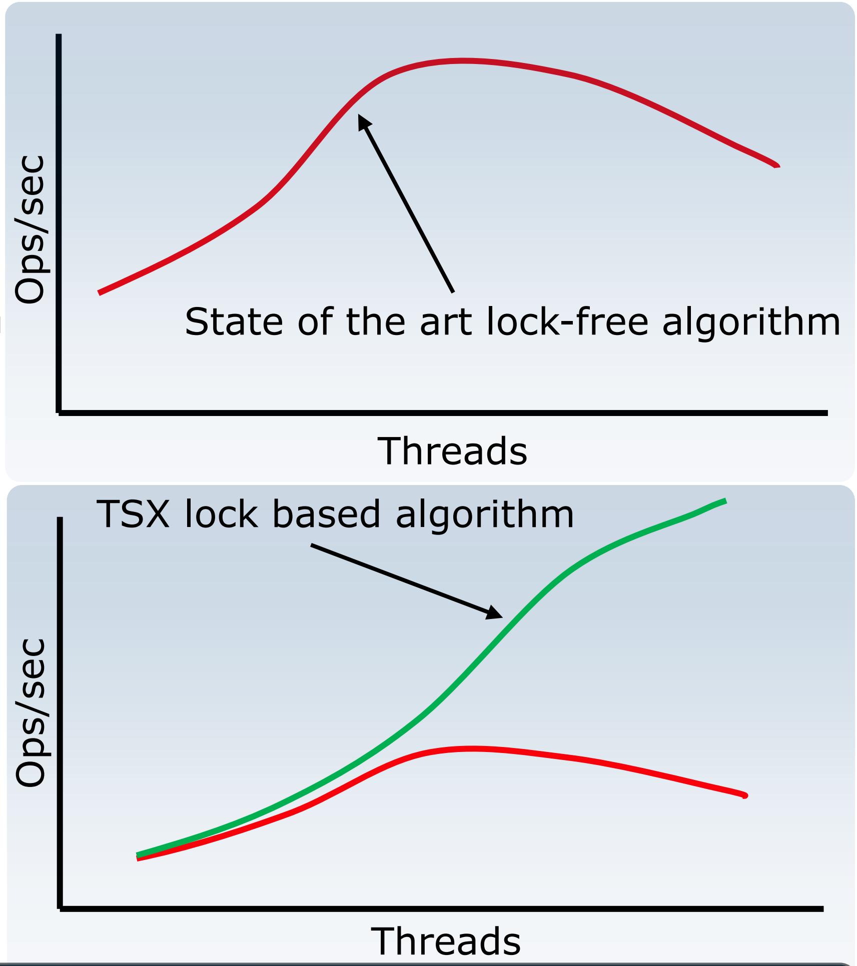
Lock-Free Algorithm

- Don’t use critical section locks
- Developer manages concurrency
- Very difficult to get correct & optimize
  - **Constrain data structure selection**
  - Highly contended atomic operations

Lock-Based + Intel® TSX

- Use critical section locks for ease
- Let hardware extract concurrency
- Enables algorithm simplification
  - **Flexible data structure selection**
  - Equivalent data structure lock-free algorithm very hard to verify

Real World Example



Intel® TSX Can Enable Simpler Scalable Algorithms

Intel® TSX Summary

- **Improves existing synchronization**
  - Lock-based critical sections
  - Goes beyond latency reduction and focuses on serialization
- **Exposes hidden concurrency**
  - Coarse grain effort by developer
  - Finer grain behavior by hardware
- **Architected for**
  - Typical concurrency use-case with lock elision
  - Simple enabling and ease of use

Think About How It Helps You and Other Novel Usages

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