Intel® SoC Watch for Windows* Release Notes

4th November 2019

Version 2020.1

Intel Corporation

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Contents

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Version History

These are the main releases of Intel® SoC Watch:

Date	Revision	Description
November, 2017	2.4	First release that aligns all command line parameters and output formats across all supported operating systems.
December, 2017	2.4.2	Update release, includes support for Intel platforms code named Apollo Lake (new stepping) and corrected console message order when using delayed start option.
February, 2018	2.5	Includes support for Intel platform code named Gemini Lake and other fixes.
April, 2018	2.6	Enhancements include new hot key Alt-S, new --log option, modified metric groupings, and improved support in gfx metrics.
May, 2018	2.6.1	Update release.
August, 2018	2.7	Added average frequency report, new options (program-delay, disable-alts), new metrics (pkg-pwr), new group names, support for Intel platforms code named Whiskey Lake, Amber Lake, and Cherry Trail, fixed issues in ddr-bw, automation summary, and multiple pkg handling.
November, 2018	2.8	Added filter for acpi-dstate devices. Fixed error in ddr-bw reporting. Alt-S hotkey off by default.
January, 2019	2.9	Added trace file report grouping and informational messages.
March, 2019	2.10	Added histogram for CPU frequency and bug fixes.
June, 2019	2.11	Improves handling of unrecognized CPUs, reporting S-state when hibernation occurs, and other bug fixes.
September, 2019	2019.12	Added support for Intel platform code named Ice Lake. Modified hw-cpu-pstate reporting.
October, 2019	2019.13	Fixed issue in hw-cpu-pstate for Intel platform code named Ice Lake.
November, 2019	2020.1	Added support for Intel platform code named Comet Lake.

Intended Audience

Use this document if you use Intel SoC Watch to analyze power consumption on a Windows* system.

Customer Support

For technical support, including answers to questions not addressed in this product, see the Intel System Studio forum (https://software.intel.com/en-us/forums/intel-system-studio).

1 Introduction

Intel® SoC Watch is a data collector for power-related data that can help identify issues on a platform that prevent entry to power-saving states. Captured metrics include:

- System sleep states
- CPU and GPU sleep states
- Processor frequencies
- Temperature data
- Device sleep states

You can correlate the collected data and visualize over time using Intel®VTune Amplifier.

This document provides system requirements, installation instructions, issues and limitations, and legal information.

To learn more about this product, see:

- New features listed in the New in this Release section below
- Reference documentation listed in the Related Documentation section below
- Installation instructions can be found at: Installation Notes

Optimization Notice

Intel's compilers may or may not optimize to the same degree for non-Intel microprocessors for optimizations that are not unique to Intel microprocessors. These optimizations include SSE2, SSE3, and SSSE3 instruction sets and other optimizations. Intel does not guarantee the availability, functionality, or effectiveness of any optimization on microprocessors not manufactured by Intel. Microprocessor-dependent optimizations in this product are intended for use with Intel microprocessors. Certain optimizations not specific to Intel microarchitecture are reserved for Intel microprocessors. Please refer to the applicable product User and Reference Guides for more information regarding the specific instruction sets covered by this notice.

Notice revision #20110804

New in This Release

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Release v2021.1 includes these changes:

- Added support for Intel platform code named Comet Lake.

3 System Requirements

Supported Architectures

Intel SoC Watch supports these Intel microarchitecture or platform code names:

- Cherryview (Cherry Trail)
- Apollo Lake
- Gemini Lake
- Broadwell
- Skylake
- Kaby Lake
- Coffee Lake
- Whiskey Lake
- Amber Lake
- Comet Lake
- Ice Lake

Minimum System Requirements

You can run Intel SoC Watch on these 64-bit operating systems with administrator permissions:

- Windows* 10

4 Where to Find the Release

Go to the Intel® System Studio website (https://software.intel.com/en-us/intel-system-studio) to get either an Evaluation (30-day trial release) license or a commercial license, and download the package from the Intel Registration Center (http://registrationcenter.intel.com/).

5 Installation Notes

Intel SoC Watch for Windows* OS is installed as part of Intel System Studio when downloaded to a Windows host system.

Refer to the *Intel® SoC Watch for Windows* OS User's Guide* for additional instructions and understand how to install WDTF to allow automatic entry to Connected Standby.

Default Installation Folders

The default top-level installation folder for this product is:

```
C:\Program Files (x86)\IntelSWTools\energy_profiler_and_socwatch\socwatch_for_target
```

If you are installing on a system with a non-English language version of Windows OS, the name of the `Program Files` folder may be different. On Intel® 64 systems, the directory name is `Program Files (X86)` or the equivalent.

Installing on a Remote Target

You can install Intel SoC Watch on a remote Windows system. Detailed instructions are available from https://software.intel.com/en-us/energy-analysis-user-guide-preparing-a-target-windows-system-for-energy-analysis.

Changing, Updating, and Removing the Product

If you want to add or remove components from an installation, open the Control Panel, select the Add or Remove Programs applet, select Intel®System Studio, and click **Change**. To remove the product, select Intel SoC Watch and click **Remove**.

When installing an updated version of Intel SoC Watch, any previously installed version will automatically be removed.

6 Fixed Issues

Release v2020.1 has a fix for these issues.

- Fixed issue resulting in some platforms being reported as Intel platform code name Amber Lake that should have been Intel platform code name Kaby Lake. The data reported was correct, only the code name was incorrect.

7 Known Issues

Bandwidth (on Intel Core Platforms)

- The presence of EDRAM on a system may not be detected by Intel SoC Watch. This is known to occur when the accelerator card VCA2, which contains EDRAM, is present.
- Total DDR bandwidth does not include EDRAM. On systems using EDRAM, the `ddr-bw` feature report may have a discrepancy between the total data reads and writes and the total component requests. The Data Reads+Data Writes will be significantly higher than the total IA+GT+IO requests, because the EDRAM requests are not included.

Bandwidth and DRAM Self Refresh (on Intel Atom® Platforms)

- On Intel platforms code named Apollo Lake and Gemini Lake, memory bandwidth and memory self-refresh metrics are not available. These features are not supported: `ddr-bw`, `cpu-ddr-bw`, `cpu-ddr-mod0-bw`, `cpu-ddr-mod1-bw`, `disp-ddr-bw`, `isp-ddr-bw`, `gfx-ddr-bw`, `io-bw`, `all-approx-bw`, `dram-srr`.

C-States / P-States

- The hardware CPU P-state data may be missing for some Cores when using feature `-f hw-cpu-pstate` on Intel platforms code named Skylake, Kaby Lake, Whiskey Lake, and Amber Lake. The issue is caused by unexpected behavior of the hardware counters. The tool ignores these bad samples which results in the missing data.
- On Intel platforms code named Broxton and Apollo Lake, the `cpu-cstate` metric results do not contain module C-state information.
- OS-based CPU P-state report does not support platforms with > 64 logical processors. The hardware-based P-state report is correct. The problem is in the OS event trace which provides state changes for only a partial set of logical processors when the platform is configured for more than 64 logical processors. When this situation occurs, a warning message is printed in the report indicating which processors have no OS P-state change events.
- In order to visualize graphics C-states that are reported as Render and Media, the table headers in the trace file (generated with option -r int), must be manually modified, adding *Render* and *Media* to the appropriate C0, C1, and C6 column headers.

S States & D States

- On Intel platform code named CherryView based devices:
  - Even when the device's screen is off, the NC DState called Display DPIO is reported in the D0i0 state 100% of the time. This result may or may not be correct.
  - When collecting NC D0ix states with the `-f nc-dstate` switch, note that the Display Island B (HDMI) IP block will remain in D0i0 when the primary display is enabled even if an HDMI cable is removed.
  - When using the `sc-dstate` feature, the SEC IP block results are incorrect and should be ignored. Also, the UFS IP block results are incorrect because an internal fuse is disabled.

Miscellaneous

- Feature -f dram-pwr is not supported by all versions of the server Intel platforms code named Skylake-Xeon, Cascade Lake-Xeon, and Denverton). The report contains all zero values in this case.
- On platforms with HyperV enabled, the sum of the CPU C-state idle residencies will not match CPU P-state idle residency time. The issue occurs because HyperV does not allow setting of a bit, resulting in incorrect core-level reporting of both C-state and P-states.

- Metrics report Unknown 0 when `-m` is not used and hibernation occurs. Metrics with a snapshot default collection mode, such as CPU C-state, will show the Unknown state with 0 time and the remaining states will not sum to the total collection duration if the system entered hibernation during the collection and the `-m` option was not specified. The snapshot metrics are only collected at the start and end of a collection by default, but finding hibernation time requires samples taken throughout the collection. Including `-m` will cause continuous sampling to occur for all metrics. When hibernation occurs, a message reporting time spent in hibernation appears at the beginning of the summary report. The Unknown state is then included for all appropriate metrics and the time in hibernation is included in that state. Refer to the *Intel SoC Watch User's Guide* "Options Quick Reference" section to learn which metrics have a snapshot collection mode by default.
- Package level power data (-f pkg-pwr) is reported incorrectly for Cascade Lake-Xeon (AP) which has multiple Die in the CPU package. Intel SoC Watch labels the power as per package but it is actually per Die. There is no package level power.
- Syntax errors in the command line may not report a visible error message. If a collection did not run and you are not seeing any error message, add option `-d 2` to your command line to get more information.
- Insufficient system resources error seen on occasion when collecting OS event trace metrics such as `acpi-dstate`. The system error “WARNING: Cannot enable provider in the trace file <etl filename>” has been reported when collecting metrics that enable event trace logging. This error prevents ETL logging from being started and is usually caused by a background process consuming system resources. Use Task Manager to find and remove such processes then try the collection again.
- Hyper-V and Virtualization-based Security (VBS) prevent some metrics from being collected. Intel SoC Watch detects when Hyper-V and Virtualization-based Security is enabled on the platform, reports a warning message on the console and disables metrics that are blocked by these settings. When Hyper-V and VBS are enabled `cpu-gpu-concurrency` cannot be collected.
- Collection on Windows* Server 2016 OS will result in failure to load the Intel SoC Watch driver if Secure Boot is enabled on the platform. The workaround is to disable Secure Boot. The problem on Windows 10 client OS was resolved.
- If a command window is closed (using either the X button or Alt-F4) while the socwatch process is running, or the Task Manager is used to kill the socwatch process, then the behavior of a subsequent run of Intel SoC Watch becomes unknown. The proper way to terminate Intel SoC Watch is using Ctrl-C. A collection driver may be left in an undefined state when Intel SoC Watch is abruptly terminated because there is no OS event to allow proper cleanup. This can cause the next Intel SoC Watch collection to result in anything from bad data to a system crash. If a driver is left running, it must be removed. You can reboot the system to clear a driver or use the following set of commands to check if the driver is running, stop it, and then delete it:`sc query socwatchdrv; sc stop socwatchdrv; sc delete socwatchdrv`.

Intel® VTune™ Amplifier Visualization

- Intel VTune Amplifier 2017 for Systems Update 1 or later is required for visualizing and analyzing Intel SoC Watch v2.10.0 and newer PWR files. We recommend using the latest version of Intel VTune Amplifier.
- If the bandwidth is 0 Mb throughout the collection for a particular bandwidth type, Intel VTune Amplifier will not show a timeline entry for it. The timeline is shown only if there is at least one non-zero value.
- In some cases, the summary CSV results produced by Intel SoC Watch can vary from the summary results shown by Intel VTune Amplifier even though they represent the same collection. For example, the summary CSV file may report a specific cpu-pstate residency of 50.78% and Intel VTune Amplifier may report the same cpu-pstate residency as 50.8%.
- The minimum and average calculations displayed in the grid for Sampled Value metrics don’t take 0 values into consideration in older versions of Intel VTune Amplifier. For example, Sampled Graphics P-States minimum values may show a value higher than 0 Mhz even when some samples have 0 Mhz values. This in turn affects the average value calculation.

8 Related Documentation

The below documents are available with this release.

- Intel® SoC Watch for Windows* OS User's Guide
- Energy Analysis help: https://software.intel.com/en-us/energy-analysis-user-guide

9 Release Content

- Intel® SoC Watch for Windows* OS User's Guide
- Intel® SoC Watch for Windows* OS Release Notes
- Intel® SoC Watch for Windows* OS executables

Acronyms and Terms

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The following acronyms and terms are used in this document (arranged in alphabetic order):

Acronym/Term	Description
SoC	System on Chip