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News Fact Sheet

INTEL SUMMARY: 2008 VLSI SYMPOSIA ON TECHNOLOGY AND CIRCUITS

June 17, 2008: Intel Corporation is presenting five technical papers at the 2008 VLSI Symposia taking place June 17-20 in Honolulu. Below are brief summaries of the Intel papers.

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The following papers will be presented on June 18:

Paper 9.4: A Scaled Floating Body Cell Memory with High-k + Metal Gate on Thin-Silicon and Thin-BOX for 15nm Node and Beyond
This paper reports Intel's successful fabrication of the smallest reported floating body cell (FBC) planar devices, with functional devices measuring down to 30nm gate lengths. FBC is a candidate for increased memory density compared to the standard six transistor (6T) cache memory that is used on all microprocessors today. FBC devices allow researchers to pack more bits within a given die area, which translates to faster computation. The dimensions of Intel's FBC devices are two generations smaller as compared to other published work on similar FBC devices. The devices with 60nm gates show suitable memory retention and at this dimension, a bit cell could be less than 0.01um2 in size, making it suitable for potential use at the 15nm node. There is also excellent agreement between device and simulation that allows prediction of continued scaling to the 10nm technology node.

Paper 13.2: 45nm High-k + Metal Gate Strain-Enhanced Transistors
This paper describes how Intel's revolutionary 45nm high-k + metal gate transistors are made with a "gate last" process flow that incorporates unique NMOS and PMOS transistor strain enhancement techniques for industry-leading performance and low power characteristics. Also described is how cost-effective 193nm dry lithography was extended to high-density 45nm design rules without adding masking layers. This technology has been shipping in multiple Intel microprocessor products in high volume and with high yield since November.

Paper 5.4: PVT-Variations and Supply-Noise Tolerant 45nm Dense Cache Arrays with Diffusion-Notch-Free (DNF) 6T SRAM Cells and Dynamic Multi-Vcc Circuits
This paper demonstrates new adaptive circuit techniques that would allow lowering the minimum operating supply voltage (or Vccmin) of SRAM cache cells by making the cells more

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tolerant to variations in process, voltage, and temperature. Under certain operating conditions, measurements on a 45nm test-chip show that number of single cell errors is reduced by as much as 26 times. These circuits could allow Intel to push to better performance and power characteristics without failures on future processes.

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The following paper will be presented on June 19:

Paper 7.1: Next Generation Intel® Micro-architecture (Nehalem) Clocking Architecture
This paper describes the next-generation Intel micro-architecture (Nehalem) processor's core and I/O clocking architecture. Nehalem is a family of Intel multi-core processors implemented in 45nm high-k + metal-gate process technology. The Nehalem microprocessor, in its first implementation, has four enhanced cores, an uncore for connecting the cores with the I/O, and third level cache. Nehalem supports a new high-speed, point-to-point, coherent, Intel® QuickPath interconnect for communication between CPUs, chipsets, and I/O hubs. It also supports an integrated memory controller supporting high-speed multi-channel DDR3 memory.

- Nehalem Highlights: Configurable clocking, fastlock low-skew PLLs, high reference clock frequencies, analog supply tracking system, adaptive frequency clocking, low jitter Intel QuickPath interconnect and integrated memory controller clock generation, and jitter-attenuating DLLs.

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The following paper will be presented on June 20:

Paper 17.2: In-Situ Jitter Tolerance Measurement Technique for Serial I/O
This paper demonstrates the on-chip integration of a common chip-to-chip I/O performance measurement normally done only in a lab. Specifically this could allow future processors to check conditions related to timing noise (jitter) directly in their ultimate consumer or enterprise environment. This capability would allow I/O links to optimize timing margins and/or data transmission speeds, resulting in higher overall performance.

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Intel Senior Fellows, Intel Fellows and Intel engineers will also participate in three VLSI panel sessions on June 17, including:

- Ten years after – Has SOI finally arrived?
  Intel Panelist: Mark Bohr
  Other panelists from: Infineon, IBM, SOITEC, AIST, TSMC, Toshiba, Hitachi

- Who will keep SRAM scaling alive by 2012: Designers or Technologists?
  Moderators: Intel and NEC representatives
  Intel panelist: Claire Webb
  Other panelists from: IBM, Texas Instruments, TSMC, Toshiba, NEC

- Photons vs. Electrons – Which Will Win and When? (The Ongoing Race for Short-Distance High-Speed Data Connectivity)
  Intel panelist: Ian Young
  Other panelists from: Stanford University, Force10 Networks, Teranetics, Fujitsu Japan, NTT Japan

Additional information and a complete agenda for the conference can be found at http://www.vlsisymposium.org/index.html.

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