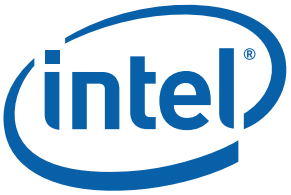

# PCI Express* 3.0 438-Pin Riser Card Edge Connector

## Specification

***February 2014***

Reference Number: 329988-001

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# Revision History

| Document Number | Revision Number | Description | Date |
|---|---|---|---|
| 329988 | 1.0 | • Initial Release | February 2014 |

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# 1 Introduction

## 1.1 Purpose and Scope

This document provides specifications for the PCI Express* 3.0 438-pin riser card edge connector that interfaces with a riser card supporting up to 48 PCIe* lanes at 8 Gbps and power at 12 V, 5 V, and 3.3 V. It contains mechanical, electrical, and environmental requirements of the connector accepting 2.36 mm (0.093 in.) nominal thickness add-in card. The intent of this document is to enable connector, system designers and manufacturers to build, qualify, and use the PCIe riser card edge connectors as the standard interface between the PCIe riser card and the Intel server platform.

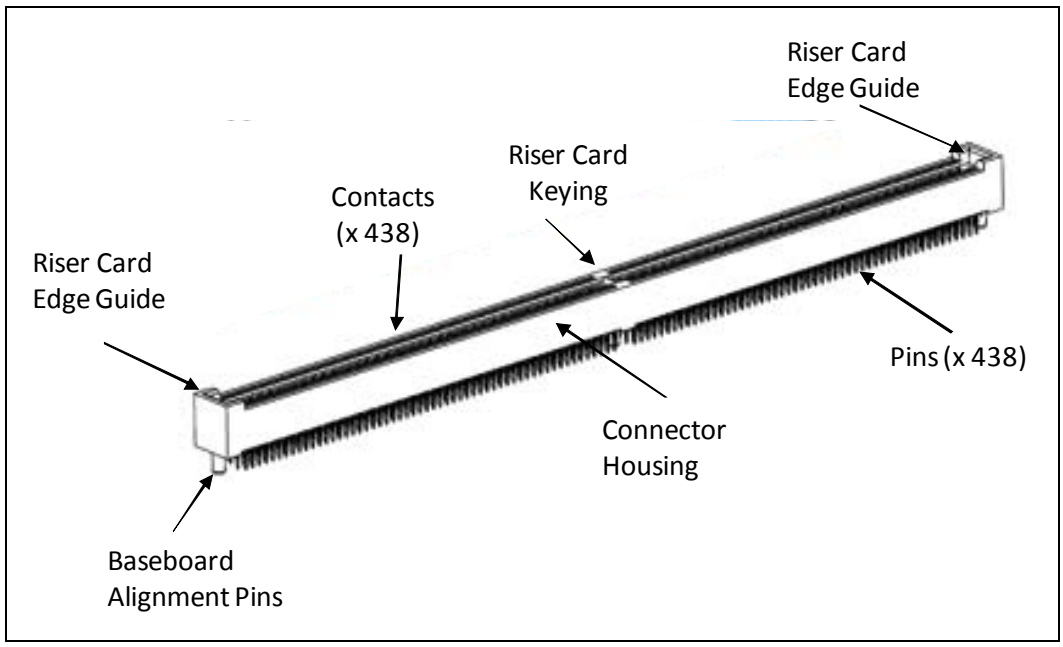
In this document the term *'connector'* refers to the PCIe riser card edge connector, the term '*baseboard'* refers to the motherboard (MB) or system board the connector is mounted onto, and the term *'riser card'* refers to the PCIe riser card, whose gold finger edge is inserted vertically into the connector.

## 1.2 Connector Overview

The PCIe riser card connector is a single-piece 438-pin vertical press fit connector with 0.7 mm staggered contact pitch. It is defined for applications where a riser card of 2.36 mm (0.093 in.) nominal thickness vertically enters the connector, perpendicular to the system board.

The connector requires the use of mechanical alignment/insertion/retention/extraction mechanisms. The connector is designed for visual alignment of the add-in card and connector. Designs that prevent visual alignment (blind-mate) must use blind-mate alignment components such as guide pins and guide pin receptacles. (See Appendix B, "Riser Card Installation" for more details.)

**Figure 1-1. 438-Pin PCIe* Riser Card Edge Connector**



## 1.3 Terms and Definitions

| Term | Description |
|---|---|
| baseboard | Also known as motherboard or system board. |
| dB | Decibel: A unit for the measurement of the strength of a signal expressed in decibels relative to one watt given as function of volts, that is, 20log10(V1/V2). |
| DUT | Device Under Test |
| EIA | Electronic Industry Alliance |
| EOL | End of life |
| gap | Space between two traces |
| Gbps | Gigabytes per second |
| GD&T | Geometric Dimensioning and Tolerances |
| LLCR | Low Level Contact Resistance |
| module | Refers to the PCIe* riser card (also known as a riser card). |
| PCB | Printed Circuit Board |
| riser card | Refers to the PCIe riser card (also known as a module). |
| SMA | Subminiature version A |
| staggered contact pitch | Refers to diagonal position of contacts with respect to one another. |
| system board | Printed circuit board on which the PCIe riser card connector is mounted. |
| TDR | Time Domain Reflectometry |
| TDT | Time Domain Transmission |
| tie bar | A physical part near the gold finger to allow electroplating of Ni and Au after etching. |
| TRL | Through, reflection, and line |
| TW | Trace width |
| vertical connector | A connector that accepts a module perpendicular to the system board. |
| VNA | Vector Network Analyzer |

## 1.4 References

A 7-year life cycle test is applied for both the mechanical requirement and the environmental requirement, per EIA 364-1000. This specification requires references to other documents.

- EIA-364-05: Contact Insertion, Release and Removal Force Test Procedure for Electrical Connectors
- EIA-364-13: Mating and Unmating Force Test Procedure for Electrical Connectors and Sockets
- EIA 364-23C - Low Level Contact Resistance Test Procedures for Electrical Connectors and Sockets
- EIA 364-70B Temperature Rise Versus Current Test Procedure for Electrical Connectors and Sockets
- EIA364-09 Durability (preconditioning)
- EIA364-17 Temperature life
- EIA364-23 Low Level Contact Resistance
- EIA364-27 Mechanical Shock

- EIA364-28 Vibration
- EIA 364-29 Contact Retention Test Procedure for Electrical Connectors
- EIA364-31 Cyclic temperature & humidity
- EIA364-32 Thermal Shock
- EIA364-65 Mixed flowing gas
- EIA364-91 Dust
- Agilent Application Note, "Agilent Network Analysis Applying the 8510 TRL Calibration for Non-Coaxial Measurements", Product Note 8510-8A
- PCIe* Card Electromechanical Specification, Revision 1.0 July 21, 2013
- 325028-001 PCIe* Gen 3 Connector High Speed Electrical Test Procedure, Rev 1.0, Jan 2011

  http://www.intel.com/content/www/us/en/io/pci-express/pci-express-architecture-devnet-resources.html
- EIA-364-1000 Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets used in Business Office Applications. www.eia.org

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# 2 Signal Description and Pin Assignment

This section describes the signals included in the PCIe riser card connector, as well as the riser card and the connector pin assignments.

## 2.1 Signal Description

PCIe riser card connector signal groups, names, and number of assigned pins are provided in Table 2-1.

**Table 2-1. PCIe* Riser Card Connector and Module Signal Descriptions**

| Signal group | Signal name | Pin Count | Notes |
|---|---|---|---|
| Transmit (Differential) | PETp* | 48 | Transmitter differential pair |
| | PETn* | 48 | |
| Receive (Differential) | PERP* | 48 | Receiver differential pair |
| | PERn* | 48 | |
| Reference Clock (Differential) | REFCLK+ | 5 | Reference Clock (differential pair) |
| | REFCLK- | 5 | |
| Reference Clock (single ended) | REFCLK | 1 | |
| Presence | PRSNT | 5 | Presence Detect |
| Reset | PERST | 2 | |
| 3.3 V Data | 3.3VDAT | 3 | |
| Reserved | RESV | 4 | Reserved |
| Miscellaneous | MISC | 9 | |
| 3.3 V power | +3.3V | 16 | 3.3 V Power |
| 3.3 V aux power | +3.3Vaux | 4 | 3.3 V auxiliary power |
| 12 V power | +12V | 30 | 12 V Power |
| Ground | GND | 162 | Signal and Power Reference VSS |
| **Total** | | **438** | |

## 2.2 Pin Assignments

PCIe riser Connectors pin assignment is listed in Table 2-3 show the typical pin-out for a 438-Pin PCIe riser connector and baseboard only (ground barrier via) assignments. Connector pins are grouped such that A1-A73 and B1-B73 are clocks, control, and ground signals; pins A74-A219 and B74-B219 are data pins. Ground barrier via are listed in columns C and D. Note the presents of ground barrier vias within the connector pin array adjacent to pins B70 and B74. Figure 3-3 and Figure 3-8 respectively illustrate pin 1 location on the connector and the riser card.

## Table 2-2. Connector Pin Assignment Color Code

- Power
- Ground (in connector baseboard and riser)
- Ground (in baseboard only)
- Reference clock
- Transmit data
- Receive data
- Control, reserved, or miscellaneous

## Table 2-3. PCIe Riser Card Connector and Module Pin Assignment (Sheet 1 of 4)

| C | | B | | | | A | | | | D | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| C1 | | B1 | | | PERST_N | GND | | | A1 | | D1 |
| C2 | | B2 | | GND | | | GND | | A2 | | D2 |
| C3 | | B3 | P12V | | | | | P12V | A3 | | D3 |
| C4 | | B4 | | | P12V | P12V | | | A4 | | D4 |
| C5 | | B5 | | P12V | | | P12V | | A5 | | D5 |
| C6 | | B6 | P12V | | | | | P12V | A6 | | D6 |
| C7 | | B7 | | | P12V | P12V | | | A7 | | D7 |
| C8 | | B8 | | P12V | | | P12V | | A8 | | D8 |
| C9 | | B9 | P12V | | | | | P12V | A9 | | D9 |
| C10 | | B10 | | | P12V | P12V | | | A10 | | D10 |
| C11 | | B11 | | P12V | | | P12V | | A11 | | D11 |
| C12 | | B12 | P12V | | | | | P12V | A12 | | D12 |
| C13 | | B13 | | | P12V | P12V | | | A13 | | D13 |
| C14 | | B14 | | P12V | | | P12V | | A14 | | D14 |
| C15 | | B15 | P12V | | | | | P12V | A15 | | D15 |
| C16 | | B16 | | | P12V | P12V | | | A16 | | D16 |
| C17 | | B17 | | P12V | | | P12V | | A17 | | D17 |
| C18 | | B18 | GND | | | | | GND | A18 | | D18 |
| C19 | | B19 | | | GND | GND | | | A19 | | D19 |
| C20 | | B20 | | GND | | | GND | | A20 | | D20 |
| C21 | | B21 | GND | | | | | GND | A21 | | D21 |
| C22 | | B22 | | | GND | GND | | | A22 | | D22 |
| C23 | | B23 | | GND | | | p3p3v | | A23 | | D23 |
| C24 | | B24 | GND | | | | | p3p3v | A24 | | D24 |
| C25 | | B25 | | | p3p3v | p3p3v | | | A25 | | D25 |
| C26 | | B26 | | p3p3v | | | p3p3v | | A26 | | D26 |
| C27 | | B27 | p3p3v | | | | | p3p3v | A27 | | D27 |
| C28 | | B28 | | | p3p3v | p3p3v | | | A28 | | D28 |
| C29 | | B29 | | p3p3v_aux | | | p3p3v | | A29 | | D29 |
| C30 | | B30 | p3p3v | | | | | p3p3v | A30 | | D30 |
| C31 | | B31 | | | p3p3v | GND | | | A31 | | D31 |
| C32 | | B32 | | p3p3v | | | p3p3v_aux | | A32 | | D32 |
| C33 | | B33 | GND | | | | | p3p3v_aux | A33 | | D33 |
| C34 | | B34 | | | p3p3v_aux | GND | | | A34 | | D34 |
| C35 | | B35 | | p3p3v_aux | | | PWRGOOD | | A35 | | D35 |
| C36 | | B36 | GND | | | | | GND | A36 | | D36 |
| C37 | GND | B37 | | | PWRGOOD_p3p3v_N | PERST_N | | | A37 | GND | D37 |
| C38 | | B38 | | GND | | | GND | | A38 | | D38 |
| C39 | | B39 | SMB_HOST_CLK | | | | | SMB_HOST_DATA | A39 | | D39 |
| C40 | GND | B40 | | | GND | GND | | | A40 | GND | D40 |
| C41 | | B41 | | SMB_VPP_CLK | | | SMB_VPP_DATA | | A41 | | D41 |
| C42 | | B42 | GND | | | | | GND | A42 | | D42 |
| C43 | GND | B43 | | | p5p5v | AUX | | | A43 | GND | D43 |
| C44 | | B44 | | GND | | | GND | | A44 | | D44 |
| C45 | | B45 | PRSNT_N | | | | | p5p5v | A45 | | D45 |

## Table 2-3. PCIe Riser Card Connector and Module Pin Assignment (Sheet 2 of 4)

| C | | B | | | | A | | | | D | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| C46 | GND | B46 | | | GND | GND | | | A46 | GND | D46 |
| C47 | | B47 | | PRSNT_N | | | PRSNT_N | | A47 | | D47 |
| C48 | | B48 | GND | | | | | GND | A48 | | D48 |
| C49 | GND | B49 | | | AUX | PRSNT_N | | | A49 | GND | D49 |
| C50 | | B50 | | GND | | | GND | | A50 | | D50 |
| C51 | | B51 | AUX | | | | | RISID | A51 | | D51 |
| C52 | GND | B52 | | | GND | GND | | | A52 | GND | D52 |
| C53 | | B53 | | AUXCLK | | | GND | | A53 | | D53 |
| C54 | | B54 | GND | | | | | GND | A54 | | D54 |
| C55 | GND | B55 | | | WAKE_N | AUX | | | A55 | GND | D55 |
| C56 | | B56 | | GND | | | GND | | A56 | | D56 |
| C57 | | B57 | GND | | | | | PERST_N | A57 | | D57 |
| C58 | GND | B58 | | | REFCLK0+ | GND | | | A58 | GND | D58 |
| C59 | | B59 | | REFCLK0- | | | RESV | | A59 | | D59 |
| C60 | | B60 | GND | | | | | GND | A60 | | D60 |
| C61 | GND | B61 | | | GND | GND | | | A61 | GND | D61 |
| C62 | | B62 | | REFCLK1+ | | | GND | | A62 | | D62 |
| C63 | | B63 | REFCLK1- | | | | | GND | A63 | | D63 |
| C64 | GND | B64 | | | GND | GND | | | A64 | GND | D64 |
| C65 | | B65 | | GND | | | GND | | A65 | | D65 |
| C66 | | B66 | REFCLK2+ | | | | | GND | A66 | | D66 |
| C67 | GND | B67 | | | REFCLK2- | GND | | | A67 | GND | D67 |
| C68 | | B68 | | GND | | | GND | | A68 | | D68 |
| C69 | | B69 | GND | | GND | | | GND | A69 | | D69 |
| C70 | GND | B70 | | | REFCLK3+ | GND | | | A70 | GND | D70 |
| C71 | | B71 | | REFCLK3- | | | GND | | A71 | | D71 |
| C72 | | B72 | GND | | | | | GND | A72 | | D72 |
| C73 | GND | B73 | | GND | GND | GND | | | A73 | GND | D73 |
| C74 | | B74 | | PETp0 | | | PERp0 | | A74 | | D74 |
| C75 | | B75 | PETn0 | | | | | PERn0 | A75 | | D75 |
| C76 | GND | B76 | | | GND | GND | | | A76 | GND | D76 |
| C77 | | B77 | | PETp1 | | | PERp1 | | A77 | | D77 |
| C78 | | B78 | PETn1 | | | | | PERn1 | A78 | | D78 |
| C79 | GND | B79 | | | GND | GND | | | A79 | GND | D79 |
| C80 | | B80 | | PETp2 | | | PERp2 | | A80 | | D80 |
| C81 | | B81 | PETn2 | | | | | PERn2 | A81 | | D81 |
| C82 | GND | B82 | | | GND | GND | | | A82 | GND | D82 |
| C83 | | B83 | | PETp3 | | | PERp3 | | A83 | | D83 |
| C84 | | B84 | PETn3 | | | | | PERn3 | A84 | | D84 |
| C85 | GND | B85 | | | GND | GND | | | A85 | GND | D85 |
| C86 | | B86 | | PETp4 | | | PERp4 | | A86 | | D86 |
| C87 | | B87 | PETn4 | | | | | PERn4 | A87 | | D87 |
| C88 | GND | B88 | | | GND | GND | | | A88 | GND | D88 |
| C89 | | B89 | | PETp5 | | | PERp5 | | A89 | | D89 |
| C90 | | B90 | PETn5 | | | | | PERn5 | A90 | | D90 |
| C91 | GND | B91 | | | GND | GND | | | A91 | GND | D91 |
| C92 | | B92 | | PETp6 | | | PERp6 | | A92 | | D92 |
| C93 | | B93 | PETn6 | | | | | PERn6 | A93 | | D93 |
| C94 | GND | B94 | | | GND | GND | | | A94 | GND | D94 |
| C95 | | B95 | | PETp7 | | | PERp7 | | A95 | | D95 |
| C96 | | B96 | PETn7 | | | | | PERn7 | A96 | | D96 |
| C97 | GND | B97 | | | GND | GND | | | A97 | GND | D97 |
| C98 | | B98 | | PETp8 | | | PERp8 | | A98 | | D98 |
| C99 | | B99 | PETn8 | | | | | PERn8 | A99 | | D99 |
| C100 | GND | B100 | | | GND | GND | | | A100 | GND | D100 |
| C101 | | B101 | | PETp9 | | | PERp9 | | A101 | | D101 |
| C102 | | B102 | PETn9 | | | | | PERn9 | A102 | | D102 |
| C103 | GND | B103 | | | GND | GND | | | A103 | GND | D103 |
| C104 | | B104 | | PETp10 | | | PERp10 | | A104 | | D104 |

## Table 2-3. PCIe Riser Card Connector and Module Pin Assignment (Sheet 3 of 4)

| C | | B | | | | | A | | | | D | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C105 | | B105 | PETn10 | | | | | | PERn10 | A105 | | D105 |
| C106 | GND | B106 | | | GND | | GND | | | A106 | GND | D106 |
| C107 | | B107 | | PETp11 | | | | PERp11 | | A107 | | D107 |
| C108 | | B108 | PETn11 | | | | | | PERn11 | A108 | | D108 |
| C109 | GND | B109 | | | GND | | GND | | | A109 | GND | D109 |
| C110 | | B110 | | PETp12 | | | | PERp12 | | A110 | | D110 |
| C111 | | B111 | PETn12 | | | | | | PERn12 | A111 | | D111 |
| C112 | GND | B112 | | | GND | | GND | | | A112 | GND | D112 |
| C113 | | B113 | | PETp13 | | | | PERp13 | | A113 | | D113 |
| C114 | | B114 | PETn13 | | | | | | PERn13 | A114 | | D114 |
| C115 | GND | B115 | | | GND | | GND | | | A115 | GND | D115 |
| C116 | | B116 | | PETp14 | | | | PERp14 | | A116 | | D116 |
| C117 | | B117 | PETn14 | | | | | | PERn14 | A117 | | D117 |
| | | KEY | KEY | KEY | KEY | KEY | KEY | KEY | KEY | KEY | | |
| C118 | | B118 | GND | | | | | | GND | A118 | | D118 |
| C119 | GND | B119 | | | GND | | GND | | | A119 | GND | D119 |
| C120 | | B120 | | PETp15 | | | | PERp15 | | A120 | | D120 |
| C121 | | B121 | PETn15 | | | | | | PERn15 | A121 | | D121 |
| C122 | GND | B122 | | | GND | | GND | | | A122 | GND | D122 |
| C123 | | B123 | | PETp16 | | | | PERp16 | | A123 | | D123 |
| C124 | | B124 | PETn16 | | | | | | PERn16 | A124 | | D124 |
| C125 | GND | B125 | | | GND | | GND | | | A125 | GND | D125 |
| C126 | | B126 | | PETp17 | | | | PERp17 | | A126 | | D126 |
| C127 | | B127 | PETn17 | | | | | | PERn17 | A127 | | D127 |
| C128 | GND | B128 | | | GND | | GND | | | A128 | GND | D128 |
| C129 | | B129 | | PETp18 | | | | PERp18 | | A129 | | D129 |
| C130 | | B130 | PETn18 | | | | | | PERn18 | A130 | | D130 |
| C131 | GND | B131 | | | GND | | GND | | | A131 | GND | D131 |
| C132 | | B132 | | PETp19 | | | | PERp19 | | A132 | | D132 |
| C133 | | B133 | PETn19 | | | | | | PERn19 | A133 | | D133 |
| C134 | GND | B134 | | | GND | | GND | | | A134 | GND | D134 |
| C135 | | B135 | | PETp20 | | | | PERp20 | | A135 | | D135 |
| C136 | | B136 | PETn20 | | | | | | PERn20 | A136 | | D136 |
| C137 | GND | B137 | | | GND | | GND | | | A137 | GND | D137 |
| C138 | | B138 | | PETp21 | | | | PERp21 | | A138 | | D138 |
| C139 | | B139 | PETn21 | | | | | | PERn21 | A139 | | D139 |
| C140 | GND | B140 | | | GND | | GND | | | A140 | GND | D140 |
| C141 | | B141 | | PETp22 | | | | PERp22 | | A141 | | D141 |
| C142 | | B142 | PETn22 | | | | | | PERn22 | A142 | | D142 |
| C143 | GND | B143 | | | GND | | GND | | | A143 | GND | D143 |
| C144 | | B144 | | PETp23 | | | | PERp23 | | A144 | | D144 |
| C145 | | B145 | PETn23 | | | | | | PERn23 | A145 | | D145 |
| C146 | GND | B146 | | | GND | | GND | | | A146 | GND | D146 |
| C147 | | B147 | | PETp24 | | | | PERp24 | | A147 | | D147 |
| C148 | | B148 | PETn24 | | | | | | PERn24 | A148 | | D148 |
| C149 | GND | B149 | | | GND | | GND | | | A149 | GND | D149 |
| C150 | | B150 | | PETp25 | | | | PERp25 | | A150 | | D150 |
| C151 | | B151 | PETn25 | | | | | | PERn25 | A151 | | D151 |
| C152 | GND | B152 | | | GND | | GND | | | A152 | GND | D152 |
| C153 | | B153 | | PETp26 | | | | PERp26 | | A153 | | D153 |
| C154 | | B154 | PETn26 | | | | | | PERn26 | A154 | | D154 |
| C155 | GND | B155 | | | GND | | GND | | | A155 | GND | D155 |
| C156 | | B156 | | PETp27 | | | | PERp27 | | A156 | | D156 |
| C157 | | B157 | PETn27 | | | | | | PERn27 | A157 | | D157 |
| C158 | GND | B158 | | | GND | | GND | | | A158 | GND | D158 |
| C159 | | B159 | | PETp28 | | | | PERp28 | | A159 | | D159 |
| C160 | | B160 | PETn28 | | | | | | PERn28 | A160 | | D160 |
| C161 | GND | B161 | | | GND | | GND | | | A161 | GND | D161 |
| C162 | | B162 | | PETp29 | | | | PERp29 | | A162 | | D162 |

## Table 2-3. PCIe Riser Card Connector and Module Pin Assignment (Sheet 4 of 4)

| C | | B | | | | A | | | | D | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| C163 | | B163 | PETn29 | | | | | PERn29 | A163 | | D163 |
| C164 | GND | B164 | | | GND | GND | | | A164 | GND | D164 |
| C165 | | B165 | | PETp30 | | | PERp30 | | A165 | | D165 |
| C166 | | B166 | PETn30 | | | | | PERn30 | A166 | | D166 |
| C167 | GND | B167 | | | GND | GND | | | A167 | GND | D167 |
| C168 | | B168 | | PETp31 | | | PERp31 | | A168 | | D168 |
| C169 | | B169 | PETn31 | | | | | PERn31 | A169 | | D169 |
| C170 | GND | B170 | | | GND | GND | | | A170 | GND | D170 |
| C171 | | B171 | | PETp32 | | | PERp32 | | A171 | | D171 |
| C172 | | B172 | PETn32 | | | | | PERn32 | A172 | | D172 |
| C173 | GND | B173 | | | GND | GND | | | A173 | GND | D173 |
| C174 | | B174 | | PETp33 | | | PERp33 | | A174 | | D174 |
| C175 | | B175 | PETn33 | | | | | PERn33 | A175 | | D175 |
| C176 | GND | B176 | | | GND | GND | | | A176 | GND | D176 |
| C177 | | B177 | | PETp34 | | | PERp34 | | A177 | | D177 |
| C178 | | B178 | PETn34 | | | | | PERn34 | A178 | | D178 |
| C179 | GND | B179 | | | GND | GND | | | A179 | GND | D179 |
| C180 | | B180 | | PETp35 | | | PERp35 | | A180 | | D180 |
| C181 | | B181 | PETn35 | | | | | PERn35 | A181 | | D181 |
| C182 | GND | B182 | | | GND | GND | | | A182 | GND | D182 |
| C183 | | B183 | | PETp36 | | | PERp36 | | A183 | | D183 |
| C184 | | B184 | PETn36 | | | | | PERn36 | A184 | | D184 |
| C185 | GND | B185 | | | GND | GND | | | A185 | GND | D185 |
| C186 | | B186 | | PETp37 | | | PERp37 | | A186 | | D186 |
| C187 | | B187 | PETn37 | | | | | PERn37 | A187 | | D187 |
| C188 | GND | B188 | | | GND | GND | | | A188 | GND | D188 |
| C189 | | B189 | | PETp38 | | | PERp38 | | A189 | | D189 |
| C190 | | B190 | PETn38 | | | | | PERn38 | A190 | | D190 |
| C191 | GND | B191 | | | GND | GND | | | A191 | GND | D191 |
| C192 | | B192 | | PETp39 | | | PERp39 | | A192 | | D192 |
| C193 | | B193 | PETn39 | | | | | PERn39 | A193 | | D193 |
| C194 | GND | B194 | | | GND | GND | | | A194 | GND | D194 |
| C195 | | B195 | | PETp40 | | | PERp40 | | A195 | | D195 |
| C196 | | B196 | PETn40 | | | | | PERn40 | A196 | | D196 |
| C197 | GND | B197 | | | GND | GND | | | A197 | GND | D197 |
| C198 | | B198 | | PETp41 | | | PERp41 | | A198 | | D198 |
| C199 | | B199 | PETn41 | | | | | PERn41 | A199 | | D199 |
| C200 | GND | B200 | | | GND | GND | | | A200 | GND | D200 |
| C201 | | B201 | | PETp42 | | | PERp42 | | A201 | | D201 |
| C202 | | B202 | PETn42 | | | | | PERn42 | A202 | | D202 |
| C203 | GND | B203 | | | GND | GND | | | A203 | GND | D203 |
| C204 | | B204 | | PETp43 | | | PERp43 | | A204 | | D204 |
| C205 | | B205 | PETn43 | | | | | PERn43 | A205 | | D205 |
| C206 | GND | B206 | | | GND | GND | | | A206 | GND | D206 |
| C207 | | B207 | | PETp44 | | | PERp44 | | A207 | | D207 |
| C208 | | B208 | PETn44 | | | | | PERn44 | A208 | | D208 |
| C209 | GND | B209 | | | GND | GND | | | A209 | GND | D209 |
| C210 | | B210 | | PETp45 | | | PERp45 | | A210 | | D210 |
| C211 | | B211 | PETn45 | | | | | PERn45 | A211 | | D211 |
| C212 | GND | B212 | | | GND | GND | | | A212 | GND | D212 |
| C213 | | B213 | | PETp46 | | | PERp46 | | A213 | | D213 |
| C214 | | B214 | PETn46 | | | | | PERn46 | A214 | | D214 |
| C215 | GND | B215 | | | GND | GND | | | A215 | GND | D215 |
| C216 | | B216 | | PETp47 | | | PERp47 | | A216 | | D216 |
| C217 | | B217 | PETn47 | | | | | PERn47 | A217 | | D217 |
| C218 | GND | B218 | | | GND | GND | | | A218 | GND | D218 |
| C219 | | B219 | | RESV | | | RESV | | A219 | | D219 |

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# 3 Connector Interface Definitions

This section defines PCIe riser connector and riser card mechanical interfaces to ensure form, fit, and function.

## 3.1 Design Essentials

The following notes apply for all drawings in this section:

1. Critical dimensions and tolerances are identified with the symbol Ⓒ, and are required to meet Cpk ≥1.00.
2. Dimensions and tolerances conform to ASME Y14.5-2009.
3. All dimensions are in millimeters (mm) unless identified otherwise.
4. All dimension tolerances are ±0.15 mm unless specified otherwise.

## 3.2 PCIe* Riser Card Connector Dimensions

The PCIe riser card connector is defined for applications that require a vertical entry of a riser card into the connector. Figure 3-1 illustrates a 3-dimensional image of such a connector. Figure 3-2 shows connector outline.

**Figure 3-1. PCIe Riser Card Connector and Riser Card**

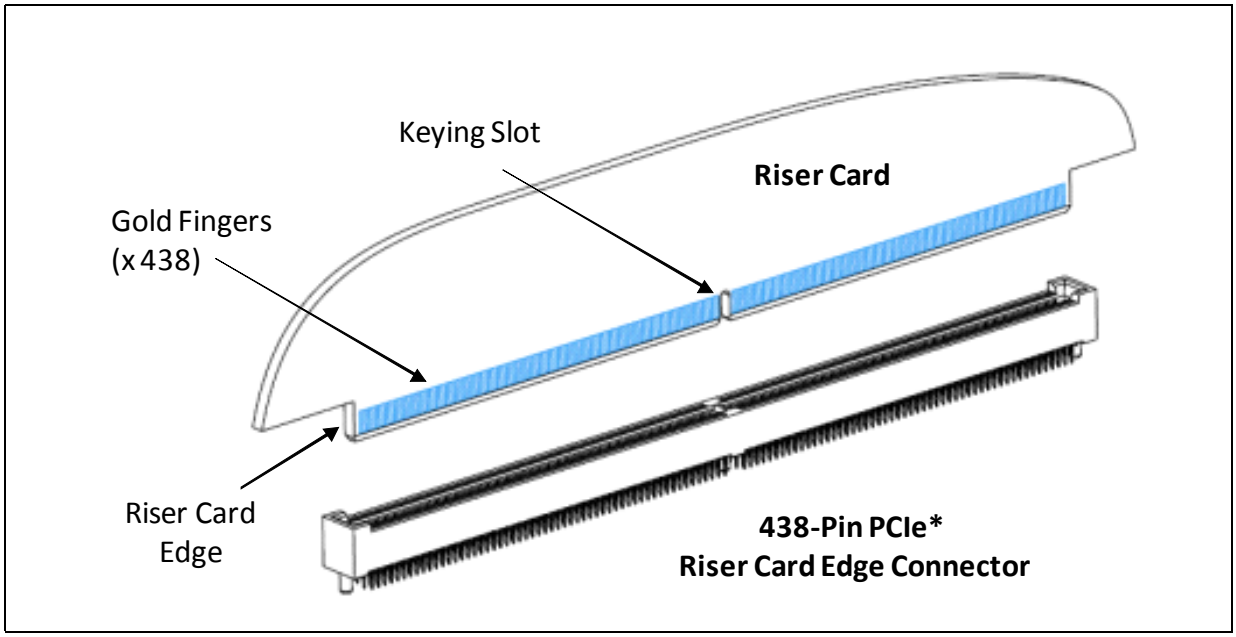
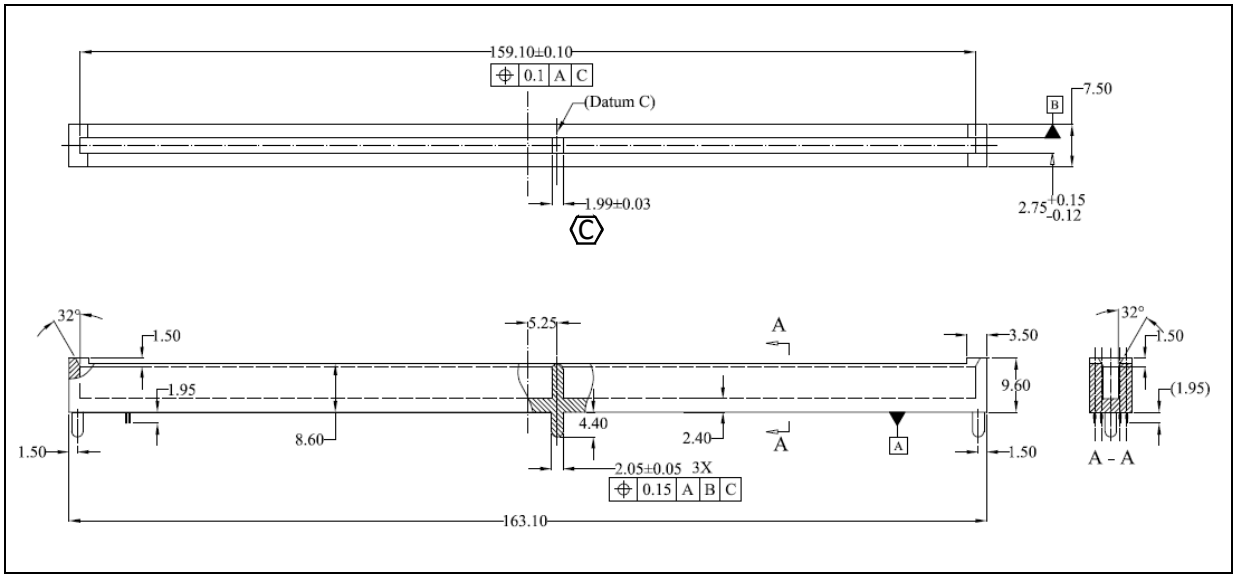


**Figure 3-2. PCIe Riser Card Connector Dimensions**




The outer locus of the PCIe riser connector contact at interface with the riser card should be ≤0.38 mm to prevent any shorts during the riser card insertion into the connector. Contact outer locus at the riser card interface is the maximum zone where contact could locate, which is controlled by housing cavity size, pin size, and housing cavity position tolerance referenced to datum key.

## 3.3 PCIe Riser Connector Baseboard Footprint

As a press-fit type connector, the PCIe riser connector relies on a mechanical interference fit between the pin on the connector and the plated through-hole (PTH) in the board to ensure electrical connection between the connector and board is made. Board finish can affect both mechanical and electrical performance of the connector.

Connector footprint and board hole details are shown in Figure 3-3. Additional board space is needed for the connector installation and removal tool. The recommended baseboard keepout zones are shown in Figure 3-4 and Figure 3-5.

## Figure 3-3. PCIe Riser Connector Footprint (Top View)

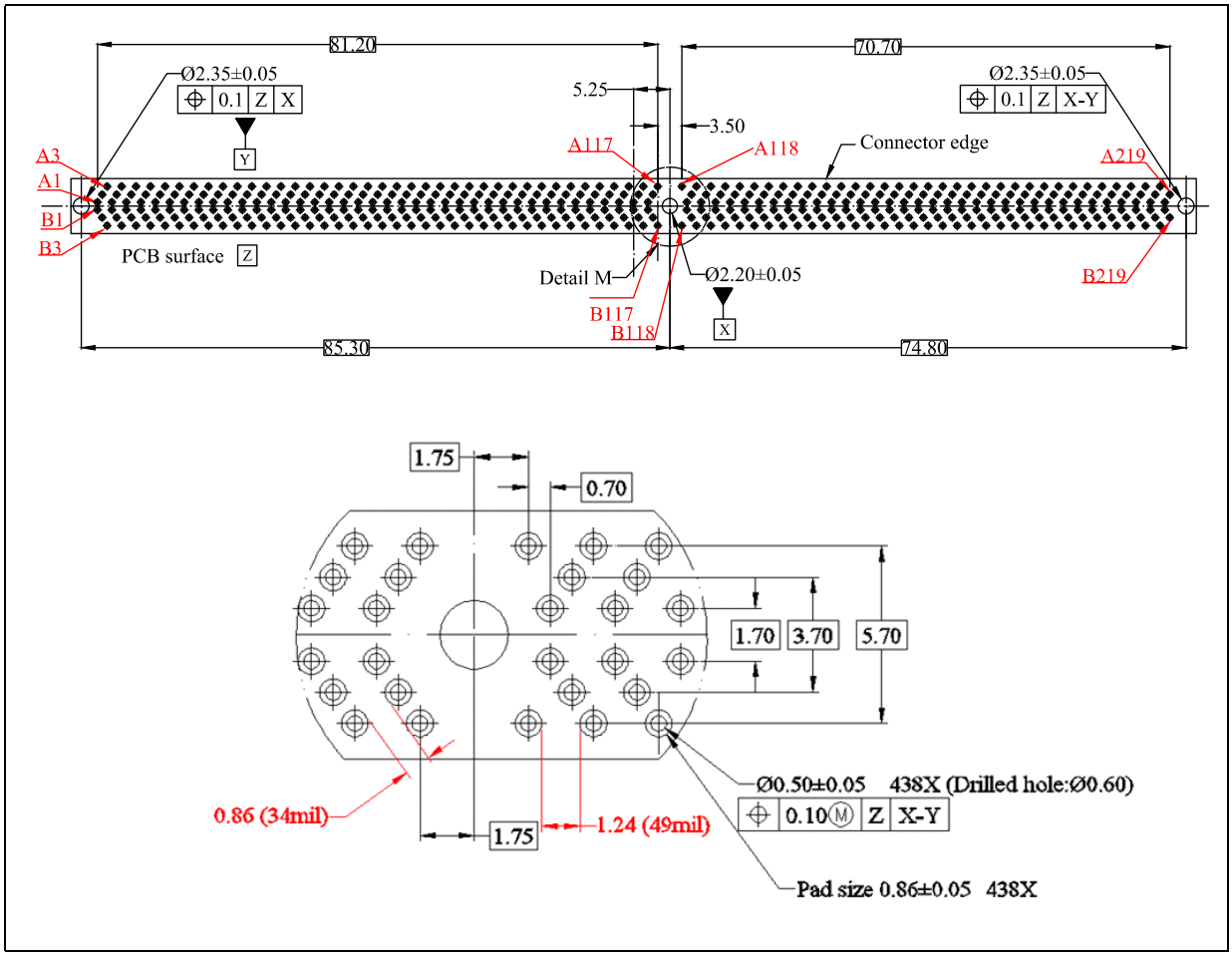
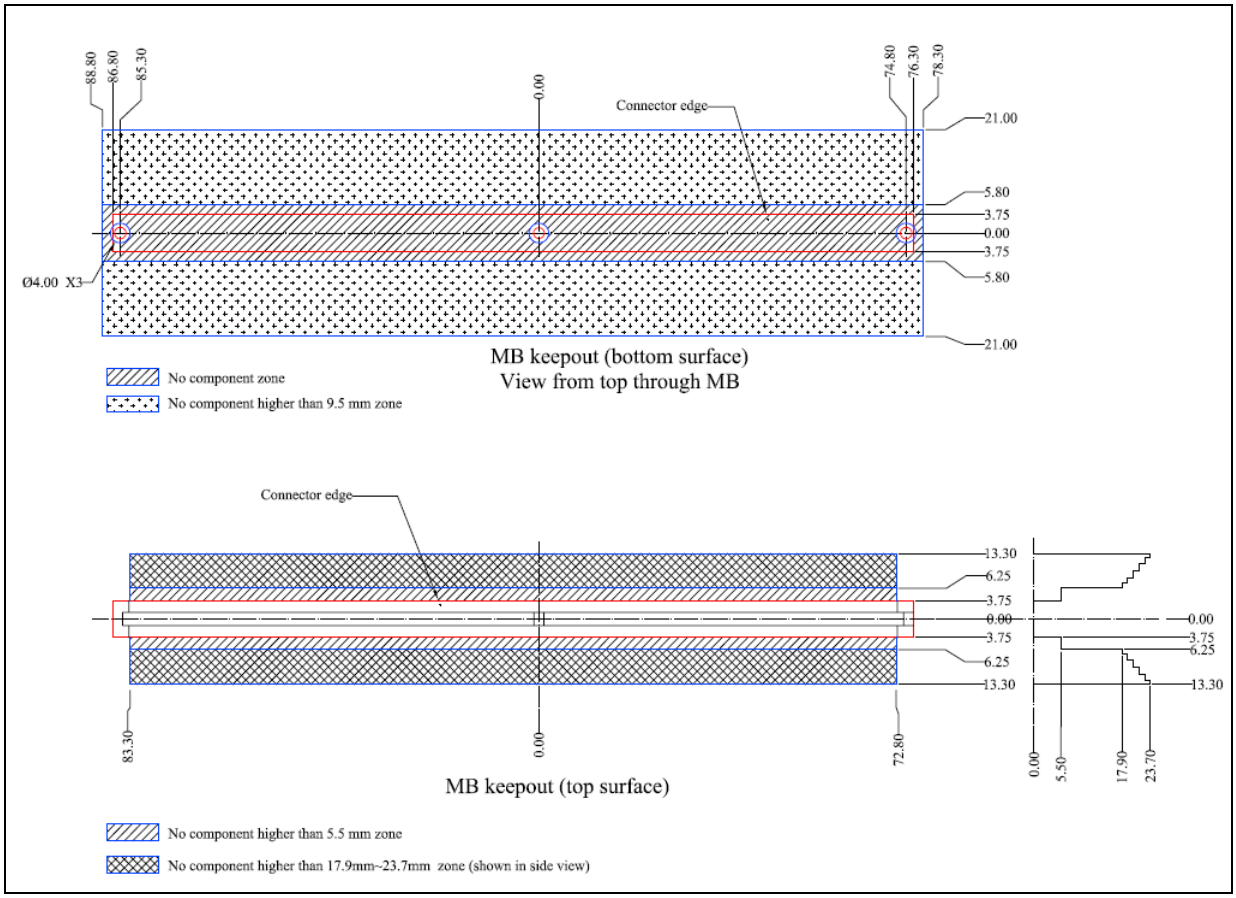
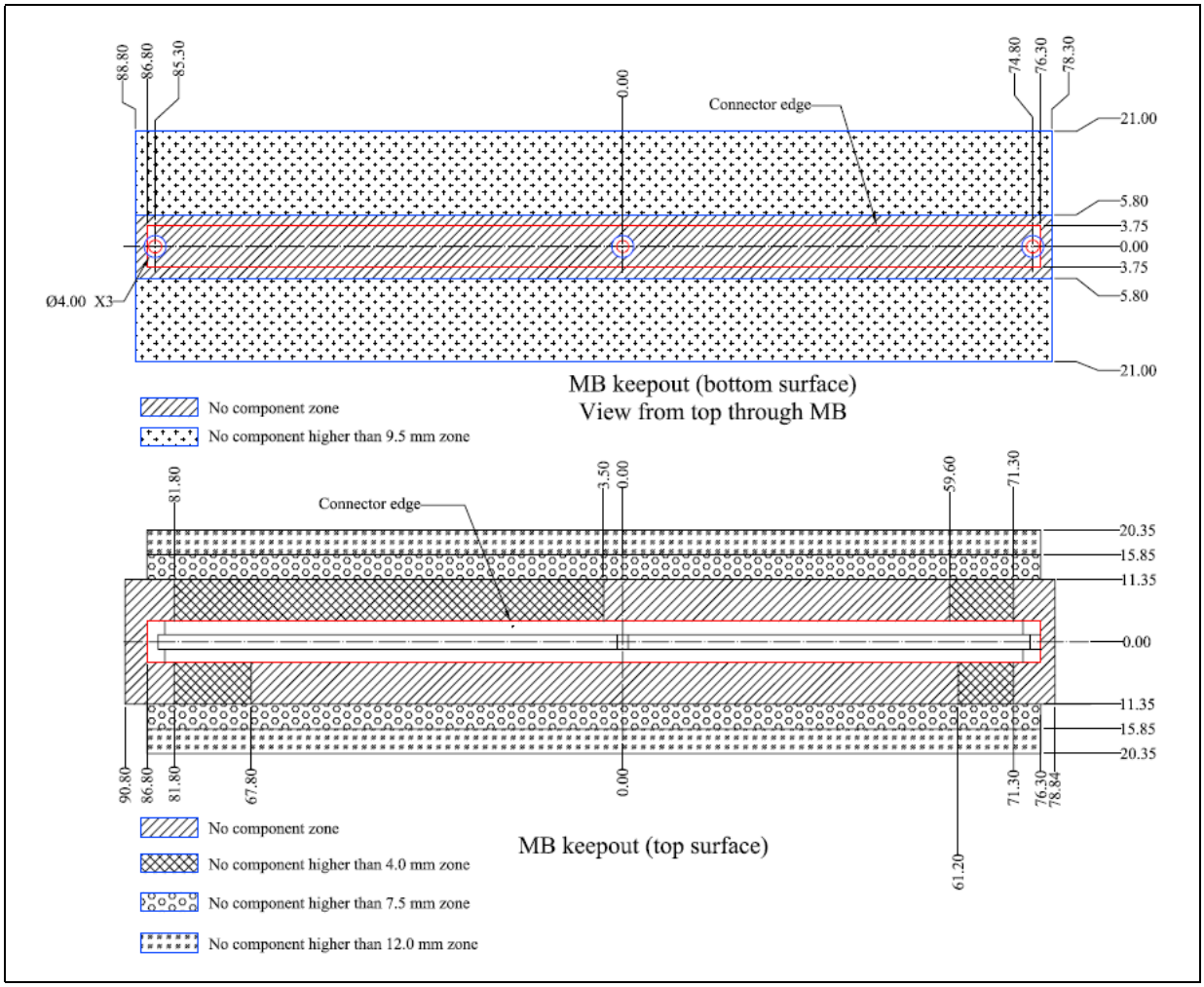


**Figure 3-4. System Board Keepout Zone for Assembly**



### Figure 3-5. System Board Keepout Zone for Rework




The PCIe riser connector relies on specific pad sizes and plating types to achieve reliable solder joints between the connector and the baseboard. See the manufacturer's drawings for specific through-hole drill/pad/antipad sizes and board finish types. Figure 3-6 illustrates a 438-pin PCIe riser card breakout routing on 5 mil lines with 7 mil spacing.

**Figure 3-6. PCIe Riser Connector Breakout Routing**

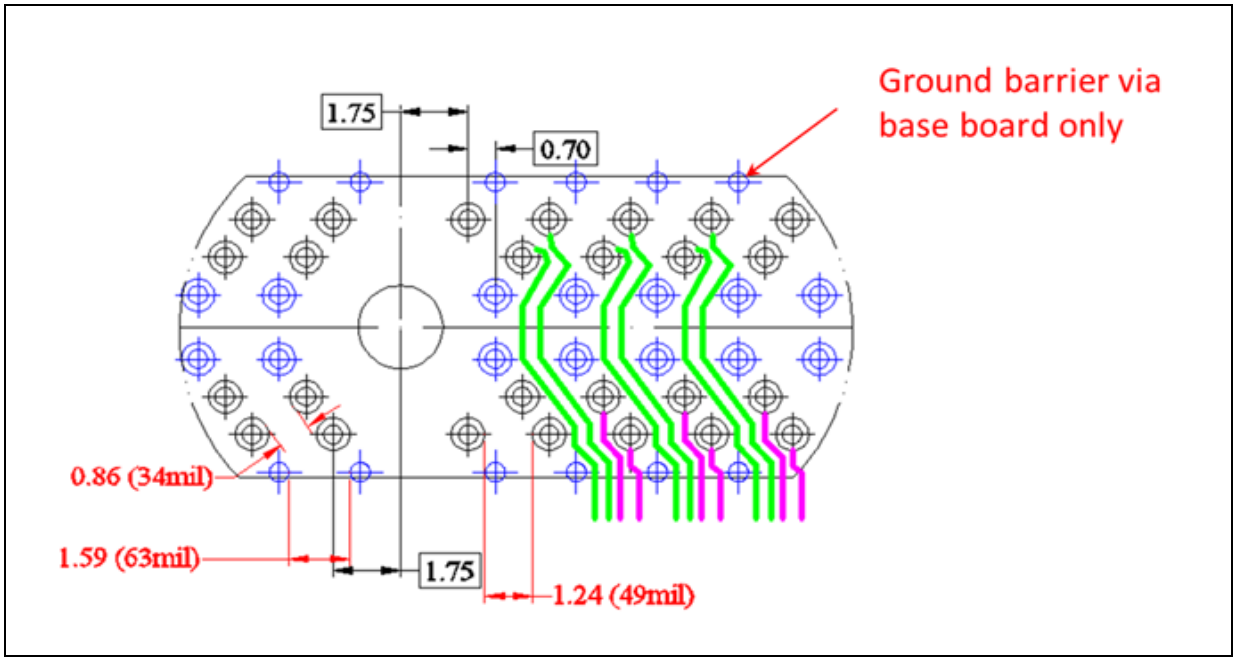
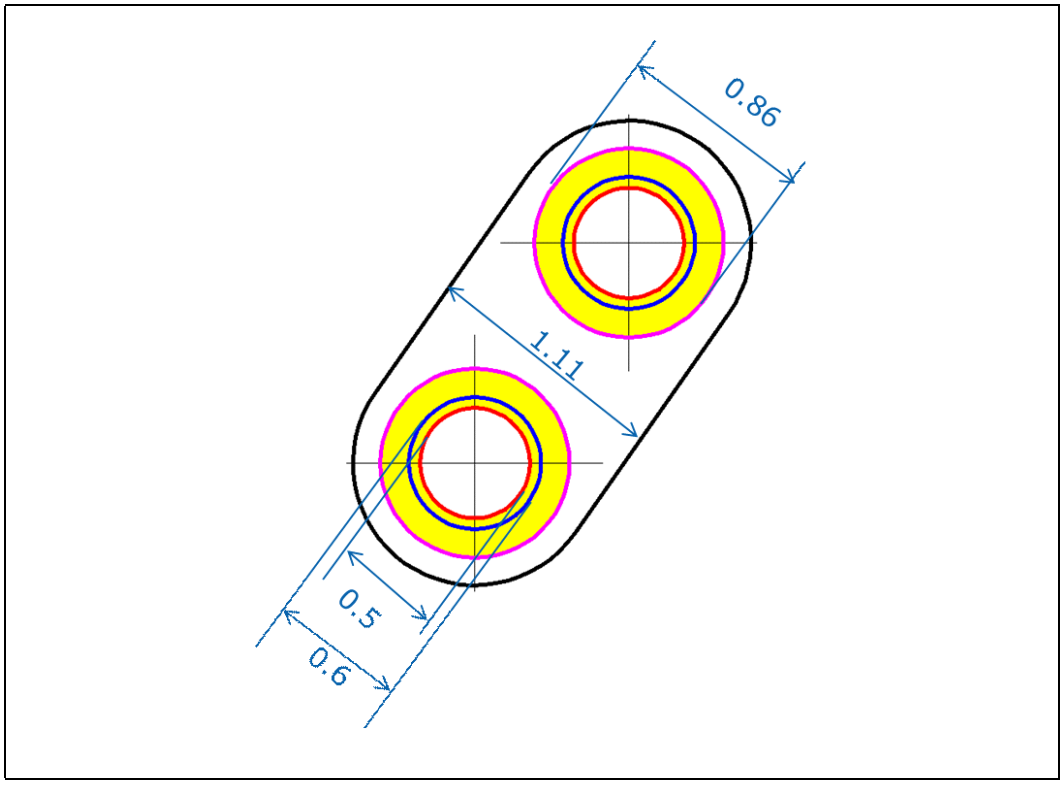



Figure 3-7 illustrates hole dimensions for a 438-pin PCIe riser connector pin with 0.5 mm finished hole diameter, 0.6 mm drill diameter, 0.86 mm pad diameter, and 1.11 mm paired antipad dimensions used on p-n differential pairs.

**Figure 3-7. PCIe Riser Connector Pin Baseboard Hole Specification**



## 3.4 PCIe 3.0 Riser Card Dimensions

The gold finger0 positional tolerance is identified as a critical riser card dimension. Gold finger position in relation to riser card edges is critical to ensure each connector contact is properly lined up with its gold finger. The PCIe riser card mechanical dimensions are shown in Figure 3-8, Figure 3-9, and Figure 3-10. The detailed explanation of the gold finger positional tolerance is provided in Appendix A.

An external tie bar will be needed on the riser card's top/bottom layer; an inner tie bar is not allowed for gold plating.

Minimum required gold finger plating is 30 µin of gold over 100 µin of nickel. Connector and riser card are to be tested per industry standard EIA 364-1000.

**Figure 3-8. PCIe 3.0 Riser Card Dimensions**

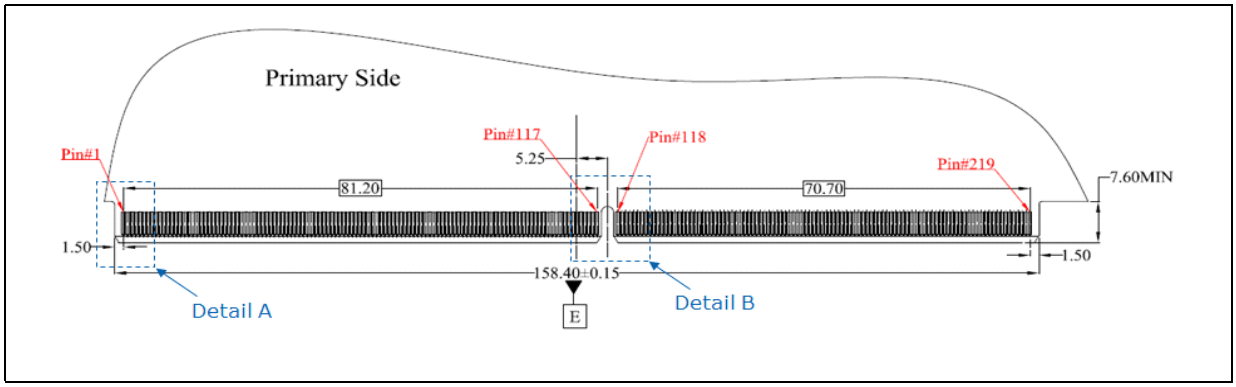



**Figure 3-9. PCIe 3.0 Riser Card Dimensions (Detail A)**

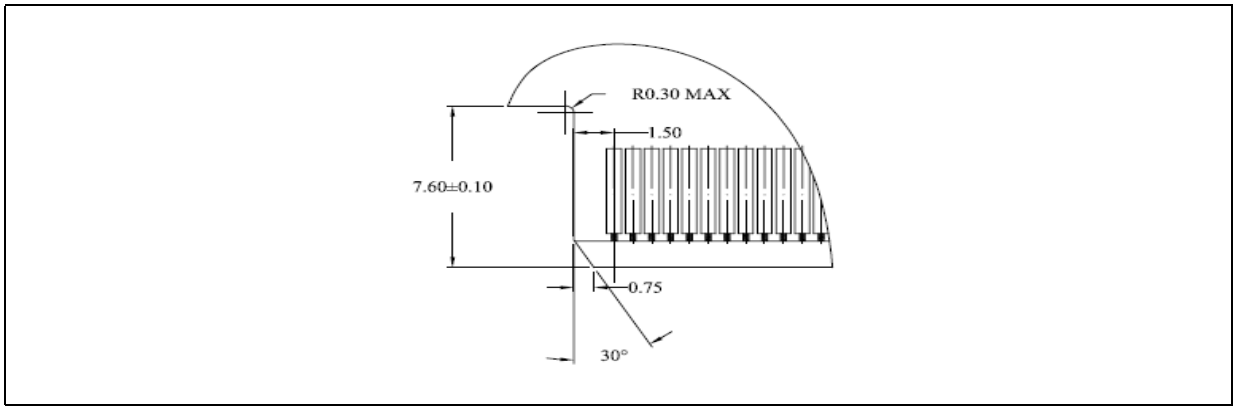
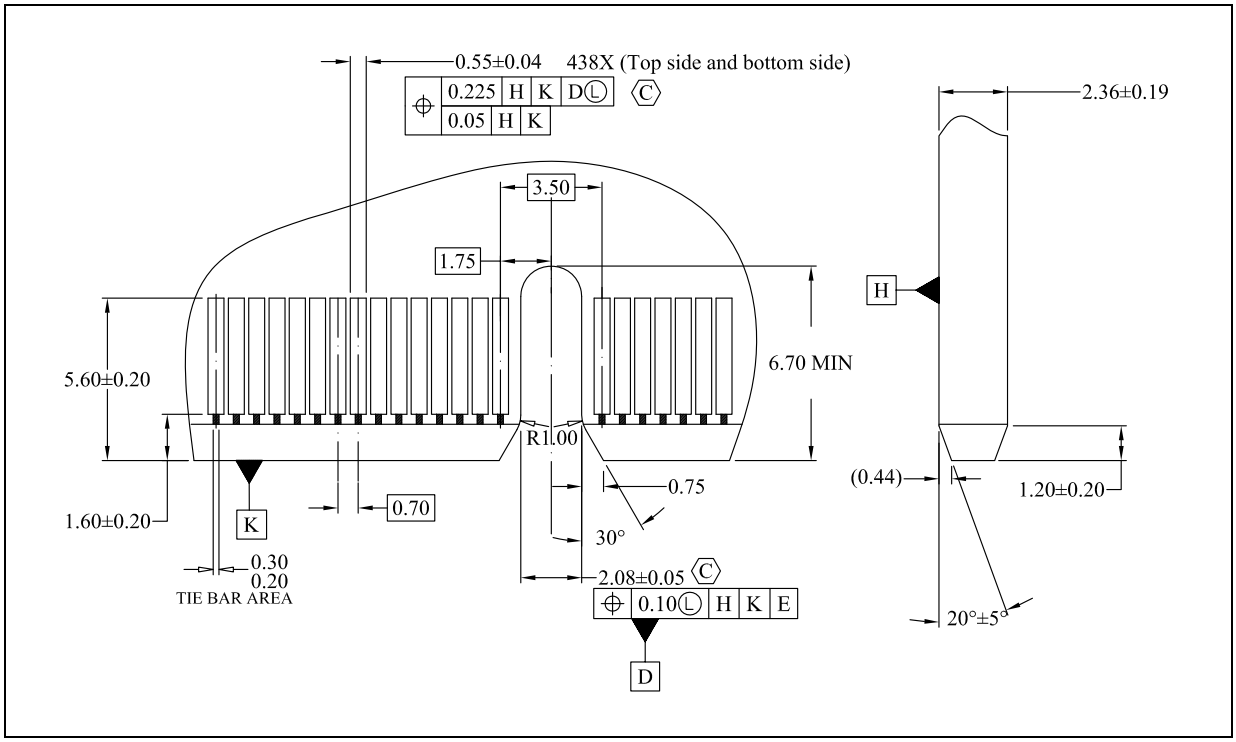


**Figure 3-10. PCIe 3.0 Riser Card Dimensions (Detail B)**

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# 4 Electrical Specification

A common electrical test fixture is specified in the PCIe 3.0 connector signal integrity PCIe 3.0 Connector High-Speed Electrical Test Procedure. This fixture is used for evaluating the connector compliance to the DC and AC electrical requirements specified in this section.

This section specifies the PCIe riser connector electrical requirements including connector impedance, contact resistance, current carrying capacity, and the parasitic requirements.

## 4.1 DC Electrical Requirements

Table 4-1 outlines the signal integrity parameters, requirements, and test procedures in qualifying the PCIe riser connector DC electrical requirements.

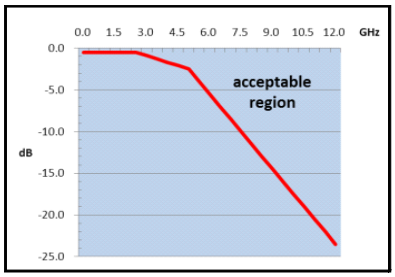
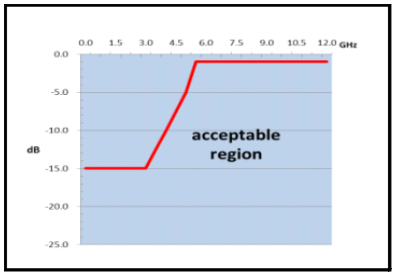
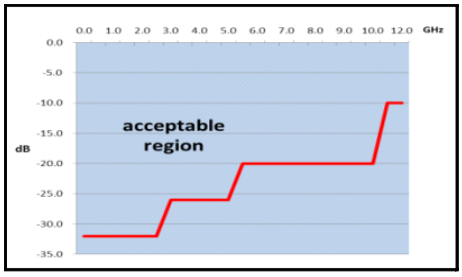
**Table 4-1. DC Electrical Requirements**

| Parameter | Requirements | Procedure |
|---|---|---|
| Low level contact resistance (LLCR) | Initial: 20 milliohms max for a mated connector<br>The resistance change, which is defined as the change in LLCR between the reading after stress and the initial reading, shall not exceed 10 milliohms. | EIA 364- 23B<br>Subject mated contacts assembled in housing to 20 mV max open circuit at 100 mA max |
| Current rating | 1.1 A per contact minimum.<br>The temperature rise above ambient shall not exceed 30°C. The ambient condition is still air at 25°C.<br>With pin-out as shown in Table 2-3 | EIA 364-70 method 2<br>Test the mated connector:<br>1. The sample size is a minimum of three mated connectors.<br>2. The sample shall be press-fit on a PC board with the appropriate footprint.<br>3. Wire all the power and all the ground pins in a series circuit.<br>4. A thermocouple of 30 AWG or less shall be placed as close to the mating contact as possible.<br>5. Conduct a temperature rise versus current test. |
| Withstand voltage | 500 V min | EIA364-20 |
| Insulation resistance | 1-Mohm min | EIA364-21 |
| Intra-pair skew | ≤5 ps | Refer to *PCIe* Gen 3 Connector High-Speed Electrical Test Procedure*, Intel document #325028. |

## 4.2 AC Electrical Requirements

Table 4-2 lists the AC electrical requirements for the PCIe riser connector. For measurement methodology, see Intel reference document *PCIe* Gen 3 Connector High-Speed Electrical Test Procedure*.

**Table 4-2. Connector Single-ended S-parameter Values**

| S-Parameter | Procedures | Requirement |
|---|---|---|
| Differential insertion loss (DDS21)[3] | Notes: 1, 2, and 3 |  <br>≥ -0.5 dB 0 GHz < f < 2.5 GHz;<br>≥ -[0.8*(f-2.5)+0.5] 2.5 GHz < f ≤5 GHz;<br>≥ -[3.0*(f-5)+2.5] dB for 5 GHz < f ≤12 GHz. |
| Differential return loss (DDS21)[3] | Notes: 1, 2, and 3 |  <br>≤ -15 dB up to 3.0 GHz;<br>≤ 5*f - 30 dB for 3.0 GHz < f ≤ 5 GHz;<br>≤ -1 dB for 5.0 GHz < f ≤ 12 GHz. |
| Cross-talk multiple aggressor pairs (Next_ma)[3] | Notes: 1, 2, 3, and 4 |  <br>≤ -32 dB up to 2.5 GHz;<br>≤ -26 dBfor 2.5 GHz < f ≤ 5.0 GHz;<br>≤ -20 dB for 5.0 GHz < f ≤ 10 GHz;<br>< -10 dB for 10 GHz < f ≤ 12 GHz. |

***Notes:***
1. A common test fixture for connector characterization shall be used.
2. Effects of the baseboard through-hole via and module gold edge finger are included.
3. Specification presumes the data is normalized to 42.5 ohm (85 ohm differential).
4. The crosstalk requirement includes contributions from all adjacent differential pairs.

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# 5 Mechanical, Environmental, and Reliability Specification

This section specifies the riser card connector's mechanical and environmental requirements. A 7-year life cycle test is applied for both the mechanical requirement and the environmental requirement, per EIA 364-1000.

## 5.1 Mechanical Specifications

The PCIe riser card connector mechanical requirements include the riser card mating force and durability. The PCIe riser card connector must comply with the mechanical requirements listed in Table 5-1.

***Note:*** The sample size shall follow the requirements in Section 2.2.1 of EIA-364-1000.

**Table 5-1. Mechanical Specifications**

| Parameter | Value | Notes |
|---|---|---|
| Volumetric and mechanical dimensions | For mechanical dimensions see Section 3 and drawings. | Visual and dimensional inspection, Procedure EIA364-18 visual, dimensional per applicable quality inspection plan, Requirement: meets drawing |
| Insertion force (riser card to connector) | 30 kgf max | Test per EIA 364-13<br>Measure the force necessary to mate the connector assemblies at a maximum rate of 2.54 cm per minute<br>Riser card gauge thickness 2.58 mm ±0.02 |
| Normal force per contact | 50 gf min (EOL) | Test per EIA 364-04 |
| Retention force – terminal pin | 300 gf min per pin | Test per EIA 364-29<br>No movement of contact greater than 0.38 mm |
| Unmate force (riser card removal from connector) | 2 kgf (~min) | Test per EIA 364-13<br>Measure the force necessary to unmate the connector assemblies at a maximum rate of 2.54 cm/minute |
| Durability | 30 cycles over connector life time | Use one riser card and one connector |

Additionally, the PCIe riser card connector must meet the material requirements listed in Table 5-2 to ensure compliance with industry standards and regulations.

**Table 5-2. Material Requirements**

| Parameter | Requirement | Notes |
|---|---|---|
| Marking | Connector marking must contain:<br>• Manufacturer's insignia<br>• Part number<br>• Date code<br>All markings must withstand typical environmental, mechanical, and reliability tests.<br>All markings must be visible after mounting. | |
| Flammability | UL 94 V-0 | Material certification or certification of compliance is required with each lot to satisfy the Underwriters Laboratories follow-up service requirements. |
| RoHS compliant | RoHS compliant per IEC 62474 | RoHS Directive (2011/65/EU) |
| Low halogen | 1000 ppm max Cl when used in a flame retardant.<br>1000 ppm max Br when used in a flame retardant.<br>Per JS-709A Standard - Clause 4. | Sample combustion followed by ion chromatography as specified by: British Standard Methods BS EN 14582:2007, Characterization of waste – Halogen and sulfur content – Oxygen combustion in closed systems and determination methods OR US EPA-5050 (BOM Preparation Method for Solid Waste). |

## 5.2 Environmental Requirements

Connector environmental tests shall follow EIA-364-1000, Groups 1 through 6 Environmental Test Methodology for Assessing the Performance of Electrical Connectors and Sockets Used in Business Office Applications. The test groups/sequences and durations shall be derived from the following application requirements:

- Field temperatures of 65°C
- Field life of 7 years
- Operating temperature range of -55°C to +85°C
- Storage temperature range of 15°C to 28°C RH at 65%.

Both the plating thickness and the baseboard thickness shall be recorded in the environmental test report.

## 5.3 Reliability Requirement

The PCIe riser card connector reliability test conditions — used in the completion of ANSI/EIA-364-1000 test groups 1 through 5 — are described in Table 5-3. After reliability testing, the connector under test must meet electrical, mechanical, and environmental criteria.

## Table 5-3. Reliability Test Conditions

| Test Description | Test Condition | Notes |
|---|---|---|
| Durability | Test per ANSI/EIA-364-09<br>precondition 5 plug/unplug cycles | No evidence of physical damage. |
| Temperature life | ANSI/EIA-364-17, Method A (without electrical load)<br>Test: 105°C, 120 hrs<br>Precondition: 105°C, 72 hrs<br>perform in mated condition | |
| Low-level contact resistance (LLCR) | ANSI/EIA-364-23 Option 1, 4-wire method. | Termination of connector to board carrier shall be included in the measurement. |
| Physical shock | ANSI/EIA-364-27, Test Condition A, Half Sine, duration 11 ms, 100 mA load, 3 drops each axis normal and reversed directions, perform in mated condition. | |
| Vibration | ANSI/EIA-364-28 Test Condition D<br>5 Hz @ 0.02 $g^2$/Hz to 20 Hz @ 0.02 $g^2$/Hz (slope up)<br>20 Hz to 500 Hz @ 0.02 $g^2$/HZ (flat)<br>Input acceleration is 3.10 g RMS.<br>Both halves rigidly fixed.<br>15 Minutes per axis on all 3 axes (X, Y, Z).<br>Random control limit tolerance is ±1.5 dB.<br>Continuity check: Electrical load 100 milliamperes for all contacts. | No discontinuities of ≥1 microsecond. |
| Cyclic temperature and humidity | ANSI/EIA-364-31B, Method III without conditioning, initial measurements, cold shock, and vibration. Ramp times should be 0.5 hour and dwell times should be 1.0 hour. Dwell times start when the temperature and humidity have stabilized within specified levels, perform 10 cycles in mated condition. | |
| Thermal shock | ANSI/EIA-364-32, Method A, Table2, Test Condition 1, -55°C to +85°C, perform 5 cycles in mated condition. | |
| Thermal disturbance | ANSI/EIA-364-1000 Cycle the connector between 15 ±3°C and 85 ±3°C, as measured on the part. Ramps should be a minimum of 2°C/minute. Dwell times should ensure that the contacts reach the temperature extremes (a minimum of 5 minutes), humidity is not controlled, perform 10 cycles in mated condition. | |
| Thermal cycle | ANSI/EIA-364-1000 Cycle the connector between 15 ±3°C and 85 ±3°C, as measured on the part. Ramps should be a minimum of 2°C/minute. And dwell times should ensure that the contacts reach the temperature extremes (a minimum of 5 minutes), humidity is not controlled, perform 500 cycles in mated condition. | |
| Mixed flowing gas | ANSI/EIA-364-65, class IIA, Option 4, perform in mated condition, duration 7 days. | |
| Dust | ANSI/EIA-364-91<br>Condition: Unmated<br>Dust Composition: #1<br>Test Duration: 1 hr 15 minutes<br>Test per group D (LLCR) | This test applies to connectors having lubricated contacts. Use testing of non-lubricated connectors as control mechanism. |

## 5.4 Riser Card Mechanical Requirements

The connector will not provide structural support for the riser card or cards that plug into the riser card. The system/chassis must provide structural support.

**Table 5-4. Riser Card Mechanical Requirements**

| Description | Requirement | Test Procedure |
|---|---|---|
| Riser card insertion/ extraction/retention | Must be used in any use condition.<br>Chassis/system must provide general alignment of riser card to connector, but riser slot to connector key interface must be allowed to provide final riser card position reference. | EIA 364-27, EIA364-28<br>Appropriate conditions to model use condition and system configuration. |
| Riser card mass limit | 2.9 lb max | Card and all components, including thermal solutions. |
| Riser card keepouts | Meet applicable inspection plan. | EIA 364-18<br>Visual, dimensional per applicable quality inspection plan. |

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# 6 Supplier Contact Information

## 6.1 Supplier Contact and Part Number Information

Third-party supplier has been enabled to ensure the PCIe riser card connector is available.

***Note:***

1. Supplier listing is provided by Intel as a convenience to its customers. Intel does not make any representations or warranties whatsoever regarding the quality, reliability, functionality, or compatibility of the connector.
2. All part numbers listed are subject to change.
3. Supplier information provided in the table was accurate at the time of release of this document.
4. Customers planning to use the PCIe riser card connector should contact the supplier for the latest information on their products.
5. Customers must evaluate the connector performance against their own product requirements.

**Table 6-1. Connector Part Number and Supplier Contact Information**

| Component | Part Number | | |
|---|---|---|---|
| | Description | Lotes | Intel |
| Connector | 30 u" min Gold, with Lube, Metal Key | APCI0011-P006C01 | G57033-003 |
| | 30 u" min Gold, Metal Key | APCI0011-P004C01 | G57033-002 |
| | 30 u" min Gold, Plastic Key | APCI0011-P002C01 | G57033-001 |
| Assembly Tool | Lotes part number: | G02-001-765 | |
| Rework Tool | Lotes part number: | G02-001-766 | |

***Note:*** Connector contact gold plating thickness, use of the metal key vs Plastic key, and applying lubrication to the contacts have shown to improve mechanical reliability of the connector. It is at the discretion of the customer to identify, select, and verify which version of the connector is best-suited for use in their application.

**Supplier Contact:**

Cathy Yang

Address: No. 526 North of Jinling Road, Nansha District, Guangzhou
Guangdong Province, China 511458

Phone: 86-20-84686519

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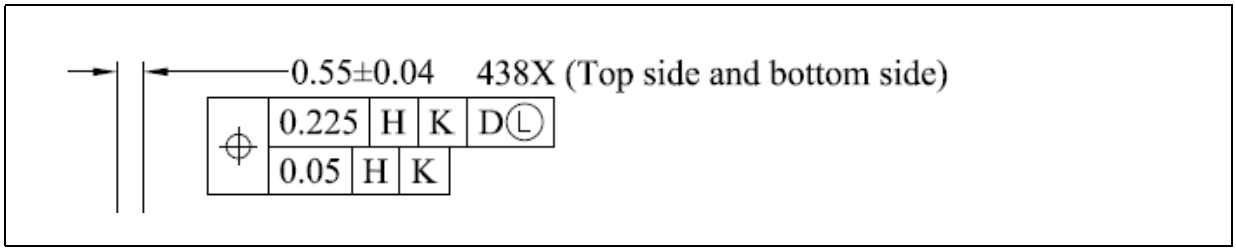
# A Riser Card Gold Finger Positional Tolerance

Dimensions of the PCIe riser card edge are provided in Section 3.4. Detailed gold finger positional tolerance is shown in Figure A-1 and Figure A-2. Least material condition (LMC) is applied to Datum D, which will introduce bonus tolerance on gold finger positional tolerance. The dimensioning is for use only as reference by the board manufacturers since it is not in compliance with geometric dimensioning and tolerances (GD&T).

In situations where the riser card notch is at LMC and where the notch width is 2.13 mm, the allowed gold finger positional tolerance is 0.225 mm (or ±0.113 mm). When the riser card notch is at nominal dimension (2.08 mm), the allowed positional tolerance is 0.275 mm (or ±0.137 mm). In situations where the riser card notch is at maximum material condition and where the notch width is 2.03 mm, the allowed positional tolerance is 0.325 mm (or ±0.162 mm). As a reference, Table A-1 lists the allowed gold finger positional tolerances (B) with respect to the riser card notch width dimension (A).

**Figure A-1. Gold Finger Size and Positional Tolerance**



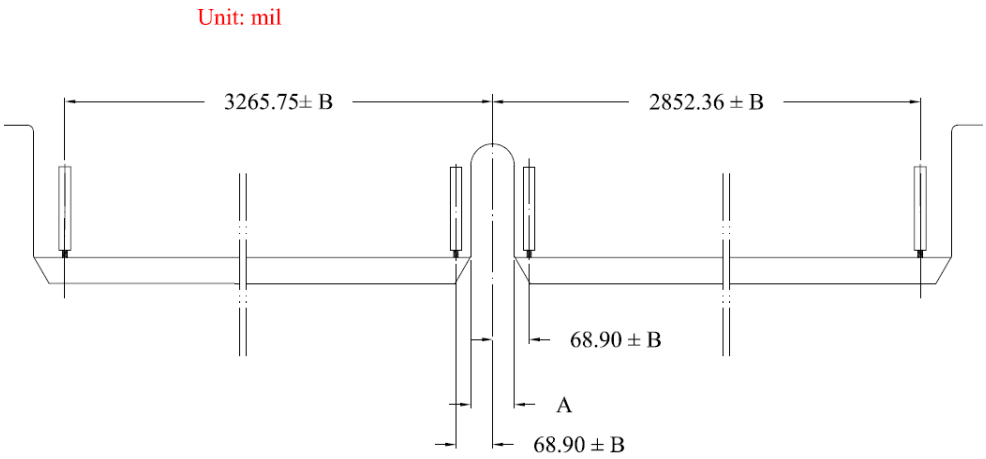

Where:

Datum H is riser card surface

Datum K is riser card bottom edge

Datum D is riser card notch center line

### Figure A-2. Gold Finger Location Tolerance




### Table A-1. Allowed Gold Finger Positional Tolerance

| Notch width (A) | | Allowed B | | Note |
|---|---|---|---|---|
| mil | mm | mil | mm | |
| 83.86 | 2.13 | 4.43 | 0.113 | Maximum notch width |
| 83.66 | 2.13 | 4.53 | 0.115 | |
| 83.46 | 2.12 | 4.63 | 0.118 | |
| 83.27 | 2.12 | 4.72 | 0.120 | |
| 83.07 | 2.11 | 4.82 | 0.123 | |
| 82.87 | 2.11 | 4.92 | 0.125 | |
| 82.68 | 2.10 | 5.02 | 0.128 | |
| 82.48 | 2.10 | 5.12 | 0.130 | |
| 82.28 | 2.09 | 5.22 | 0.133 | |
| 82.09 | 2.09 | 5.31 | 0.135 | |
| 81.89 | 2.08 | 5.41 | 0.137 | Nonimal notch width |
| 81.69 | 2.08 | 5.51 | 0.140 | |
| 81.50 | 2.07 | 5.61 | 0.142 | |
| 81.30 | 2.07 | 5.71 | 0.145 | |
| 81.10 | 2.06 | 5.81 | 0.147 | |
| 80.91 | 2.06 | 5.91 | 0.150 | |
| 80.71 | 2.05 | 6.00 | 0.152 | |
| 80.51 | 2.05 | 6.10 | 0.155 | |
| 80.31 | 2.04 | 6.20 | 0.157 | |
| 80.12 | 2.04 | 6.30 | 0.160 | |
| 79.92 | 2.03 | 6.40 | 0.162 | Minimum notch width |

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# B Riser Card Installation

## B.1 Riser Card Installation Guide

There are different alignment orders to guide the riser card into PCIe riser card connector, and to support the riser card during the shock and vibration conditions.

***Note:*** Blind mating of riser card to the connector requires alignment features.

1. Chassis will have to provide the first order of guidance for the riser card to ensure it is properly oriented and aligned to the connector.
2. The second order of guidance is provided by the connector end towers with riser card edge chamfers. Chassis guides and insertion features must allow the riser card to freely move into its correct position with respect to the connector open slot.
3. Connector key to riser card slot provides the final, third order, guidance. Once the riser card notch locates to the key, the center of the riser card should be properly aligned with the center of the connector. This is considered the "SET" position before full engagement, as shown in Figure B-2. This step is critical and needs additional caution by the installer to ensure proper engagement is made before the load is applied.
4. Apply uniform load to fully engage the riser card to the connector.
5. Secure the riser card assembly in the final fully seated position.

## B.2 Riser Card Pre-alignment Mechanism

Guide features are required for the riser card to align the card slot to the connector keying feature before insertion load is applied.

Dimensions and tolerances of the chassis guide features must be such that at the worst case condition the offset between the board slot in middle of the riser card and the center of connector key is less than 1.5 mm, as shown in Figure B-1. Any offset >1.5 mm will require the position of the rise card be adjusted manually to align with the connector before applying insertion load. All allowed positions of the card guide must enable the slot on the riser card and connector key to fully align without interference (overconstraint).

**Figure B-1. Riser Card Notch to Connector Keying Alignment**

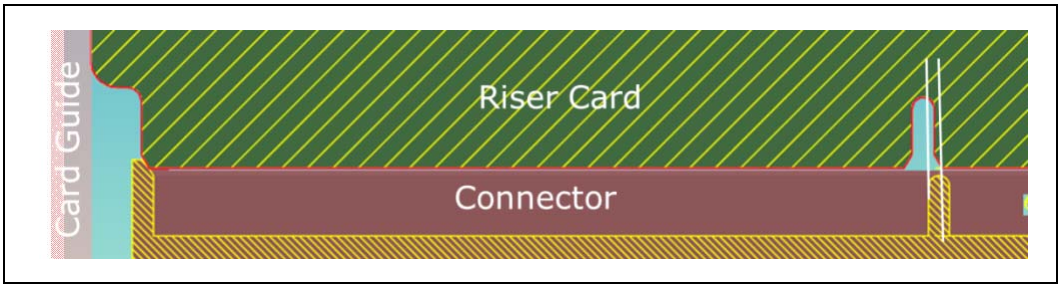
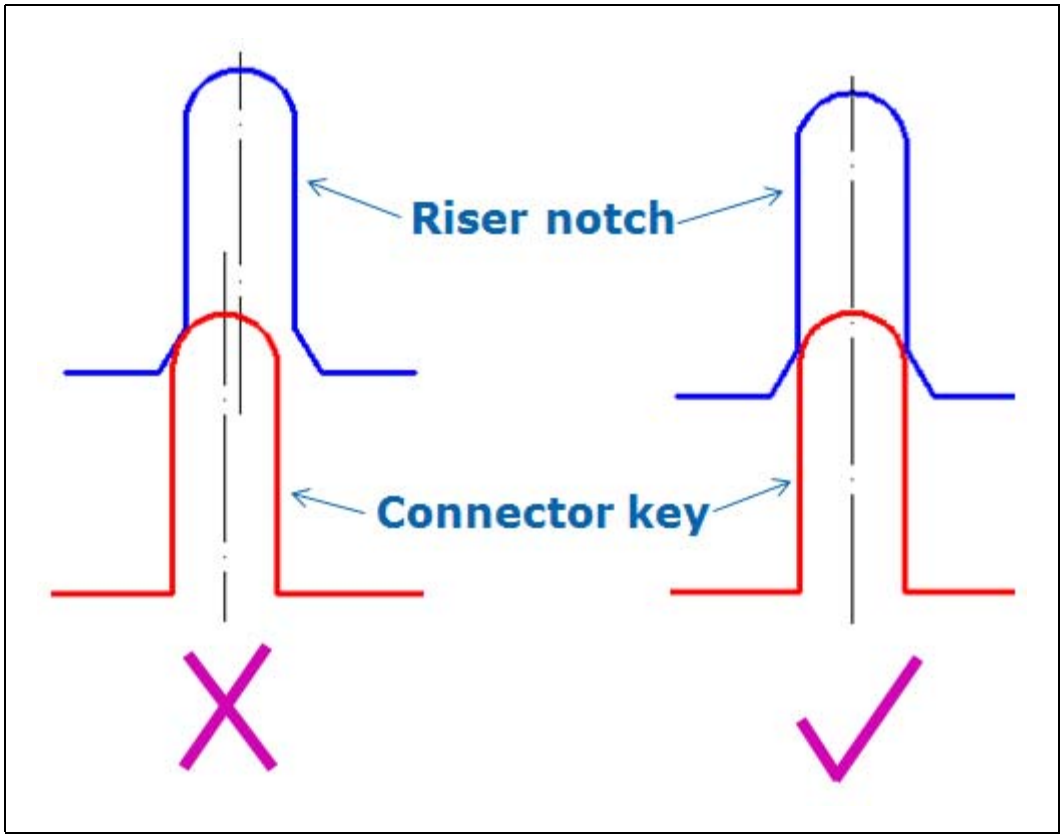


**Figure B-2. Proper Alignment Between Riser Card Notch and Connector Keying**




## B.3 Insertion/Extraction Mechanism

Because of the connector high pin count, the insertion/extraction forces exceed the ergonomic limits for a manual installation operation. Additionally, manual insertion/extraction has high possibility of rocking the riser card, which may damage the connector contacts or gold fingers, and possibly cause misalignment risk.

A mechanically assisted insertion/extraction mechanism is recommended in all use conditions. The mechanism should provide mechanical advantage to bring loads within the required ergonomic limits. The mechanism should also be designed such that it does not introduce lateral force on the connector.

Additional caution is required to ensure the riser card is uniformly inserted into the connector during insertion/extraction such that all connector contacts simultaneously engage with gold fingers.

## B.4 Retention Mechanism

Retention mechanism from the chassis (system) is required to provide the riser card with mechanical structural support. The retention mechanism will reduce the shock and vibration risks by securing the riser card to the chassis.

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# C Shock and Vibration Test Methodology

This section describes the applied physical shock and vibration (S&V) test methodology to applied to verify the connector compliance with its environmental specification.

## C.1 Test Equipment

1. Vibration Machine
2. S&V Test Fixture
3. Riser Test board with appropriate dimensions and mass representing the riser card mechanical specifications. Figure C-2 illustrates a block of aluminum attached to the a PCB representing a typical mass of component on the riser card.

   ***Riser test board dimensions:***

   Length: 225 mm

   width: 160 mm

   ***Riser test board Mass:*** 1.32 kg
4. Connector Test Board with a connector

## C.2 Test Environment

Temperature: Room temperature (21 to 24 °C)

Relative Humidity: 60-65 % RH (recommended)

## C.3 Test Conditions

See connector Physical Shock and Vibration testing requirements specified in the reliability requirement section of this document and ANSI/EIA-364 test procedures.

## C.4 Test Fixture

A test fixture is required to support and constrain the riser card movement with respect to the connector mounted on a base board. The fixture shall mimic the riser card support structure and tolerances. Figure C-1 illustrates a fully constrained riser card movement in X, Y, and Z axis. A gap of approximately 1mm is provided in the PCB slot to ensure the riser card is fully seated in the connector.

**Figure C-1. Riser Test Card Allowable Movement in Z-Axis**

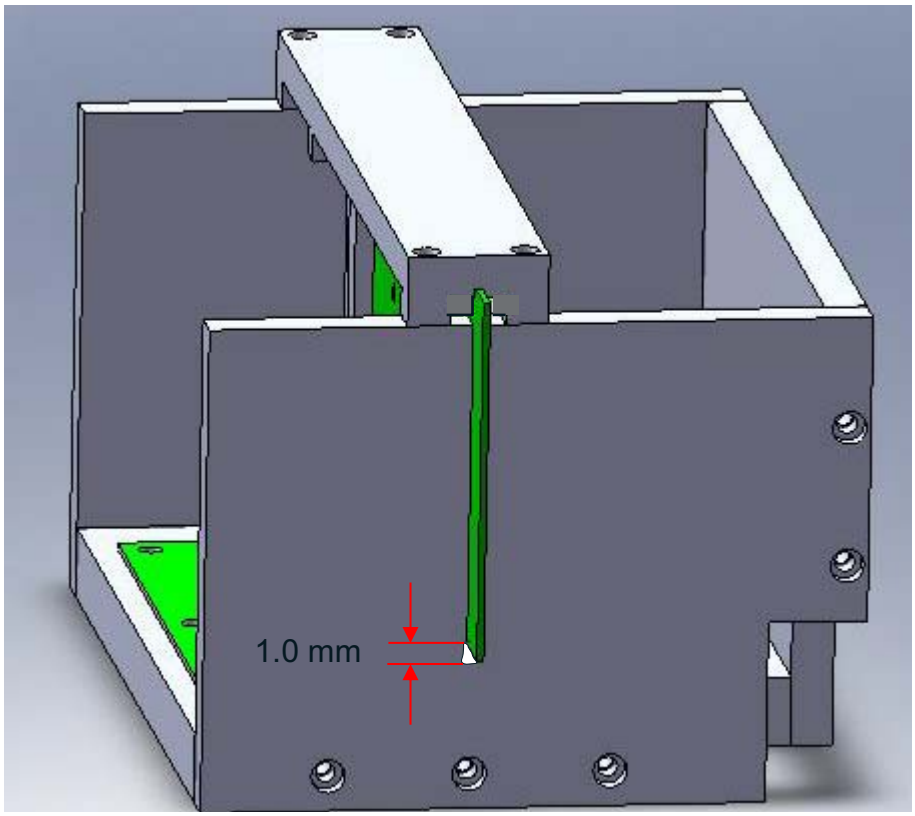
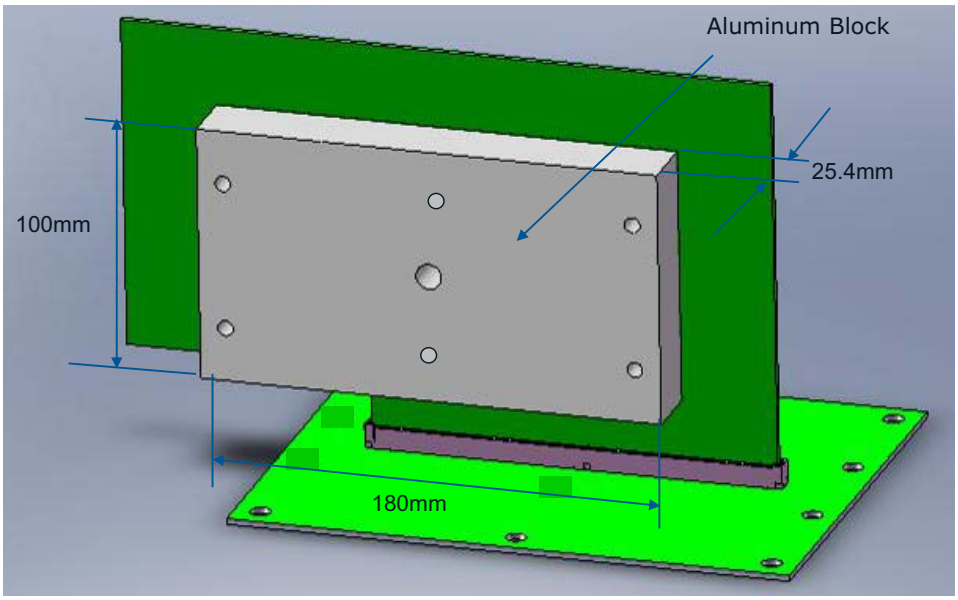



**Figure C-2. Riser Test Card Mass**



## C.5 Post Test Verification

Post shock and vibration tests inspect the riser test board and the connector for physical wear and damages. Inspection shall include but not limited to the riser card gold fingers.

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# D Assembly/Rework Guidance

## D.1 Press Tool Loading

1. **Press System Requirements**

- The press tool should have the capability to slow to 1.27 ±0.25 mm/sec while applying the appropriate force.
- The majority of qualification, testing, and characterization of the final product to be performed at the final insertion rate of 1.27 mm/sec.
- The PCIe riser card connector requires a maximum force of 1.63 kgf/pin to fully seat into the baseboard.

***Note:*** To prevent damaging the baseboard or the connector, do not exceed the maximum allowable connector pin insertion force.

- The press tool should have z-axis control capability to within 0.125 mm.
- The press tool should have a press bed flatness adequate to ensure the application tooling properly engages the connector pressing surfaces. The face of the application press should be parallel with the PCB surface to within 0.125 mm, and should have a z-axis stroke of 25 mm or greater.
- Pressing mechanism must restrict side-to-side movement during press cycle.

2. **Alignment of the PCB and Connector**

- The application tool (insertion head) can be manually placed on the mating side of the connector or attached to the press ram. The alignment of the PCB in the press is such that the press ram is approximately centered (within a diameter of 12.7 mm) above the insertion head.

3. **Press**

The application tool (insertion head) is designed to conform to the mating end geometry of the connector. Ensure the connector is properly preloaded, place the PCB into the press, and place the insertion head on the connector, as shown in Figure 6-1.

**Figure 6-1. Connector Assembly**

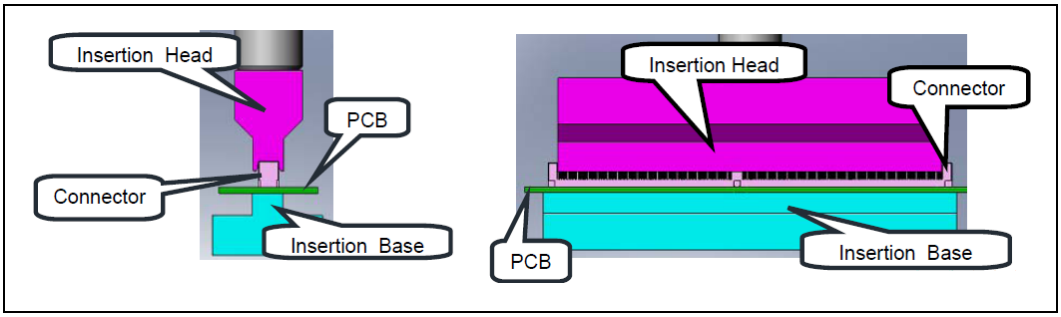


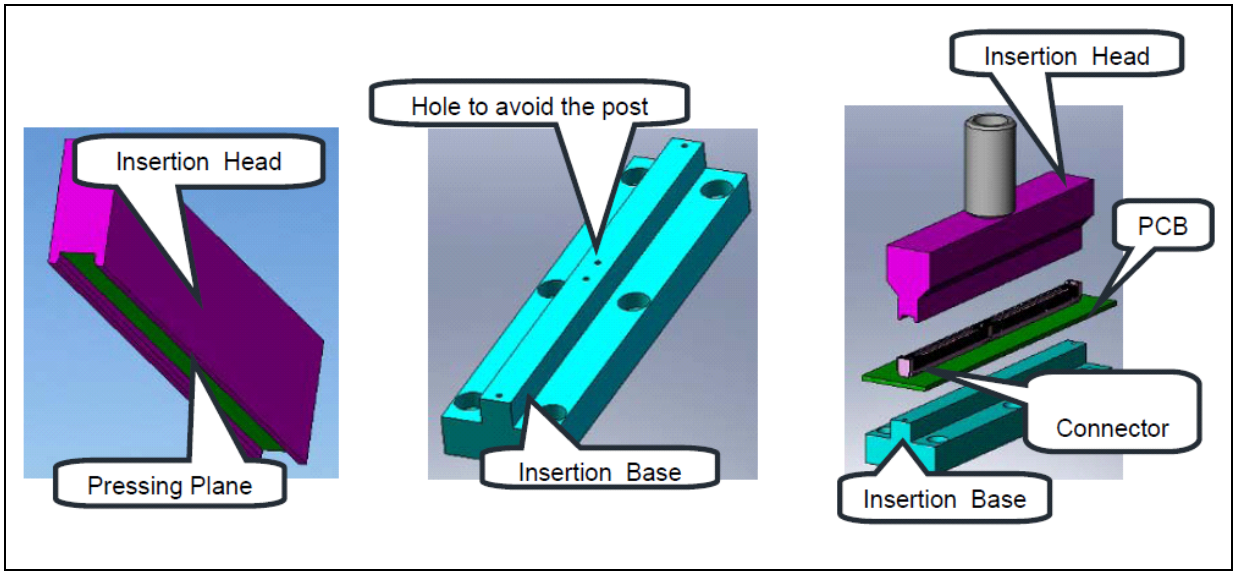
**Table D-1. Connector Pin Insertion Force**

| Press Force | Value | Notes |
|---|---|---|
| Preload force | 0.125 Kgf/pin | Force adequate to insert the connector pins into the baseboard holes.<br>This is an approximation value. |
| Preseating force | 0.25 Kgf/pin | Force adequate to ensure the connector does not become dislodged.<br>This is an approximation value. |
| Insertion force | 1.63 kgf/pin max | Force necessary to fully insert the connector pins into the baseboard holes. |

## D.2 Assembly

A press tool is required to aid in inserting PCIe riser card connector pins into the baseboard. The press tooling consists of an insertion head and an insertion base, as shown in Figure D-1. The following steps provide general instructions on using the tool to complete the connector installation onto a baseboard.

**Figure D-1. Connector Insertion Tool**




**Step 1: Inspect the connector pin tips for bends or damages**

Use an approved pin gauge to inspect the connector pin positions. This step is to ensure pin tip positional accuracy was not compromised during packaging, shipping, or handling prior to installation. An out-of-position pin could result in bent and/or folded pins and severe board damage.

**Step 2: Inspect the plated through-hole on the PCB**

Inspect all PCIe riser card connector holes in the baseboard for damage, blockage, or obstruction before performing the pressing operation. This can be done using optical or mechanical inspection tools. During any mechanical or inspection operation requiring physical contact with the baseboard, use caution to prevent damaging the inside of the PTHs.

### Step 3: Align the baseboard and the connector to the press tool

Ensure that the entire assembly is aligned and located in reference to the press and the base tool, baseboard, and the connector orientation.

### Step 4: Partially insert the connector pins into the baseboard holes

1. Under preload, insert the connector pins into the baseboard hole pattern.
2. Ensure that the connector is properly oriented or the connector will not function properly from a mechanical or electrical standpoint. See customer drawings for the position of "Pin A1" reference location.
3. Ensure that all pins are aligned with their respective PTHs and the tip of all connector to baseboard keying pins are below the top surface plane of the PCB.
4. Apply a preseating force adequate to ensure the connector does not become dislodged during any slight board movement.
5. Visually inspect each connector before actuating the press to ensure all pins have remained properly positioned inside the PTH.

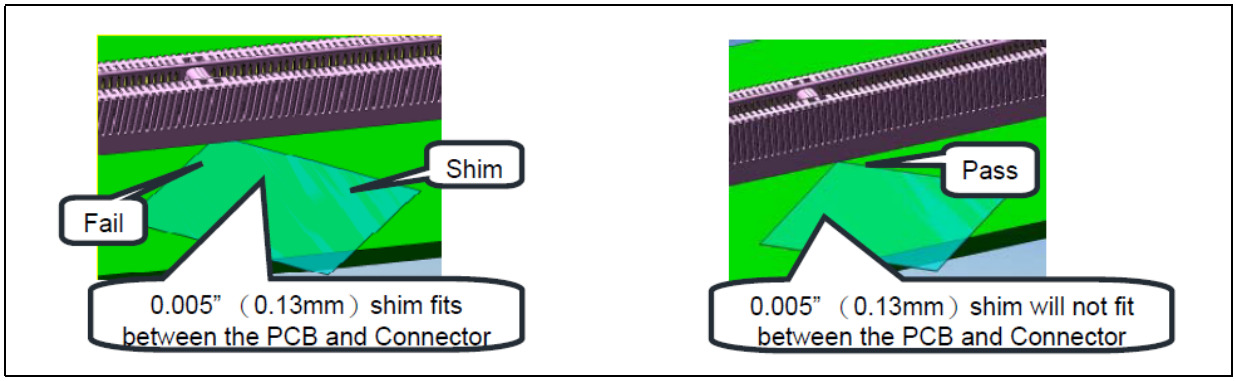
### Step 5: Press in the connector

- Lower the press head until it reaches the top surface (riser card side) of the connector. Continue lowering the press until the connector is seated flush on the PCB surface.

### Step 6: Inspection

1. **Connector Position:**
   Verify the PCIe riser card connector is seated flush on the baseboard. The gap between the connector and the baseboard must be less than 0.13 mm (0.005 in.). A gap of 0.13 mm (0.005 in.) or greater between the PCB and connector is NOT acceptable.
   Verify the final seating depth of the connector using a 0.13 mm (0.005 in.) shim. The shim should not fit between the surface of the PCB and the plastic insulator on the connector, as shown in Figure D-2.
2. **Quality:**
   Verify there are no cracks or deformities in the connector plastic. If possible, view all pins from the backside of the board. Each pin's end must be visible and pressed-in to the same height.

**Figure D-2. Quality Inspection After Assembly**



## D.3 Rework

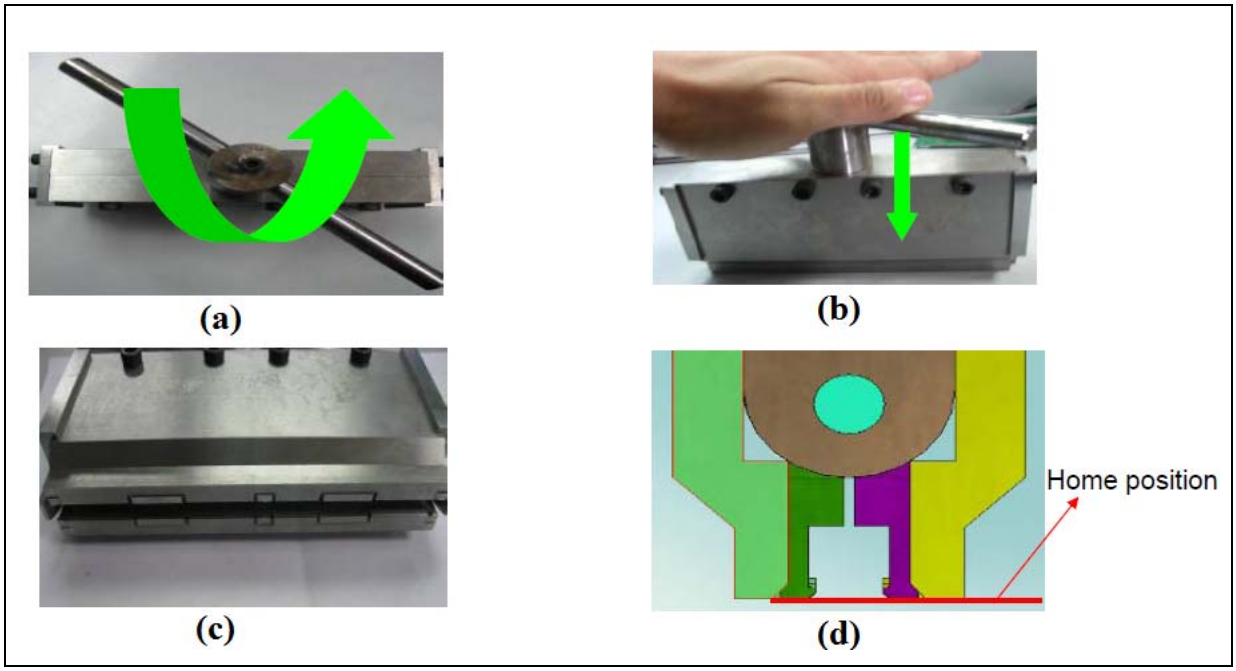
The connector rework tooling is used to remove the PCIe riser card connector from baseboard. It consists of a handle, shaft, left support, right support, screw, puller, left clamp, right clamp, front guide, and back guide.

The following steps provide general instructions on using the rework tool to complete the connector removal from the baseboard.

**Step 1: Verify the removal tool is in the home position**

Open the removal tool by turning the handle counterclockwise as shown in Figure D-3 picture (a). At the same time push the handle downwards as shown in picture (b) until the movable parts are in the home position as shown in pictures (c) and (d).

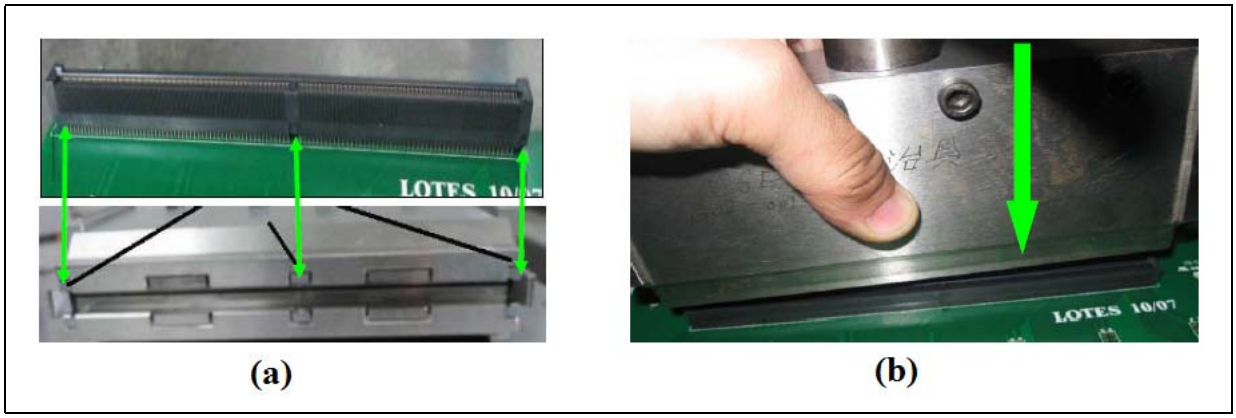
**Figure D-3. Rework Tool Home Position**




**Step 2: Place the rework tool over the connector**

1. Locate the defective connector that needs to be removed from the board.
2. Align and position the hook of the tool next to the notch of the connector as shown in Figure D-4 (a).
3. Place the removal tool flat on the surface of the board and align with the defective connector as shown in Figure D-4 (b).

### Figure D-4. Rework Tool Placement



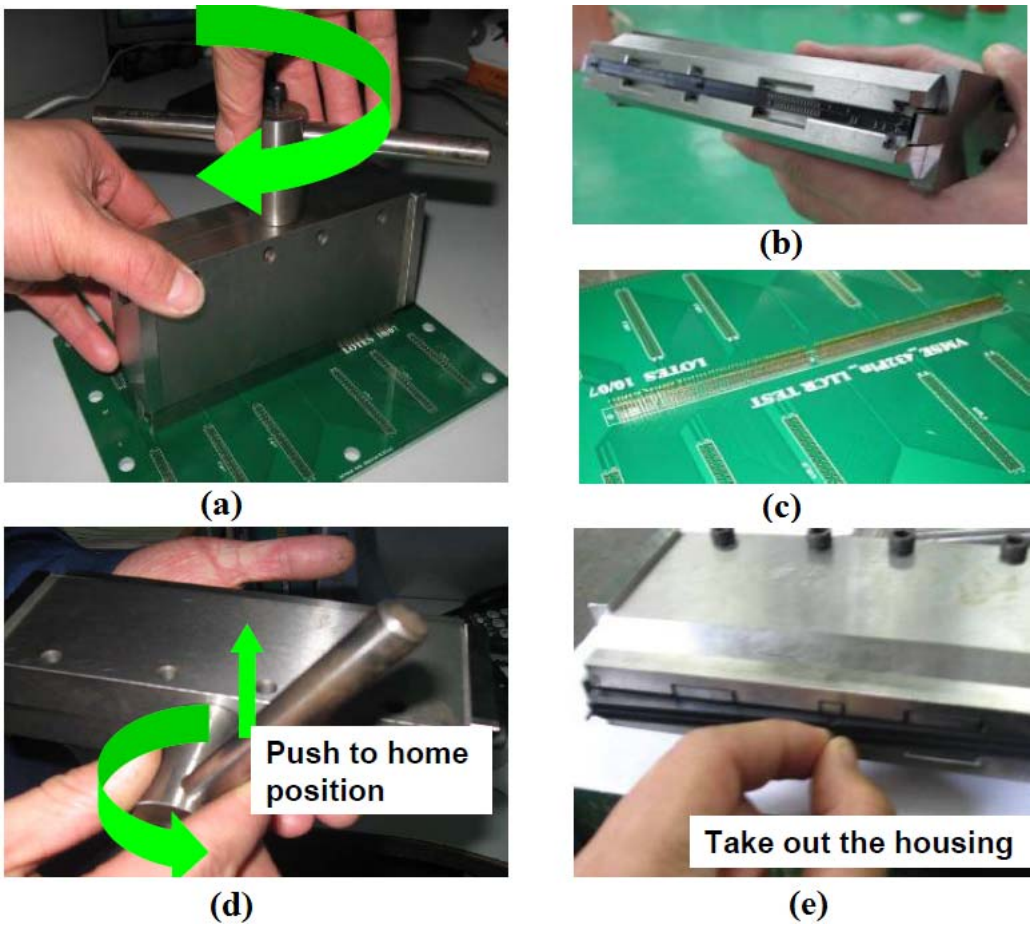

**Step 3: Remove the connector plastic housing using the removal tool.**

### Table D-2. Connector Pin Removal Force

| Press Force | Value | Notes |
|---|---|---|
| Removal force | 0.49 kgf/pin min | Force necessary to remove the connector pins from baseboard holes. |

1. Hold the removal tool down tightly against the surface of the board with one hand. Slowly turn the handle clockwise with the other hand until the handle starts to tighten and the connector housing begins to lift out of the board. See Figure D-5 picture (a).
2. Continue to turn the handle until the connector housing is completely removed from the board.
3. Lift the removal tool and the connector plastic housing away from the board.
4. Remove the connector plastic housing from the tool by turning the handle counter-clockwise, and push the movable part to return to its home position as shown in Figure D-5 (d).
5. Take out the housing as shown in Figure D-5 (e).

**Figure D-5. Removing Connector Housing**



**Step 4: Manually remove the remaining connector pins.**

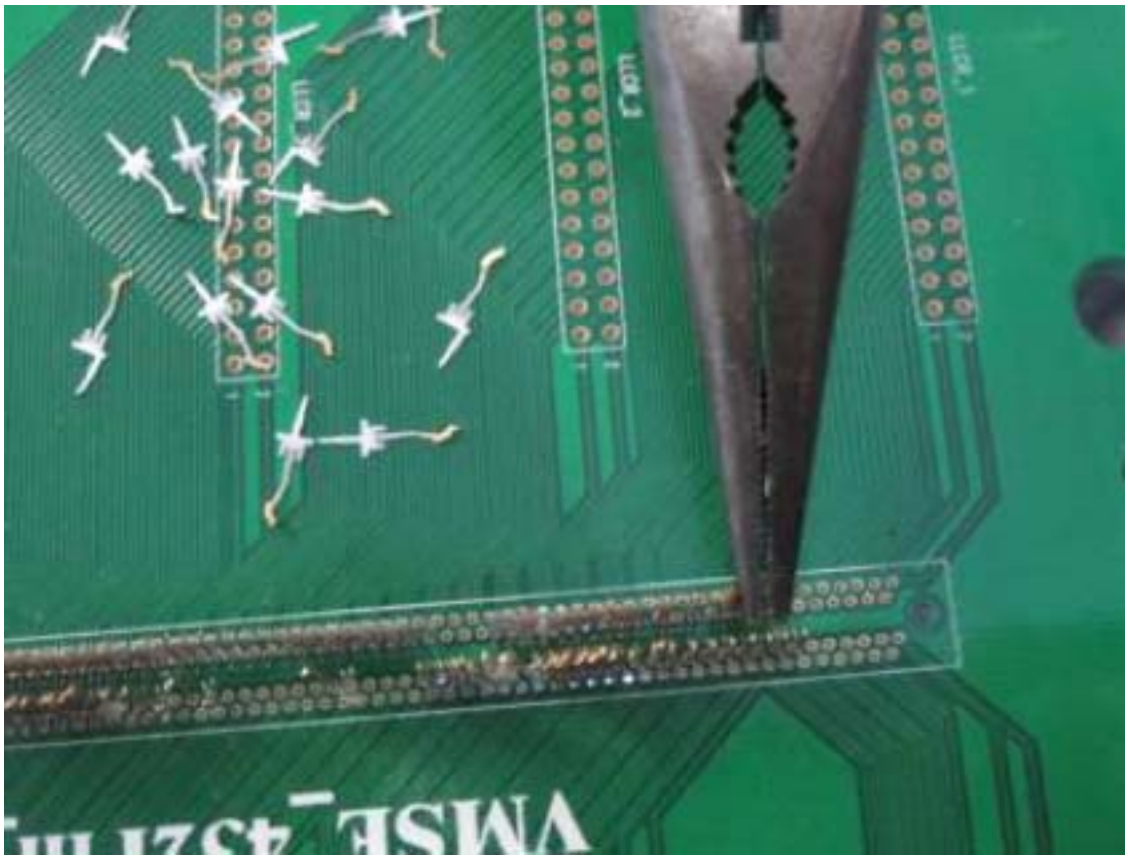
Some pins may remain in the board after the plastic housing and plastic insert are removed. These pins must be manually removed with needle-nose pliers to complete the removal process.

Use a pair of fine-tipped needle-nose pliers to extract the remaining pins one at a time.

***Caution:*** Do not attempt to remove more than one pin at a time. Removing more than one pin at a time might damage the baseboard.

Grasp the pin firmly and pull straight up as shown in Figure D-6. Check the pin and plated through-hole to ensure the pin is fully removed and the hole is clear.

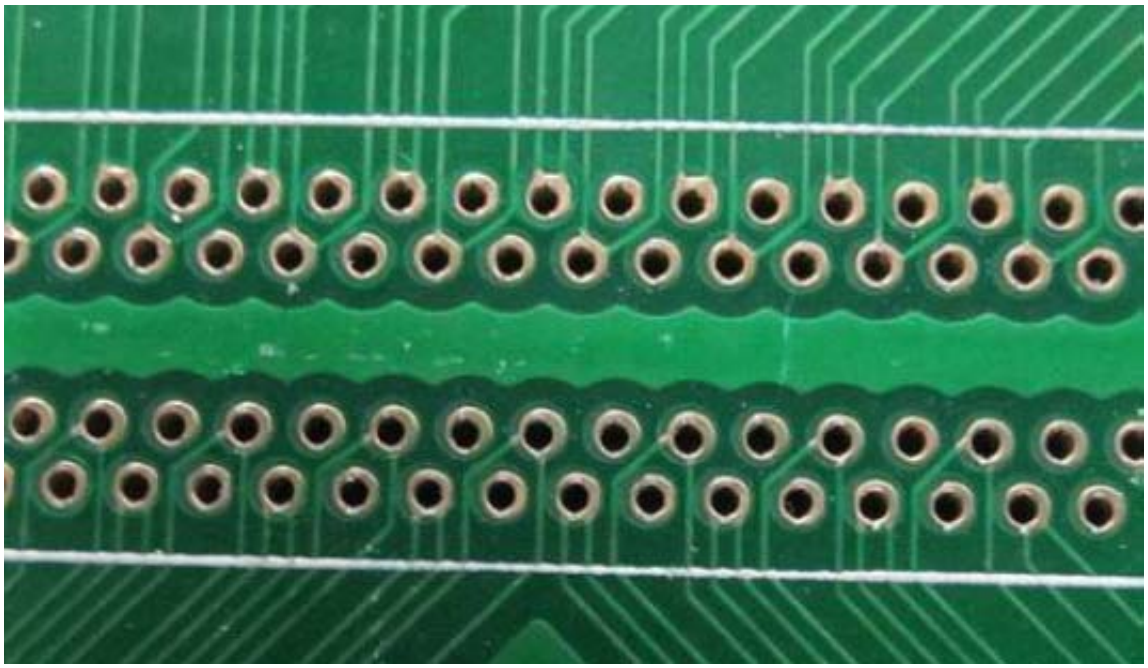
**Figure D-6. Example of Manual Pin Removal**



### Step 5: Final inspection

After removing all pins, use an optical magnifier to visually inspect the plated through-holes for damage and/or material left behind from the extraction process. See Figure D-7.

**Figure D-7. Example of Board Inspection Post Connector Removal Process**



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