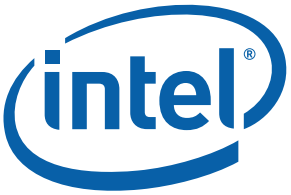

Intel® 5 Series Chipset and Intel® 3400 Series Chipset

Specification Update

May 2013

Notice: Intel® 5 Series Chipset and Intel® 3400 Series Chipset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Document Number: 322170-028

Contents

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Revision History

Revision	Description	Date
-001	• Initial Release	September 2009
-002	• Updated — Identification Information Markings — PCH Device and Revision Identification — 6-Errata: Intel® 5 Series Chipset and Intel® 3400 Series Chipset Full-Speed USB Isochronous Packet Truncation • Added — Errata: 7-Intel 5 Series Chipset and Intel 3400 Series Chipset USB Port Stall with Bulk and Control Traffic, 8-Intel 5 Series Chipset and Intel 3400 Series Chipset SATA SYNC Escape Erratum	January 7, 2010
-003	• Added — Errata: 9 - Intel® P55, PM55, 3400, and 3420 Chipsets May Not Fully Initialize Intel® Management Engine (Intel® ME), 10 - Intel 5 Series Chipset and Intel 3400 Series Chipset USB End of Frame When Retrying Packets Issue, 11 - Intel 5 Series Chipset and Intel 3400 Series Chipset USB Transaction Priority Issue, 12 - Intel H55 Express Chipset and Intel 3420 Chipset May Report Incorrect Number of USB Ports, 13 - Intel® HM55 Express Chipset May Report Incorrect Number of USB Ports	January 13, 2010
-004	• Added — Errata: 14 - Intel 5 Series Chipset and Intel 3400 Series Chipset HPET Writing Timing Issue, 15 - Intel 5 Series Chipset and Intel 3400 Series Chipset USB Full-Speed Port Staggering	February 13, 2010
-005	• Added — Errata: 16 - Intel 5 Series Chipset and Intel 3400 Series Chipset USB Device May Slow or Hang, 17- Intel 5 Series Chipset and Intel 3400 Series Chipset USB Low Speed Bulk/Control Transactions, 18- Intel 5 Series Chipset and Intel 3400 Series Chipset May Not Detect Unsolicited SATA COMINITs, 19- Intel 5 Series Chipset and Intel 3400 Series Chipset SATA Hot Unplug. — Specification Clarification: 1. GP_RST_SEL[95:0] Description Updated • Updated: — Intel® QS57 Chipset High Definition Audio Device ID Updated	March 10, 2010
-006	Added • Documentation Changes: 1. Correct Figure 8-2 S5 to S0 Timing Diagram • Updated Errata 17 Removed Bulk Transtion	April 14, 2010
-007	Added • Documentation Changes: 2. Update Table 3-1 to include SPI_CS0#. 3. Add Tj Mobile Thermal Junction Operating Temperature limits in Table 8-1. 4. Add sections 5.27.2.9 through 5.27.2.15 to section 5.27 PCH Display Interface. 5. Remove Unit Interval DMI from Table 8-14	May 12, 2010
-008	Edited • Corrected typographical error in Documentation Changes, item #4.	May 17, 2010
-009	• Added — Errata: 20- Intel 5 Series Chipset and Intel 3400 Series Chipset USB Missing ACK • Updated: — Errata: 11- Intel 5 Series Chipset and Intel 3400 Series Chipset Family USB Classic Device Removal Issue • Removed — Specification Clarification: 1; Documentation Changes: 1~5 that went into the updated datasheet 003	June 9, 2010

Revision	Description	Date
-010	• Added — Errata: 21 - Intel 5 Series Chipset and Intel 3400 Series Chipset Serial ATA Revision 3.0 (SATA 6Gb/s) Device Detection , 22 - Intel 5 Series Chipset and Intel 3400 Series Chipset PCI Express* Link Disable Bit. • Updated: — Specification Clarification: 1- Host WOL Behavior Clarification. — Documentation Changes: 1- Correct Table 5-58 PCH supported Audio formats over HDMI* and DisplayPort*.	July 14, 2010
-011	• Updated: — Documentation Changes: 2 - Correct Table 8-8 DC Output Characteristics and Notes 1; 3 - Correct 21.1.2 HSFS-Hardware Sequencing Flash Status Register (SPI Memory Mapped Configuration Registers) ; 4 - Correct 21.4.2 HSFS—Hardware Sequencing Flash Status Register (GbE LAN Memory Mapped Configuration Registers)	August 11, 2010
-012	• Added — Errata: 23 - Pixel Corruption Over Integrated LVDS* Interface of Intel 5 Series Chipset. • Updated: — Specification Clarification: 2 - DisplayPort Clarification	September 8, 2010
-013	• Updated: — Errata: 21 - Pixel Corruption Over Integrated LVDS Interface of Intel 5 Series Chipset	October 13, 2010
-014	• Added — Errata: 24- Intel 5 Series Chipset and Intel 3400 Series Chipset Family High-speed USB Device False Disconnect. — Specification Changes: 1 - SMLink0 Speed Change; 2 - VccVRM Min/Max Change — Specification Clarification: 3 - PIRQ Sharing; 4 - t205 Vcc Reference; 5 - Table 2-27 Power and Ground Signals — Documentation Changes: 5 - Correct 13.1.23 GEN1_DEC—LPC I/F Generic Decode Range 1 Register (LPC I/F—D31:F0); 6 - Correct Table 2-28 Functional Strap Definitions; 7 - Correct Table 9-4 Memory Decode Ranges from Processor Perspective; 8 - Correct 10.1.43 OIC—Other Interrupt Control Register; 9 - Miscellaneous Typographical and Omission Error Corrections; 10 - Update Table 2-8 USB Interface Signals; 11 - Update Note 2 of Table 9-1 PCI Devices and Functions; 12 - Correct 14.2.1 BMIC[P,S]—Bus Master IDE Command Register (D31:F2); 13 - Correct 15.2.1 BMIC[P,S]—Bus Master IDE Command Register (D31:F5); 14 - Update Table 4-1 PCH System Clock Inputs; 15 - Update Table 2-20 Clock Interface Signals; 16 - Display Interface Updates; 17 - Correct Table 1-4. Intel 5 Series Chipset Mobile SKUs; 18 - Correct Table 1-3. Intel 5 Series Chipset Desktop SKUs	November 10, 2010
-015	• Added — Errata: 25- USB Isoch In Transfer Error Issue; 26- USB Full-Speed / Low-Speed Device Removal Issue; 27- USB Babble Detected with SW Overscheduling; 28- USB Low-Speed/Full-Speed EOP Issue; 29- USB PLL Control FSM Not Getting Reset on Global Reset; 30- Asynchronous Retries Prioritized Over Periodic Transfers; 31- Incorrect Data for LS or FS USB Periodic IN Transaction; 32- Intel 5 Series and 3400 Series Chipset Family Delayed Periodic Traffic Timeout Issue. — Specification Clarification: 6- EHCI Function Numbers; 7- PCI Express Root Port Function Numbers; 8- t212 Measurement Clarification; 9- Wake Event Causes Update; 10- SGPIO Reference Clock Speed. — Documentation Changes: 19- Controller Link Updates; 20- Miscellaneous Typographical Error Corrections II; 21- Remove note 11 on Table 3-3; 22- Remove VccpNAND on Table 8-3 and Table 8-4; 23- Section 8.2 Updates.	December 8, 2010
-016	• Update — Errata: 14- Intel 5 Series Chipset and Intel 3400 Series Chipset HPET Writing Timing Issue; 21 - Intel 5 Series Chipset and Intel 3400 Series Chipset Serial ATA Revision 3.0 (SATA 6Gb/s) Device Detection • Added — Specification Clarification: 11- I^2C Block Read/Write Buffer — Documentation Changes: 24- TEMP_ALERT# Muxing; 25- Causes of Host and Global Resets Update; 26- GPIO18 Toggling Note; 27- Pre-fetch Based Pause Bit Definition; 28- Register Corrections; 29- Display BDF Register Additions; 30- Miscellaneous Typographical Error Corrections III	January 12, 2011
-017	• Update — Errata: 21 - Intel 5 Series Chipset and Intel 3400 Series Chipset Serial ATA 6Gb/s Device Detection	February 16, 2011

Revision	Description	Date
-018	• Added — Documentation Changes: 31- Chapter 8 Table Renumbering; 32- AC Characteristics Notes Additions and Corrections; 33- Table 8-22 Clock Timings Clean Up; 34- Miscellaneous Typographical Error Corrections IV	March 16, 2011
-019	• Added — Errata: 33- Intel 5 Series Chipset and Intel 3400 Series Chipset Not Responding to Cx Request when USB Async Advance Door Bell is Set; 34- Intel 5 Series Chipset LAN Tx/Rx Hang during heavy bi-directional traffic when Back-to-Back	April 13, 2011
-020	Added •Specification change: 2- VccVRM Min/Max change; 3- determinate and define signal update; 4- AFTERG3 bit name change •Specification Clarification: 12- Register and Bit Definition Clarification; 13- GPIO13 Voltage Tolerance; 14- Intel® HD Audio Register Accesses; 15- SLP_LAN# Pin Behavior; 16- HDA_DOCK_RST#/GPIO13 Description Clarification • Documentation Changes: 35- Absolute Maximum Ratings; 36- USB Register Corrections; 37- Revised Industry Specification; 38- Note Renumbering and Correction on Table 3-1; 39-Power Management Initialization Register updates; 40- chapter 9 Corrections; 41- HD Audio Corrections	Jun 13, 2011
-021	Updated •Documentation Changes: 16-Display Interface Updates section 5.27.4. Added •Errata: 36- Intel 5 Series Chipset and Intel 3400 Series Chipset Family USB Classic port reset or clear TT buffer request • Documentation Changes: 42- AFTERG3_EN Bit Reset Cause Corrections; 43- Clock Gating Register Correction; 44- Intel® ME Functional Description Updates; 45- Capability Overview Updates; 46- PCI Express Miscellaneous Port Configuration Register 2 Corrections; 47- DMI Link Capabilities and Control Registers Corrections; 48- Intel® RST Feature Capabilities Register Updates; 49- Display Technology Documentation Updates; 50- PxSCTL — Serial ATA Control Register (D31:F5); 51- PxSERR—Serial ATA Error Register Bit 23 Correction; 52- Miscellaneous Typographical Error Corrections	July 13, 2011
-022	Update •Specification Clarification: 13- GPIO13 Voltage Tolerance. Added •Specification Clarification: 17- Device 31 Function 6 Disable Bit; 18- LAN Disable Reset; 19- SGPIO Signal Usage; 20- RTCRST# and SRTCRST# Clarification • Documentation Changes: 53- Reset Behavior Updates; 54- Addition of LPC Capability List Pointer Register; 55- Addition of Legacy ATA Backwards Compatibility Registers; 56- DMI L1 Exit Latency Documentation Change; 57- Miscellaneous Documentation Corrections; 58-Intel® 5 Series Chipset Desktop SKUs Corrections	Aug 17, 2011
-023	Update • Errata: 36- [Intel® 5 Series Chipsets / Intel? 3400 Series Chipsets] USB Full-/low-speed Port Reset or Clear TT Buffer Request. Added • Specification Clarification: 21- LED Locate Intel Rapid Storage Technology Capability Removal • Documentation Changes: 59- SMBus/SMLink Timing Naming Corrections; 60- Auxiliary Trip Point Lock Bit Correction; 61- Top Swap Updates; 62- Miscellaneous Documentation Corrections;	Sep 14, 2011
-024	Added • Errata: 36- USB RMH Think Time Issue. • Specification Changes: 1- A20GATE and A20M# Functionality Removal; 2- SATA Clock General Configuration Register Update. • Specification Clarification: 1- GPIO Lock Clarification; 2- PME_Turn_Off TLP. Note: The old changes before this version had been moved to 322169 *Intel® 5 Series Chipset and Intel ® 3400 Series Chipset Datasheet, Rev 004*	December 12, 2011

Revision	Description	Date
-025	Update • Errata: 36- Intel® 5 Series Chipset / Intel® 3400 Series Chipset USB full-/low-speed Port Reset or Clear TT Buffer Request. • Errata: 37- USB RMH Think Time Issue. Added • Specification Clarification: 3- t200 Timing Clarification; 4- SPI Flash Regions Update. • Documentation Changes: 1- Controller Link Updates; 2- Miscellaneous Typographical Error Corrections; 3- Reset Behavior Updates; 4- CPU_PWR_FLR removal Removed • Specification Changes: 2- SATA Clock General Configuartion Register Update; Note: Specification Changes #2 does not apply to IBX.	February 15, 2012
-026	Added • Errata: 37- Intel® AMT and Intel® Standard Manageability KT/SOL Interrupt Status Cleared Prematurely; 38- Incorrect IRQ(x) Vector Returned for 8259 Interrupts With RAEOI Enabled. • Specification Change: 2- ROAEI options removal for OCW2. • Documentation Changes: 5- DC Inputs Characteristics Tables Corrections; 6- Miscellaneous Documentation Corrections I.	March 12, 2012
-027	Added • Errata: 39- Intel® 5 Series Chipset / Intel® 3400 Series Chipset USB RMH False Disconnect Issue.	June 18, 2012
-028	Added • Specification Change: 3- RAID 1 Description; 4- USB Register Correction. • Documentation Change: 7- Function Level Reset Pending Status Register Correction; 8- Miscellaneous Documentation Corrections II; 9- EHCIIR4 Removal.	May 15, 2013

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Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Document Number
Intel® 5 Series Chipset and Intel® 3400 Series Chipset Datasheet	322169

Nomenclature

Errata are design defects or errors. Errata may cause the behavior of the PCH to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present in all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

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Summary Tables of Changes

The following tables indicate the errata, specification changes, specification clarifications, or documentation changes which apply to the Product Name product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. These tables uses the following notations:

Codes Used in Summary Tables

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been previously fixed.
No Fix:	There are no plans to fix this erratum.

Row

Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Errata (Sheet 1 of 2)

Erratum Number	Stepping		Status	ERRATA
	B2	B3		
1	X	X	No Fix	Intel® 5 Series Chipset and Intel® 3400 Series Chipset High-Speed USB Test J/Test K Output Drive Level
2	X	X	No Fix	Intel 5 Series Chipset and Intel 3400 Series Chipset High-Speed USB 2.0 Vhsoh
3	X	X	No Fix	Intel 5 Series Chipset and Intel 3400 Series Chipset 1.5 Gb/s & 3.0 Gb/s SATA Signal Voltage Level
4	X	X	No Fix	Intel 5 Series Chipset and Intel 3400 Series Chipset SATA Low Power Device Detection
5	X	X	No Fix	Intel 5 Series Chipset and Intel 3400 Series Chipset Intel® HD Audio Interface Intermittently Does Not Play Sound
6	X		Fixed	Intel 5 Series Chipset and Intel 3400 Series Chipset Full-Speed USB Isochronous Packet Truncation
7	X	X	No Fix	Intel 5 Series Chipset and Intel 3400 Series Chipset USB Port Stall with Bulk and Control Traffic
8	X	X	No Fix	Intel 5 Series Chipset and Intel 3400 Series Chipset SATA SYNC Escape Erratum.
9	X		Fixed	Intel® P55, PM55, 3400, and 3420 Chipsets May Not Fully Initialize Intel® Management Engine
10	X	X	No Fix	Intel 5 Series Chipset and Intel 3400 Series Chipset USB End of Frame When Retrying Packets Issue
11	X	X	No Fix	Intel 5 Series Chipset and Intel 3400 Series Chipset Family USB Classic Device Removal Issue
12	X	X	No Fix	Intel® H55 Express Chipset and Intel 3420 Chipset May Report Incorrect Number of USB Ports
13	X	X	No Fix	Intel® HM55 Express Chipset May Report Incorrect Number of USB Ports
14	X	X	No Fix	Intel 5 Series Chipset and Intel 3400 Series Chipset HPET Writing Timing Issue
15	X	X	No Fix	Intel 5 Series Chipset and Intel 3400 Series Chipset USB Full-Speed Port Staggering
16	X	X	No Fix	Intel 5 Series Chipset and Intel 3400 Series Chipset USB Devices May Slow or Hang
17	X	X	No Fix	Intel 5 Series Chipset and Intel 3400 Series Chipset USB Low Speed Control Transactions
18	X	X	No Fix	Intel 5 Series Chipset and Intel 3400 Series Chipset May Not Detect Unsolicited SATA COMINITs
19	X	X	No Fix	Intel 5 Series Chipset and Intel 3400 Series Chipset SATA Hot Unplug
20	X	X	No Fix	Intel 5 Series Chipset and Intel 3400 Series Chipset USB Missing ACK
21	X	X	No Fix	Intel 5 Series Chipset and Intel 3400 Series Chipset Serial ATA 6Gb/s Device Detection
22	X	X	No Fix	Intel 5 Series Chipset and Intel 3400 Series Chipset PCI Express* Link Disable Bit
23	X	X	No Fix	Pixel Corruption Over Integrated LVDS* Interface of Intel 5 Series Chipset
24	X	X	No Fix	Intel 5 Series Chipset and Intel 3400 Series Chipset Family High-speed USB Device False Disconnect
25	X	X	No Fix	USB Isoch In Transfer Error Issue
26	X	X	No Fix	USB Full-Speed / Low-Speed Device Removal Issue
27	X	X	No Fix	USB Babble Detected with SW Overscheduling
28	X	X	No Fix	USB Low-Speed/Full-Speed EOP Issue
29	X	X	No Fix	USB PLL Control FSM Not Getting Reset on Global Reset
30	X	X	No Fix	Asynchronous Retries Prioritized Over Periodic Transfers
31	X	X	No Fix	Incorrect Data for LS or FS USB Periodic IN Transaction
32	X	X	No Fix	Intel 5 Series Chipset and Intel 3400 Series Chipset Family Delayed Periodic Traffic Timeout Issue

Errata (Sheet 2 of 2)

Erratum Number	Stepping		Status	ERRATA
	B2	B3		
33	X	X	No Fix	Intel 5 Series Chipset and Intel 3400 Series Chipset Not Responding to Cx Request when USB Async Advance Door Bell is Set
34	X	X	No Fix	Intel 5 Series Chipset LAN Tx/Rx Hang during heavy bi-directional traffic when Back-to-Back
35	X	X	No Fix	Intel® 5 Series Chipset / Intel® 3400 Series Chipset USB full-/low-speed Port Reset or Clear TT Buffer Request.
36	X	X	No Fix	USB RMH Think Time Issue
37	X	X	No Fix	Intel® AMT and Intel® Standard Manageability KT/SOL Interrupt Status Cleared Prematurely.
38	X	X	No Fix	Incorrect IRQ(x) Vector Returned for 8259 Interrupts With RAEOI Enabled.
39	X	X	No Fix	Intel® 5 Series Chipset / Intel® 3400 Series Chipset USB RMH False Disconnect Issue.

Specification Changes

Spec Change Number	Stepping		SPECIFICATION CHANGES
	B2	B3	
1	X	X	A20GATE and A20# Functionality Removal
2	X	X	ROAEI options removal for OCW2
3	X	X	RAID 1 Description
4	X	X	USB Register Correction

Specification Clarification

No.	Document Revision	SPECIFICATION CLARIFICATIONS
1	004	GPIO Lock Clarification
2	004	PME_Turn_Off TLP
3	004	t200 timing clarification
4	004	SPI flash Regions clarification

Documentation Changes (Sheet 1 of 2)

No.	Document Revision	DOCUMENTATION CHANGES
1	004	Controller Link Updates
2	004	Miscellaneous Typographical Error Corrections
3	004	Reset Behavior Updates
4	004	CPU_PWR_FLR removal
5	004	DC Inputs Characteristics Tables Corrections
6	004	Miscellaneous Documentation Corrections I

Documentation Changes (Sheet 2 of 2)

No.	Document Revision	DOCUMENTATION CHANGES
7	2.3	Function Level Reset Pending Status Register Correction
8	004	Miscellaneous Documentation Corrections II
9	004	EHCIIR4 Removal

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Identification Information

Markings

PCH Stepping	S-Spec	Top Marking	Notes
B2	SLGWN	82PM55	Intel® PM55 Chipset
B2	SLGWV	82P55	Intel® P55 Chipset
B2	SLGWX	3400	Intel® 3400 Chipset
B2	SLGWW	3420	Intel® 3420 Chipset
B3	SLGZQ	82QM57	Intel® QM57 Chipset
B3	SLGZR	82HM57	Intel® H57 Chipset
B3	SLGZS	82HM55	Intel® HM55 Chipset
B3	SLGZW	82Q57	Intel® Q57 Chipset
B3	SLGZL	82H57	Intel H57 Chipset
B3	SLGZX	82H55	Intel® H55 Chipset
B3	SLH25	3520	Intel 3420 Chipset
B3	SLGZY	3450	Intel® 3450 Chipset
B3	SLGZV	82QS57	Intel® QS57 Chipset
B3	SLH23	82PM55	Intel PM55 Chipset
B3	SLH24	82P55	Intel P55 Chipset

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PCH Device and Revision Identification

The Revision ID (RID) is traditionally an 8-bit register located at the offset 08h in the PCI header of every PCI device and function. The assigned value is based on the product's stepping.

Intel® 5 Series Chipset and Intel® 3400 Series Chipset Device and Revision ID Table (Sheet 1 of 2)

Device Function	Description	Dev ID[1]	B2 Rev ID	B3 Rev ID	Comments
D31:F0	LPC	3B02h	05h	06h	Intel® P55 Chipset
		3B03h	05h	06h	Intel® PM55 Chipset
		3B06h	n/a	06h	Intel® H55 Chipset
		3B07h	n/a	06h	Intel® QM57 Chipset
		3B08h	n/a	06h	Intel® H57 Chipset
		3B09h	n/a	06h	Intel® HM55 Chipset
		3B0Ah	n/a	06h	Intel® Q57 Chipset
		3B0Bh	n/a	06h	Intel® HM57 Chipset
		3B0Fh	n/a	06h	Intel® QS57 Chipset
		3B12h	05h	n/a	Intel® 3400 Chipset
		3B14h	05h	06h	Intel® 3420 Chipset
		3B16h	n/a	06h	Intel® 3450 Chipset
D31:F2	SATA	3B20h	05h	06h	Desktop: Non-AHCI and Non-RAID Mode (Ports 0, 1, 2, 3)
		3B21h	05h	06h	Desktop: Non-AHCI and Non-RAID Mode (Ports 0 and 1)
		3B22h	05h	06h	Desktop: AHCI (Ports 0-5)
		3B23h	05h	06h	Desktop: AHCI (Ports 0, 1, 4 and 5)
		3B25h	05h	06h	Desktop RAID: 0/1/5/10
		3B28h	05h	06h	Mobile: Non-AHCI and Non-RAID Mode (Ports 0, 1, 4 and 5)
		3B29h	05h	06h	Mobile: AHCI (Ports 0, 1, 4 and 5)
		3B2Ch	05h	06h	Mobile: RAID: 0/1/5/10
		3B2Eh	05h	06h	Mobile: Non-AHCI and Non-RAID Mode (Ports 0, 1, 2, 3)
		3B2Fh	05h	06h	Mobile: AHCI (Ports 0-5)

Intel® 5 Series Chipset and Intel® 3400 Series Chipset Device and Revision ID Table (Sheet 2 of 2)

Device Function	Description	Dev ID[1]	B2 Rev ID	B3 Rev ID	Comments
D31:F5	SATA	3B26h	05h	06h	Desktop: Non-AHCI and Non-RAID Mode (Ports 4 and 5)
		3B2Dh	05h	06h	Mobile: Non-AHCI and Non-RAID Mode (Ports 4 and 5)
D31:F3	SMBus	3B30h	05h	06h	
D31:F6	Thermal	3B32h	05h	06h	
D30:F0	DMI to PCI Bridge	244Eh	A5h	A6h	Desktop
D30:F0	DMI to PCI Bridge	2448h	A5h	A6h	Mobile
D29:F0	USB EHCI #1	3B34h	05h	06h	
D26:F0	USB EHCI #2	3B3Ch	05h	06h	
D27:F0	Intel® High Definition Audio	3B56h	05h	06h	
D27:F0	Intel High Definition Audio	3B57h	05h	06h	Intel® QS57 Chipset Only
D28:F0	PCI Express* Port 1	3B42h	05h	06h	
D28:F1	PCI Express Port 2	3B44h	05h	06h	
D28:F2	PCI Express Port 3	3B46h	05h	06h	
D28:F3	PCI Express Port 4	3B48h	05h	06h	
D28:F4	PCI Express Port 5	3B4Ah	05h	06h	
D28:F5	PCI Express Port 6	3B4Ch	05h	06h	
D28:F6	PCI Express Port 7	3B4Eh	05h	06h	
D28:F7	PCI Express Port 8	3B50h	05h	06h	
D25:F0	LAN[3]	3B41h	05h	06h	
D22:F0	Intel® MEI #1	3B64h	05h	06h	
D22:F1	Intel MEI #2	3B65h	05h	06h	
D22:F2	IDE-R	3B66h	05h	06h	
D22:F3	KT	3B67h	05h	06h	

NOTES:

1. The PCH contains two SATA controllers. The SATA Device ID is dependant upon which SATA mode is selected by BIOS and what RAID capabilities exist in the SKU.
2. The SATA RAID Controller Device ID may reflect a different value based on Bit 7 of D31:F2:Offset 9Ch.
3. LAN Device ID is loaded from EEPROM. If EEPROM contains either 0000h or FFFFh in the Device ID location, then 3B41h is used. Refer to the appropriate Intel® GbE Physical Layer Transceiver (PHY) Datasheet for LAN Device IDs.

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Errata

1. Intel® 5 Series Chipset and Intel® 3400 Series Chipset High-Speed USB Test J/Test K Output Drive Level

Problem: Pre-emphasis is not disabled on high-speed USB ports during Test J/Test K.

Implication: J and K DC voltage levels may exceed USB 2.0 V_{HSOH}-MAX and V_{HSOL}-MAX during Test J/Test K testing and may not meet the USB 2.0 specification.

Workaround: Clear bit 1 of the USB Initialization Registers [0-13] prior to enabling Test J/Test K mode using a memory editing tool. This bit must be set back to 1 for each port after Test J/Test K testing is complete.

Port	Offset: RCBA + Offset:
0	3500h
1	3504h
2	3508h
3	350Ch
4	3510h
5	3514h
6	3518h
7	351Ch
8	3520h
9	3524h
10	3528h
11	352Ch
12	3530h
13	3534h

Status: No Fix. For steppings affected, see the Summary Table of Changes.

2. Intel® 5 Series Chipset and Intel® 3400 Series Chipset High-Speed USB 2.0 V_{hsoh}

Problem: High-Speed USB 2.0 V_{hsoh} may not meet the USB 2.0 Specification.

- The maximum expected V_{hsoh} is 495 mV.

Implication: Some motherboards may exceed specification limits during USB-IF compliance testing.

Workaround: None.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

3. Intel® 5 Series Chipset and Intel® 3400 Series Chipset 1.5 Gb/s & 3.0 Gb/s SATA Signal Voltage Level

Problem: The Intel® 5 Series Chipset and Intel® 3400 Series Chipset 1.5 Gb/s & 3.0 Gb/s SATA transmit buffers have been designed to maximize performance and robustness over a variety of routing scenarios. As a result, the Intel 5 Series Chipset and Intel 3400 Series Chipset SATA 1.5 Gb/s & 3.0 Gb/s (Gen1i, Gen1m, Gen2i, and Gen2m) transmit signaling voltage levels may exceed the maximum motherboard TX connector and device RX connector voltage specifications (section 7.2.1 of the Serial ATA Specification, rev 2.5).

Implication: None Known.

Workaround: None.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

4. Intel® 5 Series Chipset and Intel® 3400 Series Chipset SATA Low Power Device Detection

Problem: Intel 5 Series Chipset and Intel 3400 Series Chipset SATA Low Power Device Detection (SLPD) may not recognize, or may falsely detect, a SATA hot-plug event during a Partial or Slumber Link Power Management (LPM) state.

Implication: On Systems which enable LPM, when a SATA device attached to the Intel 5 Series Chipset and Intel 3400 Series Chipset is configured as External or hot-plug capable, one of the following symptoms may occur:

- Symptom #1: A hot-plug or External SATA device removal which is not detected results in the OS and Intel® Matrix Storage Manager/Intel® Rapid Storage Technology console falsely reporting the device present, or incorrectly identifying an eSATA device.
- Symptom#2:A false hot-plug removal detection may occur resulting in OS boot hang or ODD media playback hang

Workaround: A driver workaround is available.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

5. Intel® 5 Series Chipset and Intel® 3400 Series Chipset Intel® HD Audio Interface Intermittently Does Not Play Sound

Problem: The Intel 5 Series Chipset and Intel 3400 Series Chipset Intel® HD Audio Controller logic may not be gated by DMI L1 entry.

Implication: Systems may intermittently not play sound on the Intel HD Audio interface Following a DMI L1 exit.

Workaround: BIOS workaround available.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

6. Intel® 5 Series Chipset and Intel® 3400 Series Chipset Full-Speed USB Isochronous Packet Truncation

Problem: Full-Speed isochronous-out transactions with multi-frame packets may be truncated, in the presence of Full or Low-Speed USB asynchronous transactions.

- For this to occur, two devices, one performing Full-Speed isochronous-out transactions and one performing asynchronous transactions must be connected to the same USB controller (Ports 0-7 and 8-13).

Implication: In the case of a USB audio device this issue may result in no audible impact or audible artifacts such as pops and clicks.
Note:

- High-Speed and Low-Speed USB devices are not impacted by this issue.
- Only devices supporting Full-Speed isochronous-out transactions that Intel is aware of are audio devices, such as sound adapters, speakers, and headphones.
- Intel has only observed the issue when a Full-Speed audio devices and Full-Speed USB web camera are connected to the same USB controller.

Workaround: None.

Status: Fixed For steppings affected, see the Summary Table of Changes.

7. Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Port Stall with Bulk and Control Traffic

Problem: When a single USB bulk device is active on an EHCI controller, and the device has pending control and bulk traffic the PCH may not be able to resolve which traffic type is a priority and the associated with the device may stall.

- The processor must be in C0 for an extended period of time such as when Cx states are disabled, or if system traffic prevents the system from leaving C0.

Implication: The USB device may appear unresponsive. If Cx states are enabled the device may recover a short time later.

Note: Intel has only observed this failure on a limited number of devices. Failure only occurs if software associated with a USB device programs the Nak Count Reload bits defined in the EHCI Specification for USB Rev 1.0 to 0.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

8. Intel® 5 Series Chipset and Intel® 3400 Series Chipset SATA SYNC Escape Erratum

Problem: When SYNC Escape by a SATA device occurs on a D2H FIS, the PCH does not set the PxIS.IFS bit to '1.' This deviates from section 6.1.9 of the Rev 1.3 Serial ATA Advanced Host Controller Interface (AHCI).

Implication: There is no known observable impact. Instead of detecting the IFS bit, software will detect a timeout error caused by the SYNC escape and then respond.

Workaround: None.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

9. Intel® P55, PM55, 3400, and 3420 Chipsets May Not Fully Initialize Intel® ME

Problem: Some Intel® P55, PM55, 3400, and 3420 based systems with Intel® ME Ignition 6.0.0.1126 PV firmware may fail to correctly initialize the Intel ME subsystem during boot at colder temperatures.

Implication: Failures may occur during BIOS update. Systems fans may run continuously at full speed and the system may have increased power consumption.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: Fixed. For steppings affected, see the Summary Table of Changes.

10. Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB End of Frame When Retrying Packets Issue

Problem: If the PCH encounters a Full-Speed or Low-Speed USB transaction with errors, the PCH may retry the transaction without considering if the transaction can finish before the end of the current frame.

Implication: The implication is dependant on the USB device. The PCH will attempt to recover per error handling specified in Section 4.5.2 of the USB Specification 2.0. The device may hang and require cycle to resume normal functionality.

Note: Intel has only observed this behavior on a limited number of USB devices. The implication only occurs if a USB device does not correctly respond to error handling as specified Section 4.5.2 of the USB Specification 2.0.

Workaround: None.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

11. Intel® 5 Series Chipset and Intel® 3400 Series Chipset Family USB Classic Device Removal Issue

Problem: If two or more USB Full-Speed / Low-Speed devices are connected to the same USB controller, the devices are not suspended, and one device is removed, one or more of the devices remaining in the system may be affected by the disconnect.

Implication: The implication is device dependant. A device may experience a delayed transaction, stall and be recovered via software, or stall and require a reset such as a hot plug to resume normal functionality.

Workaround: None.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

12. Intel® H55 Express Chipset and Intel® 3420 Chipset May Report Incorrect Number of USB Ports

Problem: The Intel® H55 Express Chipset and Intel 3420 Chipset support 6 ports on RMH #1 and may incorrectly report 8 USB ports in the bNbrPorts field of the RMH hub descriptor.

Implication: If AC power is removed while the system is in hibernate, when the system resumes, new USB devices may not be detected, and all devices on RMH #1 may not function.

Note: AC power removal while a system is in S4 is not a common occurrence.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

13. Intel® HM55 Express Chipset May Report Incorrect Number of USB Ports

Problem: The Intel® HM55 Express Chipset supports 6 ports on RMH #1 and will incorrectly report 8 USB ports in the bNbrPorts field of the RMH hub descriptor.

Implication: There are no known functional implications due to this issue on production Intel HM55 chipsets.

Workaround: None.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

14. Intel® 5 Series Chipset and Intel® 3400 Series Chipset HPET Writing Timing Issue

Problem: A read transaction that immediately follows a write transaction to the HPET register space may return an incorrect value.

Implication: Implication is dependent on the usage model as noted below:

- For the HPET TIMn_COMP Timer 0 Comparator Value Register and HPET MAIN_CNT—Main Counter Value Register the issue could result in the software receiving stale data. This may result in undetermined system behavior.

Note: Timers [1:7] are not affected by this issue.

- For TIMERn_VAL_SET_CNF bit 6 in the TIMn_CONF—Timer n Configuration there is no known usage model for reading this bit and there are no known functional implications.
- A write to the High Precision Timer Configuration (HPTC) register followed by a read to HPET register space may return all 0xFFFF_FFFFh.

Workaround: A workaround is available.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

15. Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Full-Speed Port Staggering

Problem: When USB full-speed/low-speed port staggering is enabled, the PCH may not wait for the bus to return to an idle state after an End of Packet (EOP) and may incorrectly acknowledge bus noise as a data packet.

Implication: Some full-speed/low-speed devices may fail to enumerate and function.

Note: This issue has been seen with a minimum number of devices on some motherboard ports with certain cable and trace lengths.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

16. Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Devices May Slow or Hang

Problem: When the processor is in C0, and a single bulk High-Speed USB device is active the port associated with the active device may hang.

Implication: The implication is device driver dependant. Intel has observed some USB devices may have decreased performance, or the device may hang.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

17. Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Low Speed Control Transactions

Problem: If the USB control buffers in the PCH Rate Matching Hub(s) are saturated with pending transactions the buffers may not be serviced in round robin order.

Implication: Some low-speed endpoints may not receive their pending control transactions.

Note: This issue has only been observed in synthetic test environment. The implication will be Device, driver and operating system specific.

Workaround: None.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

18. Intel® 5 Series Chipset and Intel® 3400 Series Chipset May Not Detect Unsolicited SATA COMINITs

Problem: Intel 5 Series Chipset and Intel 3400 Series Chipset may not detect an unsolicited COMINIT from a SATA device

Implication: The SATA device may not be properly detected and configured resulting in the device Not functioning as expected.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

19. Intel® 5 Series Chipset and Intel® 3400 Series Chipset SATA Hot Unplug

Problem: Intel 5 Series Chipset and Intel 3400 Series Chipset may not detect the unplug of a SATA 3.0 Gb/s device on a hot-plug enabled SATA port.

Implication: Unplugged SATA device may temporarily appear to be available.

Workaround: A BIOS code change has been identified and may be implemented as a workaround for this erratum.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

20. Intel® 5 Series Chipset and Intel® 3400 Series Chipset USB Missing ACK

Problem: Following system power cycling or S3-S5 resume, if both HS and LS/FS devices are attached to the same controller, the host controller may not respond to a HS device ACK during a Get Descriptor request from the host SW to a USB HS port.

Implication: USB high-speed devices may not be detected after a power cycling or S3-S5 resume.

- Intel has only observed this failure on a limited number of platforms. On a failing platform, the issue occurs infrequently.
- Full-speed and low-speed USB devices are not impacted by this issue.

Workaround: None.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

21. Intel® 5 Series Chipset and Intel® 3400 Series Chipset Serial ATA 6Gb/s Device Detection

Problem: Intel 5 Series Chipset and Intel 3400 Series Chipset may not be able to complete SATA Out Of Band (OOB) signaling with SATA 6Gb/s devices and down-shift to SATA 3Gb/s speed.

Implication: Intel 5 Series Chipset and Intel 3400 Series Chipset may not detect a SATA 6Gb/s device upon power up or resume form S3, S4 or S5 State, resulting in indeterminate system behavior.

Workaround: None.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

22. Intel® 5 Series Chipset and Intel® 3400 Series Chipset PCI Express* Link Disable Bit

Problem: Intel 5 Series Chipset and Intel 3400 Series Chipset PCI Express* Ports may not exit the disable state when the Link Control Register "Link Disable" bit is set and PCIe Device Electrical Idle Exit is detected.

Implication: Port Specific Software Directed Hot Plug or Power Management support using the "Link Disable" bit may cause an Intel 5 Series Chipset and Intel 3400 Series Chipset PCI Express Port to be stuck in the "Link Disable state" until a Host Reset with Power Cycling occurs.

Workaround: For Intel 5 Series Chipset and Intel 3400 Series Chipset PCI Express Port Specific Software Directed Hot Plug or Power Management support, use PCI Power Management Control register D3HOT bits instead of Link Disable bit.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

23. Pixel Corruption Over Integrated LVDS* Interface of Intel® 5 Series Chipset

Problem: Pixel corruption may be observed over integrated LVDS* interface on Mobile Intel 5 Series Platforms.

Implication: Display artifacts may be seen upon mode sets (resolution changes, screen rotation) and/or system boot on the platforms that use integrated LVDS.

Note: Visual artifacts observed in LVDS dual channel mode with panels supporting maximum native resolution of 1920 x1080 and higher.

Workaround: VBIOS and Intel Graphics Media Accelerator driver change has been identified and may be implemented as a workaround for this erratum.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

24. Intel® 5 Series Chipset and Intel® 3400 Series Chipset Family High-speed USB Device False Disconnect

Problem: Intel 5 Series Chipset and Intel 3400 Series Chipset may falsely detect a USB high-speed (HS) device has been disconnected.

False detection is dependent upon:

— HS USB devices with termination impedance at the high-end or greater than USB2.0 specification.

— And USB ports routed with high motherboard trace impedance.

Implication: HS USB device will appear to be disconnected and no longer accessible until a device reset, such as a hot plug, to resume normal functionality.

Note: This issue has only been observed on a limited number of HS USB devices. This issue does not affect full-speed or low-speed USB devices

Workaround: None.

Status: No Fix. For steppings affected, see the Summary Table of Changes.

25. USB Isoch In Transfer Error Issue

Problem: If a USB Full-Speed inbound isochronous transaction with a packet length 190 bytes or greater is started near the end of a micro-frame the PCH may see more than 189 bytes in the next micro-frame.

Implication: If the PCH sees more than 189 bytes for a micro-frame an error will be sent to software and the isochronous transfer will be lost. If a single data packet is lost no perceptible impact for the end user is expected.

Note: Intel has only observed the issue in a synthetic test environment where precise control of packet scheduling is available, and has not observed this failure in its compatibility validation testing.

- Isochronous traffic is periodic and cannot be retried thus it is considered good practice for software to schedule isochronous transactions to start at the beginning of a micro-frame. Known software solutions follow this practice.
- To sensitize the system to the issue additional traffic such as other isochronous transactions or retries of asynchronous transactions would be required to push the inbound isochronous transaction to the end of the micro-frame.

Workaround: None.

Status: No Plan to Fix.

26. USB Full-Speed / Low-Speed Device Removal Issue

Problem: If two or more USB Full-Speed / Low-Speed devices are connected to the same USB controller, the devices are not suspended, and one device is removed, one or more of the devices remaining in the system may be affected by the disconnect.

Implication: The implication is device dependent. A device may experience a delayed transaction, stall and be recovered via software, or stall and require a reset such as a hot plug to resume normal functionality.

Workaround: None.

Status: No Plan to Fix.

27. USB Babble Detected with SW Overscheduling

Problem: If software violates USB periodic scheduling rules for Full-Speed isochronous traffic by overscheduling, the RMH may not handle the error condition properly and return a completion split with more data than the length expected.

Implication: If the RMH returns more data than expected, the endpoint will detect packet babble for that transaction and the packet will be dropped. Since overscheduling occurred to create the error condition, the packet would be dropped regardless of RMH behavior. If a single isochronous data packet is lost, no perceptible impact to the end user is expected.

Note: USB software overscheduling occurs when the amount of data scheduled for a microframe exceeds the maximum budget. This is an error condition that violates the USB periodic scheduling rule.

Note: This failure has only been recreated synthetically with USB software intentionally overscheduling traffic to hit the error condition.

Workaround: None.

Status: No Plan to Fix.

28. USB Low-Speed/Full-Speed EOP Issue

Problem: If the EOP of the last packet in a USB Isochronous split transaction (Transaction >189 bytes) is dropped or delayed 3 ms or longer the following may occur:

- If there are no other pending Low-Speed or Full-speed transactions the RMH will not send SOF, or Keep-Alive. Devices connected to the RMH will interpret this condition as idle and will enter suspend.
- If there is other pending Low-Speed or Full-Speed transactions, the RMH will drop the isochronous transaction and resume normal operation.

Implication:

- If there are no other transactions pending, the RMH is unaware a device is entered suspend and may start sending a transaction without waking the device. The implication is device dependent, but a device may stall and require a reset to resume functionality.
- If there are other transactions present, only the initial isochronous transaction may be lost. The loss of a single isochronous transaction may not result in end user perceptible impact.

Note: Intel has only observed this failure when using software that does not comply with the USB specification and violates the hardware isochronous scheduling threshold by terminating transactions that are already in progress.

Workaround: None.

Status: No Plan to Fix.

29. USB PLL Control FSM not Getting Reset on Global Reset

Problem: Intel 5 Series Chipset and Intel 3400 Series Chipset USB PLL may not lock if a Global Reset occurs early during a cold boot sequence.

Implication: USB interface would not be functional an additional cold boot would be necessary to recover.

Workaround: None.

Status: No Plan to Fix.

30. Asynchronous Retries Prioritized Over Periodic Transfers

Problem: The integrated USB RMH incorrectly prioritizes Full-Speed and Low-Speed asynchronous retries over dispatchable periodic transfers.

Implication: Periodic transfers may be delayed or aborted. If the asynchronous retry latency causes the periodic transfer to be aborted, the impact varies depending on the nature of periodic transfer:

- If a periodic interrupt transfer is aborted, the data may be recovered by the next instance of the interrupt or the data could be dropped.
- If a periodic isochronous transfer is aborted, the data will be dropped. A single dropped periodic transaction should not be noticeable by end user.

Note: This issue has only been seen in a synthetic environment. The USB spec does not consider the occasional loss of periodic traffic a violation.

Workaround: None.

Status: No Plan to Fix.

31. Incorrect Data for LS or FS USB Periodic IN Transaction

Problem: The Periodic Frame list entry in DRAM for a USB LS or FS Periodic IN transaction may incorrectly get some of its data from a prior Periodic IN transaction which was initiated very late into the preceding Micro-frame.

It is considered good practice for software to schedule Periodic Transactions at the start of a Micro-frame. However Periodic transactions may occur late into a Micro-frame due to the following cases outlined below:

- Asynchronous transaction starting near the end of the proceeding Micro-frame gets Asynchronously retried.

Note: Transactions getting Asynchronous retried would only occur for ill behaved USB device or USB port with a signal integrity issue.

- Or Two Periodic transactions are scheduled by software to occur in the same Micro-frame and the first needs to push the second Periodic IN transaction to the end of the Micro-frame boundary

Implication: The implication will be device, driver or operating system specific.

Note: This issue has only been observed in a synthetic test environment.

Workaround: None.

Status: No Plan to Fix.

32. Intel® 5 Series Chipset and Intel® 3400 Series Chipset Family Delayed Periodic Traffic Timeout Issue

Problem: If an interrupt transaction is pushed to the x+4 micro-frame boundary due to asynchronous retries, the RMH may not wait for the interrupt transaction to timeout before starting the next transaction.

IF RMH TT reaches a discard boundary, a timeout may be ignored.

Implication: If the next transaction is intended for the same device targeted by the interrupt, the successful completion of that transaction is device dependent and cannot be guaranteed. The implication may differ depending on the nature of transaction: (only impacts TT – FS / LS).

- If the transaction is asynchronous and the device does not respond, it will eventually be retried with no impact.
- If the transaction is periodic and the device does not respond, the transfer may be dropped. A single dropped periodic transaction should not be noticeable by end user.
- NOTE: This issue has only been seen in a synthetic environment.

Workaround: None.

Status: No Plan to Fix.

33. Intel® 5 Series Chipset and Intel® 3400 Series Chipset Not Responding to Cx Request when USB Async Advance Door Bell is Set

Problem: The Intel 5 Series Chipset and Intel 3400 Series Chipset may prevent the Processor from returning to C0 if the USB Async Advance Doorbell gets set just prior to the Processor transition into Cx and EHCI Host controller is not able to completely process the USB Async Advance Doorbell event prior to a Cx wake event occurring.

Note: The susceptibility window for this issue to occur is very low, as the alignment of Async Advance doorbell event completion and Cx to C0 State transition event need to intersect within a 64ns or less window.

Implication: System may hang.

Note: Intel has only observed this failure with a single proprietary device's GUI application.

Workaround: A workaround is available. Contact your local Intel representative for workaround information.

Status: No Plan to Fix.

34. Intel® 5 Series Chipset LAN Tx/Rx Hang During Heavy Bi-Directional Traffic when Back-to-Back

Problem: When two systems with Intel® 82577 or 82578 Gigabit Network Connection and Intel 5 Series Chipset are connected back-to-back, a network hang might occur during simultaneous Transmit and Receive file transfers of heavy network traffic. A connection with any other link partner is not impacted.

Implication: The Intel 82577 or 82578 Gigabit Network Connection does not respond to a ping and no traffic can be transferred between the link partner even though the link is maintained and LEDs are on.

Workaround: A workaround exists starting in the 11.8.72.0 version of the e1k Windows* driver and starting in 1.0.2.5 of the e1000e Linux driver.

Status: No Plan to Fix.

35. Intel® 5 Series Chipset / Intel® 3400 Series Chipset USB full-/low-speed Port Reset or Clear TT Buffer Request

Problem: One or more Full-Speed / Low-Speed USB devices on the same RMH controller may be affected if the devices are not suspended and either (a) software issues a Port Reset OR (b) software issues a Clear TT Buffer request to a port executing a split Full-Speed / Low-Speed ASYNC Out command.

- The Small window of exposure for Full-Speed device is around 1.5 micro-seconds and around 12 micro-seconds for a Low-Speed device.

Implication: The affected port may stall or receive stale data for a newly arrived split transfer occurring at the time of the port Reset or Clear TT Buffer request.

Note: This issue has only been observed in a synthetic test environment.

Workaround: None.

Status: No Plan to Fix.

36. USB RMH Think Time Issue

Problem: The Intel 5 Series Chipset and Intel 3400 Series Chipset USB RMH Think Time may exceed its declared value in the RMH hub descriptor register of 8 full-speed bit times.

Implication: If the OS USB driver fully subscribes a USB microframe, LS/FS transactions may exceed the microframe boundary.

Note: No functional failures have been observed.

Workaround: None.

Status: No Plan to Fix.

37. Intel® AMT and Intel® Standard Manageability KT/SOL Interrupt Status Cleared Prematurely

Problem: A read of the Intel® AMT and Intel® Standard Manageability enabled SOL KTIIR (KT Interrupt Identification Register) or KTLSR (KT Line Status Register) that occurs simultaneous to the arrival of an SOL Host interrupt event may result in a read of the Interrupt Status (INTSTS) bit 0 returning the status of "No Pending interrupt to Host" despite KTLSR reporting a serviceable event.

Implication: Implication of a missed SOL Host interrupt is software implementation dependent. Subsequent interrupts not aligned to a KTIIR or KTLSR read will clear "0" bit 0 (INTSTS) to indicate a pending interrupt to the Host.

Workaround: Software should not rely on reading only bit 0 (INTSTS) of the KTIIR register and should also poll the KTLSR to determine if a SOL Host interrupt is pending.

Status: No Plan to Fix.

38. Incorrect IRQ(x) Vector Returned for 8259 Interrupts With RAEOI Enabled

Problem: If multiple interrupts are active prior to an interrupt acknowledge cycle with Rotating Automatic End of Interrupt (RAEOI) mode of operation enabled for 8259 interrupts (0-7), an invorrect IRQ(x) vector may be returned to the CPU..

Implication: Implications of an incorrect IRQ(x) vector being returned to the CPU are SW implementation dependent.

Note: This issue has only been observed in a synthetic test environment.

Workaround: None.

Status: No Plan to Fix.

39. Intel® 5 Series Chipset / Intel® 3400 Series Chipset USB RMH false disconnect Issue

Problem: The PCH may falsely detect a USB High-Speed (HS) device disconnect if all of the following conditions are met:

1. The HS Device is connected through the Rate Matching Hub (RMH) of the PCH's EHCI controller either directly or through a high-speed hub or series of high-speed hubs.

2. The device is resuming from selective suspend or port reset.

3. The resume occurs within a narrow time window during the EOP (End of Packet) portion of the SOF (Start of Frame) Packet on the USB bus.

Implication: Following the false disconnect, the HS device will be automatically re-enumerated. The system implication will depend on the resume event cause:

- If the resume event is a port reset, a second port reset will be automatically generated and the device re-enumerated. No end user impact is expected.
- If the resume event is a hardware or software initiated resume from selective suspend, the implication will be device and software specific, which may result in anomalous system behavior.

Note: If the HS device is a hub, then all of the devices behind the hub, independent of the device speed, may also be re-enumerated.

Workaround: None.

Status: No Plan to Fix.

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Specification Changes

1. A20GATE and A20M# Functionality Removal

A20M# functionality is not supported on processors on Intel 5 Series/3400 Series Chipset Family-based platforms.

a. Table 2-10 is updated as shown:

Name	Type	Description
A20GATE	I	A20 Gate: Functionality reserved. A20M# functionality is not supported.

b. Table 3-4 is updated as shown:

Signal Name	Power Well	Driver During Reset	S0/S1	S3	S4/S5
Processor Interface					
A20GATE	Core	Pull-up	Static	Off	Off

c. Table 3-5 is updated as shown:

Signal Name	Power Well	Driver During Reset	C-x states	S0/S1	S3	S4/S5
Processor Interface						
A20GATE	Core	Pull-up	Static	Static	Off	Off

d. A20M# is removed as a VLW message from section 5.12.

e. Section 5.12.1.1 is removed.

f. A20GATE/A20M# removed from section 5.12.2.1.

g. A20M# removed from section 5.12.3.

h. 13.1.27 ULKMC — USB Legacy Keyboard / Mouse Control Register bit 5 is modified as shown:

Bit	Description
5	**A20Gate Pass-Through Enable (A20PASSEN)** — R/W. 0 = Disable. 1 = Enable. Allows A20GATE sequence Pass-Through function. A specific cycle sequence involving writes to port 60h and 64h does not result in the setting of the SMI status bits. **NOTE:** A20M# functionality is not supported.

i. Section 13.7.3 name changed from PORT92—Fast A20 and Init Register to PORT92—Init Register and bit 1 is modified as shown:

Bit	Description
1	Alternate A20 Gate (ALT_A20_GATE) — R/W. Functionality reserved. A20M# functionality is not supported.

2. ROAEI options removal for OCW2

Remove bit setting "000" and "100" for Operational Control Word 2 Register bits [7:5] in section 13.4.8.

13.4.8 OCW2—Operational Control Word 2 Register

Offset Address: Master Controller – 020h Attribute:WO
Slave Controller – 0A0h Size: 8 bits
Default Value: Bit[4:0]=undefined, Bit[7:5]=001

Following a part reset or ICW initialization, the controller enters the fully nested mode of operation. Non-specific EOI without rotation is the default. Both rotation mode and specific EOI mode are disabled following initialization.

Bit	Description
7:5	**Rotate and EOI Codes** (R, SL, EOI)—WO. These three bits control the Rotate and End of Interrupt modes and combinations of the two. 000 = ~~Rotate in Auto EOI Mode (Clear)~~ Reserved 001 = Non-specific EOI command 010 = No Operation 011 = *Specific EOI Command 100 = ~~Rotate in Auto EOI Mode (Set)~~ Reserved 101 = Rotate on Non-Specific EOI Command 110 = *Set Priority Command 111 = *Rotate on Specific EOI Command *L0 – L2 Are Used

3. RAID 1 Description

The second bullet of section 5.16.6 Intel® Rapid Storage Technology Configuration is changed to:

Data redundancy is offered through RAID Level 1, which performs mirroring.

4. USB Register Correction

a. Section 16.1.31 EHCIIR1—EHCI Initialization Register 1 is modified as shown:

16.1.31 EHCIIR1—EHCI Initialization Register 1 (USB EHCI—D29:F0, D26:F0)

Offset Address: 84h–87h Attribute: R/W
Default Value: 83088E01h Size: 32-bit

Bit	Description
31:29	Reserved
28	EHCI Prefetch Entry Clear — R/W. 0 = EHC will clear prefetched entries in DMA. 1 = EHC will not clear prefetched entries in DMA
27:19	Reserved
18	EHCI Initialization Register 1 Field 2— R/W. BIOS may program this field.
17:11	Reserved
10:8	EHCI Initialization Register 1 Field 1— R/W. BIOS may program this field.
7:5	Reserved
4	**Intel® Pre-fetch Based Pause Enable** — R/W. 0 = Intel Pre-fetch Based Pause is disabled. 1 = Intel Pre-fetch Based Pause is enabled.
3:0	Reserved

b. Section 16.1.32 EHCIIR2—EHCI Initialization Register 2 is modified as shown:

EHCIIR2—EHCI Initialization Register 2 (USB EHCI—D29:F0, D26:F0)

Offset Address: 88h–8Bh Attribute: R/W
Default Value: 04000010h Size: 32-bit

Bit	Description
31:8	Reserved
7	**EHCI Initialization Register 2 Field 2** — R/W. BIOS may program this field.
6	Reserved
5	**EHCI Initialization Register 2 Field 1** — R/W. BIOS may program this field.
4:0	Reserved

c. Section 16.1.38 EHCIIR3—EHCI Initialization Register 3 is modified as shown:

EHCIIR3—EHCI Initialization Register 3 (USB EHCI—D29:F0, D26:F0)

Offset Address: F4h–F7h Attribute: R/W
Default Value: 00408588h Size: 32-bit

Bit	Description
31	**EHCIIR3 Write Enable** — R/W. 0 = Writes to the EHCIIR3 register are disabled 1 = If set, the values of the EHCIIR3 register may be modified

Bit	Description
30:24	Reserved
23:22	**EHCI Initialization Register 3 Field 1** — R/W. BIOS may program this field.
21:0	Reserved

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Specification Clarification

1. GPIO Lock Clarification

The following note is added to section 5.15.4 GPIO Registers Lockdown:

Note: All other GPIO registers not listed here are not be locked by GLE.

2. PME_Turn_Off TLP

The following note is added to section 5.2.2.1 S3/S4/S5 Support:

Note: The PME_Turn_Off TLP messaging flow is also issued during a host reset with and without power cycle. Refer to table 5-38 for a list of host reset sources.

3. t200 Timing Clarification

The following note is added to table 8-39 to clarify t200 timing.

Note: Measured from VccRTC-10% to RTCRST# reaching 55%*VccRTC. VccRTC is defined as the final settling voltage that the rail ramps.

4. SPI Flash Regions Update

Use below sentences to replace the sentences which marked in captured picture in section 5.24.1.2.1.

"Flash Descriptor and Intel ME region are the require regions. Flash Descriptor has to be in Region 0 and Region 0 must be located in the first sector of Device 0 (offset 10)".

5.24.1.2.1 SPI Flash Regions

In Descriptor Mode the Flash is divided into five separate regions:

Region	Content
0	Flash Descriptor
1	BIOS
2	Management Engine
3	Gigabit Ethernet
4	Platform Data

Only three masters can access the four regions: Host processor running BIOS code, Integrated Gigabit Ethernet and Host processor running Gigabit Ethernet Software, and Management Engine. The only required region is Region 0, the Flash Descriptor. Region 0 must be located in the first sector of device 0 (offset 0).

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Documentation Changes

1. Controller Link Updates

Controller Link is supported on all platforms. “Mobile Only” in table 8-9 should be removed.

VOH_CL1/ VOL_CL1	**Controller Link Signals:** Mobile Only: CL_CLK1, CL_DATA1

2. Miscellaneous Typographical Error Corrections

a. Occurrences of SM_BASE are changed to SMB_BASE throughout the document

b. In table 15-1 SATA Controller PCI Register Address Map (SATA–D31:F5), the mnemonic for SATA Capability Register 0 is changed from SCAP0 to SATACR0 and the mnemonic for SATA Capability Register 1 is changed from SCAP1 to SATACR1.

Table 15-1. SATA Controller PCI Register Address Map (SATA-D31:F5)

Offset	Mnemonic	Register Name	Default	Type
A8h–ABh	SATACR0	SATA Capability Register 0	0010B012h	RO
ACh–AFh	SATACR1	SATA Capability Register 1	00000048h	RO

3. Reset Behavior Updates

Table 5-35 and notes update as below.

Table 5-35. Causes of Host and Global Resets

Trigger	Host Reset without Power Cycle[1]	Host Reset with Power Cycle[2]	Global Reset with Power Cycle[3]	Straight to S5 (Host Stays there)
Write of 0Eh to CF9h Register when Global Reset Bit=0b	No	Yes	No (Note 4, 5)	
Write of 06h to CF9h Register when Global Reset Bit=0b	Yes	No	No (Note 4, 5)	
Write of 06h or 0Eh to CF9h Register when Global Reset Bit=1b	No	No	Yes	
SYS_RESET# Asserted and CF9h Bit 3 = 0	Yes	No	No (Note 4, 5)	
SYS_RESET# Asserted and CF9h Bit 3 = 1	No	Yes	No (Note 4, 5)	
SMBus Slave Message received for Reset with Power Cycle	No	Yes	No (Note 4, 5)	
SMBus Slave Message received for Reset without Power Cycle	Yes	No	No (Note 4, 5)	
TCO Watchdog Timer reaches zero two times	Yes	No	No (Note 4, 5)	
Power Failure: PWROK signal goes inactive in S0/S1 or RSMRST# asserts	No	No	Yes	

Table 5-35. Causes of Host and Global Resets

Trigger	Host Reset without Power Cycle[1]	Host Reset with Power Cycle[2]	Global Reset with Power Cycle[3]	Straight to S5 (Host Stays there)
SYS_PWROK Failure: SYS_PWROK signal goes inactive in S0/S1	No	No	Yes	
Processor Thermal Trip (THRMTRIP#) causes transition to S5 and reset asserts	No	No	No	Yes
Power Button 4 second override causes transition to S5 and reset asserts	No	No	No	Yes
Special shutdown cycle from processor causes CF9h-like PLTRST# and CF9h Global Reset Bit = 1	No	No	Yes	
Special shutdown cycle from processor causes CF9h-like PLTRST# and CF9h Global Reset Bit = 0 and Bit 3 = 1	No	Yes	No (Note 4, 5)	
Special shutdown cycle from processor causes CF9h-like PLTRST# and CF9h Global Reset Bit = 0 and Bit 3 = 0	Yes	No	No (Note 4, 5)	
Intel® Management Engine Triggered Host Reset without power cycle	Yes	No	No (Note 4, 5)	
Intel Management Engine Triggered Host Reset with power cycle	No	Yes	No (Note 4, 5)	
Intel Management Engine Watchdog Timer Timeout	No	No	No	Yes
Intel Management Engine Triggered Global Reset	No	No	Yes	
Intel Management Engine Triggered Host Reset with power down (host stays there)	No	Yes (Note 6)	No (Note 4, 5)	
PLTRST# Entry Time-out	No	No	Yes	
S3/4/5 Entry Timeout	No	No	No	Yes
PROCPWRGD Stuck Low	No	No	Yes	
Power Management Watchdog Timer	No	No	No	Yes
Intel Management Engine Hardware Uncorrectable Error	No	No	No	Yes

Notes:

1. The PCH is allowed to drop this type of reset request if received while the system is in S3/S4/S5.
2. PCH must not drop this type of reset request if received while system is in a software-entered S3/S4/S5 state. However, the PCH is allowed to perform the reset without executing the RESET_WARN protocol in these states.
3. The PCH does not send warning message to processor, reset occurs without delay.
4. Trigger will result in Global Reset with power cycle if the acknowledge message is not received by the PCH.
5. Trigger can result in Global Reset if "Promote Host Partition Reset to Global Reset" policy bit is set to '1'.
6. The PCH waits for enabled wake event to complete reset.

4. CPU_PWR_FLR removal

Remove the last line CPU_PWR_FLR bit in the table 5-36 Event Transitions that Cause Messages.

Table 5-36. Event Transitions that Cause Messages

Event	Assertion?	de-assertion?	Comments
INTRUDER# pin	yes	no	Must be in "S1 or hung S0" state
THRM# pin	yes	yes	Must be in "S1 or hung S0" state. Note that the THRM# pin is isolated when the core power is off, thus preventing this event in S3–S5.
Watchdog Timer Expired	yes	no (NA)	"S1 or hung S0" state entered
GPIO[11]/SMBALERT# pin	yes	yes	Must be in "S1 or hung S0" state
BATLOW#	yes	yes	Must be in "S1 or hung S0" state

5. DC Inputs Characteristics Tables Corrections

a. All notes are removed from the end of table 8-8 DC Characteristic Input Signal Association.

b. "(1)" removed from SML[1:0]CLK, SML[1:0]DATA in table 8-8 DC Characteristic Input Signal Association.

c. Table 8-9 DC Input Characteristics and its notes are modified as follows:

i) Note 11 is removed from VIL6.

ii) Note 10 is removed from VIL16.

iii) Note 8 is removed from the table.

6. Miscellaneous Documentation Corrections I

a. Usages of "display port" not referring to the DisplayPort interface are changed to "digital port" or "display interface" throughout the document as well as changing "display port" to DisplayPort when referring to the interface.

b. The attribute of TCO_EN (PMBASE+30h:bit 13) is changed from R/W to R/WL.

c. The attribute of GBL_SMI_EN (PMBASE+30h:bit 0) is changed from R/W to R/WL.

d. The second paragraph of section 5.21.2.1 Supported Addresses is removed.

e. The following sentence in section 5.21.2.6 Temperature Comparator and Alert:

In general the TEMP_ALERT# signal will assert within a 1–4 seconds, depending on the actual BIOS implementation and flow.

is changed to:

In general the TEMP_ALERT# signal will assert within 1–4 seconds, depending on the actual BIOS implementation and flow.

f. Section 5.21.2.8.2 title is changed from Power On to Block Read Special Handling.

g. Note 1 is added to PWM[3:0] in table 8-10 DC Characteristic Output Signal Association.

7. Function Level Reset Pending Status Register Correction

Section 10.1.16 FLRSTAT—Function Level Reset Pending Status Register is updated as shown:

Bit	Description
31:24	Reserved
23	**FLR Pending Status for EHCI #1 (D29)** — RO. 0 = Function Level Reset is not pending. 1 = Function Level Reset is pending.
22:16	Reserved
15	**FLR Pending Status for EHCI #2 (D26)** — RO. 0 = Function Level Reset is not pending. 1 = Function Level Reset is pending.
14:0	Reserved

8. Miscellaneous Documentation Corrections II

a. Section 10.1.65 FDSW—Function Disable SUS Well Register is updated as shown:

Bit	Description
7	**Function Disable SUS Well Lockdown (FDSWL)**— R/W 0 = FDSW registers are not locked down. 1 = FDSW registers are locked down and this bit will remain set until a global reset occurs. **NOTE:** This bit must be set when Intel® Active Management Technology is enabled.

b. Section 10.1.67 USBIR[0:13] - USB Initialization Register [0-13] is changed to USB Initialization Registers[13:0] - USB Initialization Register Port [13:0].

c. Section 15.1.36 title is changed to ATS-APM Trapping Status Register.

d. Section 16.1.37 mnemonic is changed to FLR_STAT.

e. Usages of "display port" not referring to the DisplayPort interface are changed to "digital port" or "display interface" throughout the document as well as changing "display port" to DisplayPort when referring to the interface.

f. The attribute of TCO_EN (PMBASE+30h:bit 13) is changed from R/W to R/WL.

g. The attribute of GBL_SMI_EN (PMBASE+30h:bit 0) is changed from R/W to R/WL.

h. The second paragraph of section 5.21.2.1 Supported Addresses is removed.

i. The following sentence in section 5.21.2.6 Temperature Comparator and Alert:

In general the TEMP_ALERT# signal will assert within a 1–4 seconds, depending on the actual BIOS implementation and flow.

is changed to:

In general the TEMP_ALERT# signal will assert within 1–4 seconds, depending on the actual BIOS implementation and flow.

j. Section 5.21.2.8.2 title is changed from Power On to Block Read Special Handling.

k. Remove "1.05 V Core Voltage" from Platform Controller Hub Features section.

l. The second paragraph of section 5.16.7 Intel® Rapid Storage Technology Configuration is replaced as follows:

By using the PCH's built-in Intel Rapid Storage Technology, there is no loss of additional PCIe/system resources or add-in card slot/motherboard space footprint used compared to when a discrete RAID controller is implemented.

m.Occurrences of "DOCK_RST#" are changed to "HDA_DOCK_RST#".

n. The default value for section 10.1.33 D22IP—Device 22 Interrupt Pin Register is changed from 00000001h to 00004321h.

o. R/W/C attribute is changed to R/WC.

9. EHCIIR4 Removal

Remove section 16.1.39 EHCIIR4- EHCI Initialization Register 4 (USB EHCI-D29:F0, D26:F0).

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