82562 Family ("E" & "G" series) 10/100 Mbps Platform LAN Connect (PLC) Devices

Stepping Information

May 2007

Revision 2.6

Notice: The 82562xx PLC may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in this document.

82562 Family ("G" & "E") Stepping Information

Revision History

Date	Version	Description
Feb. 2001	1.0	Initial release. (Intel Secret)
Apr. 2002	2.0	• Changed document status to Intel Confidential. • Added component identification marking information for the 82562EX and 82562EZ. • Added "Packet Rejected after ESD Symbol" in the errata section. • Replaced global references to "82562" to "82562xx," where 82562xx denotes any member of the 82562 Family of PLC devices (for example, 82562EM &82562G).
Sept. 2002	2.1	Added errata number six, "Packets with Valid CRC Checksums and Invalid Length Fields Discarded."
Mar. 2003	2.2	Changed document status from Intel Confidential to no status.
Sept. 2005	2.5	Added the 82562EP product codes.
May 2007	2.6	Included "G" series information.

Preface

Note: This document uses the "82562xx" to denote any member of the 82562 Family of PLC devices (for example, "82562ET" or "82562G").

This document is an update to the specifications contained in the 82562xx 10/100 Mbps Platform LAN Connect (PLC) Datasheet, and contains issues affecting all design using the 82562xx device.

This document is intended for hardware system manufacturers and software developers of applications, operating systems or tools. It contains Specification Changes, Errata, Specification Clarifications, and Document Changes.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Errata may cause the 82562xx's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Product Code

The product ordering code for the 82562ET is: DA82562ET.

The product ordering code for the 82562EM is: DA82562EM.

The product ordering code for the 82562EX is: DA82562EX.

The product ordering code for the 82562EZ is: DA82562EZ.

The product ordering code for the 82562EP is: RC82562EP.

The product ordering code for the lead-free 82562EP is: PC82562EP.

The product ordering code for the 82562GT is: EP82562GT.

The product ordering code for the 82562GX is: GD82562GX (leaded), LU82562GX (unleaded).

The product ordering code for the 82562GZ is: GD82562GZ (leaded), LU82562GZ (unleaded).

The product ordering code for the 82562G is: EP82562G..

Identification Information

82562xx Component Marking Identification

82562ET

Device	Stepping	Top Marking	Q-specification	MM Number	Notes
82562ET	A-1	82562ET	Q420	827447	Samples (757 units shipped in 1999/2000)
82562ET	A-2	82562ET	Q423	828526	Samples (484 units shipped in 2000)
82562ET	A-2	82562ET	STD	829706	Production - Tray
82562ET	A-2	82562ET	SL4KM	830642	Production - Tape and Reel

82562EM

Device	Stepping	Top Marking	Q-specification	MM Number	Notes
82562EM	A-1	82562EM	Q421	827448	Samples (1340 units shipped in 2000)
82562EM	A-2	82562EM	Q424	828529	Samples (1800 units shipped in 2000)
82562EM	A-2	82562EM	STD	829707	Production - Tray
82562EM	A-2	82562EM	SL4KN	830645	Production - Tape and Reel

82562EX

Device	Stepping	Top Marking	Q-specification	MM Number	Notes
82562EX	A-2	82562EX	Q509	844002	Samples
82562EX	A-2	82562EX	STD	844997	Production - Tray
82562EX	A-2	82562EX	SL663	844999	Production - Tape only

82562EZ

Device	Stepping	Top Marking	Q-specification	MM Number	Notes
82562EZ	A-2	82562EZ	Q508	844001	Samples
82562EZ	A-2	82562EZ	STD	845000	Production - Tray
82562EZ	A-2	82562EZ	SL662	845001	Production - Tape only

82562EP

Device	Stepping	Top Marking	S-specification	MM Number	Notes
82562EP	B-1	PC82562EP	S L7QW	862943 863061	Production - Tape only Production - Tape & Reel only
82562EP	B-1	PC82562EP	S L5NF	832361 836312	Production - Tape only Production - Tape & Reel only

82562G

Device	Stepping	Top Marking	S-specification	MM Number	Notes
82562G	A-0	82562G	STD S L899	868030 868036	Production - Tape only Production - Tape & Reel only

82562GT

Device	Stepping	Top Marking	S-specification	MM Number	Notes
82562GT	A-0	82562GT	STD S L7RL	863269 863271	Production - Tape only Production - Tape & Reel only

82562GX

Device	Stepping	Top Marking	S-specification	MM Number	Notes
82562GX	A-0	82562GX	STD S L8B9	869134 869135	Production - Tape only Production - Tape & Reel only

82562GZ

Device	Stepping	Top Marking	S-specification	MM Number	Notes
82562GZ	A-0	82562GZ	STD S L7QQ	862934 862928	Production - Tape only Production - Tape & Reel only

82562V

Device	Stepping	Top Marking	S-specification	MM Number	Notes
82562V	A-0	82562V	STD S L8ZU	877092 877090	Production - Tape only Production - Tape & Reel only

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed 82562xx steppings. Intel intends to fix some of the errata in future steppings of the component and to account for other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes used in summary table:

X:	Specification Change, Erratum, or Specification Clarification that applies to this stepping.
Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future stepping of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.
Shaded:	This Item is either new or modified from the previous version of the document.

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Specification Changes

1. Exclude Pin X1 from the Exclusive OR (XOR) Tree Chain

Explanation: The X1 pin of the 82562xx should not be included in the eXclusive OR (XOR) tree.

Implication: The inclusion of the X1 pin introduces noise from the crystal into the XOR tree. To prevent the noise, the X1 is excluded from the XOR tree chain. This is done internally in the silicon and affects board level testing only.

Status: This was fixed in the A-2/B-1 stepping and the appropriate definition changes were made to all relative documents.

2. Exclusive OR (XOR) Tree Mode Changes

Explanation: The eXclusive OR (XOR) tree mode settings differ between the A-1 stepping and A-2/B-1 stepping. The modes are configured using the four of the miscellaneous control signals: Test Enable (TESTEN), Test Clock (ISOL_TCK), Test Input (ISOL_TI), and Test Execute (ISOL_TEX).

The mode settings for the 82562xx A-1 is as follows:

TESTEN	ISOL_TCK	ISOL_TI	ISOL_TEX	Mode
0	0	0	0	Normal operating mode
0	**0**	**1**	**1**	**XOR tree mode**
0	1	1	1	Isolate mode
1	1	1	1	Power down mode

The settings for the A-2/B-1 stepping is:

TESTEN	ISOL_TCK	ISOL_TI	ISOL_EX	Mode
0	0	0	0	Normal operating mode
1	**0**	**0**	**0**	**XOR tree mode**
0	1	1	1	Isolate mode
1	1	1	1	Power down mode

Implication: To insure proper test results, designs using the XOR tree test function need to incorporate the necessary changes.

Status: XOR tree mode configuration changes were implemented between the A-1 and A-2/B-1 steppings of the 82562xx. The appropriate definition changes were made to all relative documents.

Errata

1. Auto-Negotiation Fails to Link

Problem: During the auto-negotiation process, the 82562xx may fail to establish link. This is due to a hardware race condition that only exists during the process. This has been observed with hubs and switches from several vendors.

Implication: The affected system will fail to establish link during the auto-negotiation process. This does not have any effect in situations where link has already been established.

Workaround: The autonegotiation bit should be disabled and the Force 10 or Force 100 mode should be used. This is accomplished by configuring the MDI Control Register as follows:

MDI Control Register (Register 0)

Speed Selection (bit 13) = 0 for 10 Mbps or 1 for 100 Mbps

Auto Negotiation Enable (bit 12) = 0

Duplex Mode (bit 8) = 0 for half duplex or 1 for full duplex

Status: This erratum has been fixed in the A-2/B-1 stepping of the 82562xx device.

2. Long Cable Receive Performance

Problem: The 82562xx exhibits poor receive performance using long cables. This occurs because of a reference voltage in the baseline wander circuitry.

Implication: The 82562xx may lose link during receive operation when cables longer than 75 meters are used.

Workaround: The use of shorter cables, less than 50 meters, will improve reliability.

Status: This anomaly has been fixed in the 82562xx A-2/B-1 stepping.

3. Hardware Integrity Fails Using Low Power

Problem: During low voltage conditions, if the Hardware Integrity feature is enabled, the 82562xx incorrectly detects a hardware integrity failure. This occurs due to improper threshold voltages on the hardware integrity comparators.

Implication: The implication of this erratum is that hardware integrity test fails.

Workaround: The Hardware Integrity feature should be disabled by setting the HWI Enabled bit (bit 15 of the HWI Control Register) to 0. (Setting this bit to 1 enables the Hardware Integrity feature.)

Status: This issue has been fixed in the A-2/B-1 stepping of the 82562xx device.

4. Failure to Enter Reduced Power Mode with MDI-X Enabled

Problem: If the LAN cable is disconnected (valid to invalid link transition) when Reduced Power Down is enabled, the 82562xx should enter a reduced power down mode. However, this does not occur if MDI/MDI-X is concurrently enabled. Switching noise from the MDI/MDI-X circuit causes the cable disconnect transition to be incorrectly recorded resulting in a failure to enter the reduced power mode.

Implication: Power consumption will be slightly higher than expected with the link disconnected.

Workaround: The MDI/MDI-X feature should be disabled if the reduced power down functionality is needed.

Reduced Power Down is enabled by setting the Reduced Power Down bit (bit 11) in the MDI Control Register (register 0) to 1.

MDI/MDI-X is enabled by setting the MDI/MDI-X Enable bit (bit 7) in the MDI/MDI-X Control Register (register 28) to 1, and disabled by setting the MDI/MDI-X Enable to 0.

Status: This has been fixed in the 82562xx A-2/B-1 stepping.

5. Packet Rejected after ESD Symbol

Problem: The 82562xx devices may sometimes reject packets with a non-idle symbol after the end of stream (ESD) delimiter symbol.

Implication: In a network configuration, this situation may be encountered. The link partner should always transmit an idle after the ESD character. If the packet is rejected, upper layer protocols will request a re-transmission to recover from the dropped frame.

Workaround: There is no workaround for this anomaly.

Status: There are no plans to fix this erratum.

6. Packets with Valid CRC Checksums and Invalid Length Fields Discarded

Problem: The 82562xx devices do not discard packets with a valid CRC Checksum and invalid Length field.

Implication: The transmitting station typically generates an accurate length field. Since the entire packet (including the Length field) is protected by one CRC Checksum, if the Length field is corrupted or the data field truncated during packet transmission, the packet is discarded due to an invalid CRC.

Workaround: There are no workarounds for this anomaly.

Status: There are no plans to fix this erratum.

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