

Intel[®] 946 Express Chipset Family

Specification Update

– For the Intel[®] 82946GZ Graphics and Memory Controller Hub (GMCH) and Intel[®] 82946PL Memory Controller Hub (MCH)

September 2006



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The Intel® 82946GZ GMCH and 82946PL MCH may contain design defects or errors known as errata, which may cause the product to deviate from published specifications. Current characterized errata are available on request.

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Revision History

Revision	Description	Date
-001	Initial release	June 2006
-002	Added C2 stepping Updated Erratum #1 Added documentation change #1 and #2	September 2006

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Preface

This document is an update to the specifications contained in the documents listed in the following Affected Documents/Related Documents table. It is a compilation of device and document errata and specification clarifications and changes, and is intended for hardware system manufacturers and for software developers of applications, operating system, and tools.

Information types defined in the Nomenclature section of this document are consolidated into this update document and are no longer published in other documents. This document may also contain information that has not been previously published.

Affected Documents

Document Title	Document Number/Location
Intel® 946 Express Chipset Family Datasheet	313083-001

Nomenclature

Errata are design defects or errors. Errata may cause the 82946GZ/82946PL's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).



Summary Tables of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications or Documentation Changes, which apply to the listed MCH steppings. Intel intends to fix some of the errata in a future stepping of the component, and to account for the other outstanding issues through documentation or Specification Changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

- X: Erratum, Specification Change or Clarification that applies to this stepping.
- (No mark) or (Blank Box): This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Status

- Doc: Document change or update that will be implemented.
- PlanFix: This erratum may be fixed in a future stepping of the product.
- Fixed: This erratum has been previously fixed.
- NoFix: There are no plans to fix this erratum.

Row

- Shaded: This item is either new or modified from the previous version of the document.



Number	Steppings		Plans	ERRATA
	C1	C2		
1	X		Fixed	Integrated GFX Corruption May Occur When Overlay Enabled (Intel® 82946GZ Only)
2	X	X	NoFix	Data Recovery Clock (DRC) Lock Up

NOTE: NA means Not Applicable.

Number	SPECIFICATION CHANGES
	There are no Specification Changes in this Specification Update revision.

Number	SPECIFICATION CLARIFICATIONS
	There are no Specification Clarifications in this Specification Update revision.

Number	DOCUMENTATION CHANGES
1	Feature page graphics core frequency and pixel rate
2	System memory bandwidth reference



Identification Information

Component Identification via Programming Interface

The Intel 82946GZ GMCH may be identified by the following register contents:

Stepping	Vendor ID ¹	Device ID ²	Revision Number ³
C1	8086h	2970	02h
C2	8086h	2970	03h

The Intel 82946PL MCH may be identified by the following register contents:

Stepping	Vendor ID ¹	Device ID ²	Revision Number ³
C1	8086h	2970	02h
C2	8086h	2970	03h

NOTES:

1. The Vendor ID corresponds to bits 15:0 of the Vendor ID Register located at offset 00–01h in the PCI function 0 configuration space.
2. The Device ID corresponds to bits 15:0 of the Device ID Register located at offset 02–03h in the PCI function 0 configuration space.
3. The Revision Number corresponds to bits 7:0 of the Revision ID Register located at offset 08h in the PCI function 0 configuration space.

Component Marking Information

The Intel 829446GZ GMCH may be identified by the following component markings:

Stepping	Product	S-Spec	Top Marking	Notes
C1	GMCH	SL9NZ	LE82946GZ	Production – pb free
C2	GMCH	SL9R4	LE82946GZ	Production – pb free

The Intel 82946PL MCH may be identified by the following component markings:

Stepping	Product	S-Spec	Top Marking	Notes
C1	MCH	SL9NV	LE82946PL	Production – pb free
C2	MCH	SL9QY	LE82946PL	Production – pb free



Errata

1. Integrated GFX Corruption May Occur When Overlay Enabled (Intel® 82946GZ Only)

- Problem:** When using the Intel® 82946GZ overlay feature video corruption may occur.
- Implication:** Visual corruption may be experienced after media applications that utilize overlay have been closed. This corruption can be seen when a window pane is moved around on the desktop or if any 3d application is running.
- Workaround:** The graphics driver will enable Sprite C as the primary overlay function. Hardware overlay will be disabled for Intel® 946GZ Express Chipset Family platforms.
- Status:** Fixed. For affected steppings, see the Summary Table of Changes

2. Data Recovery Clock (DRC) Lock Up

- Problem:** If the S1 ACPI state is enabled on the Intel® 946 Express chipset family, and L1 PCI Express* Link Power Management is supported by a PCI Express* card inserted into the x16 PCI Express* port, the system may on rare occasions experience abnormal system behavior upon resuming from S1.
- Implication:** On rare occasions when performing S1 ACPI stress test cycling on an Intel® 946 Express chipset platform, the system may experience abnormal behavior, such as correctable bit errors, system hang, or a blank screen.
- Workaround:** Disable S1 support via BIOS.
Or
Ensure L1 PCI Express* link power management is not supported by an external PCI Express* card.
- Status:** No Plan to Fix.

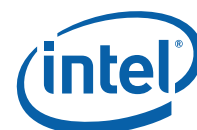
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Specification Changes

There are no Specification Changes in this Specification Update revision.

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Specification Clarifications

There are no specification clarifications in this Specification Update revision.

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Documentation Changes

1. Feature page graphics core frequency and pixel rate

On page 13 of the Intel® 946 Express Chipset Family Datasheet the Integrated Graphics Device sub bullet will be updated with the correct graphics core frequency and pixel rate as shown below.

- Core frequency of 667MHz
- 1.33Gp/s pixel rate

2. System memory bandwidth reference

Section 9.5 on page 256 of the Intel® 946 Express Chipset Family Datasheet will be updated with the correct memory bandwidth access rate of 10.6GB/s.

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